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Hardware Implementation of Soft Mapper/Demappers in Iterative EP-based Receivers

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Abstract—This paper presents a comprehensive study and implementations onto FPGA device of an Expectation Propagation (EP)-based receiver for QPSK, 8-PSK, and 16-QAM. To the best of our knowledge, this is the first for this kind of receiver. The receiver implements a Frequency Domain (FD) Self-Iterated Linear Equalizer (SILE), where EP is used to approximate the true posterior distribution of the transmitted symbols with a simpler distribution. Analytical approximations for the EP feedback generation process and the three constellations are applied to lessen the complexity of the soft mapper/demapper architectures. The simulation results demonstrate that the fixed-point version performs comparably to the floating-point. Moreover, implementation results show the efficiency in terms of FPGA resource usage of the proposed architecture.

Index Terms—Expectation Propagation, Frequency Domain Self-Iterated Linear Equalizer, Analytical approximations, architecture design, FPGA prototyping

I. INTRODUCTION

In digital communication systems, achieving minimal error rates in data detection and/or decoding requires the resolution of a Maximum A Posteriori (MAP) or Maximum Likelihood (ML) problem [1]. However, the computational complexity of resolving such criteria is often prohibitive, particularly in real-world frequency selective channels, where the number of computations increases exponentially with factors such as data length, modulation order, and channel memory. As a result, practical receiver design often involves applying simplifying hypotheses and approximations. One promising approach in the context of Frequency Domain (FD) Linear Equalization (LE) is equalizers designed with Expectation Propagation (EP). Indeed, they have demonstrated an appealing trade-off between performance and computational complexity [2].

In this paper, a comprehensive study and implementation of an EP-based receiver for communications over frequency selective channels using standard Phase Shift Keying (PSK) or Quadrature Amplitude Modulation (QAM) constellations is presented. The receiver implements an FD Self-Iterated Linear Equalizer (SILE), where EP is applied to approximate the true posterior distribution of the transmitted symbols with a simpler distribution that can be easily manipulated. Previously, the implementation of a simplified EP receiver for multiple

antenna receivers has been reported in [3]. A low complexity EP detector for sparse code multiple access was also proposed in [4]. However, the authors only study the impact of simplifications on the performance and estimate the computational cost of their proposal per operation type. Simplified EP-based FD equalization is studied in [5]. Similar to the previous case, only a computational complexity assessment was provided. To the best of our knowledge, we propose the first hardware implementation of an EP-based FD SILE receiver.

The contributions of this paper are the following:

- 1) Methods to reduce the complexity of the EP-based FD-SILE algorithm are proposed, which are different from the ones in [5]. They include a new way to generate the EP soft feedback and also a new method to calculate extrinsic Log-Likelihood Ratios (LLR) for 8-PSK.
- 2) A fixed-point version of the model enables to verify that the degradation in terms of performance due to these new algorithmic simplifications is limited.
- 3) The implementation of soft mapper/demapper architectures is carried out on a Field Programmable Gate Array (FPGA), specifically the PYNQ Z2 board.

The PYNQ Z2 board contains a device that combines an ARM processor and an FPGA, which enables easier Ethernet communication. The implementation was done in a Hardware in the Loop (HIL) configuration, with the EP parts implemented onto the FPGA, while the others run on a computer thanks to py-AFF3CT, a Python wrapper for the Forward Error Correction Toolbox AFF3CT [6]. The analysis of FPGA resource usage shows very low complexity overhead for three different and widely used constellations. These results confirm that the proposed EP equalizer is potentially a good candidate for practical implementation even on cost- and complexity-constrained digital communication equipment.

The paper is organized as follows. A description of the FD SILE receiver with EP is provided in Section II. The simplifications and analytical approximations applied to the soft mapper/demapper to decrease its complexity are presented in Section III. The fixed-point conversion analysis to facilitate the soft mapper/demapper architecture design is presented in Section IV. The architecture implementation and FPGA prototyping, with the experimental setup and resource usage, are detailed in Section V. The paper is concluded in Section VI.

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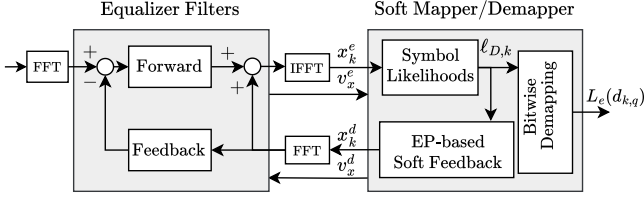


Fig. 1: FD SILE functional structure.

II. EP-BASED FD-SILE ALGORITHM

Expectation Propagation (EP) is a powerful technique exploited in statistical inference for approximating complex probability distributions by simpler distributions from the exponential family through moment matching. The FD self-iterated linear equalizer (SILE) algorithm derived in [2] is based on EP to compute extrinsic soft decision feedback.

The functional structure of the iterative receiver is illustrated in Fig. 1. The received signal is first mapped to the frequency domain thanks to an FFT function. Then, a linear Minimum Mean Square Error (MMSE) filter with interference cancellation is used for equalization. In addition to the channel frequency response and noise statistics, the filter computation requires the statistics of the soft decision feedback [2].

The receiver performs S self-iterations which go through the equalizer, the soft demapper, and the EP-based soft mapper. At self-iteration $s = 0, \dots, S$, after the filtering stage, the equalized symbols in the time-domain $x_k^{e(s)}$ are fed into the soft demapper, along with an estimate of the residual post-equalization noise and interference variance $v_x^{e(s)}$. The soft demapper then estimates the unnormalized log-likelihood distribution $\ell_{D,k}^{(s)}(\alpha)$ with

$$\ell_{D,k}^{(s)}(\alpha) = -|x_k^{e(s)} - \alpha|^2 / v_x^{e(s)}, \forall k, \forall \alpha \in X, \quad (1)$$

where X is the symbol constellation and K is the equalized block length.

If $s < S$, the EP soft mapper computes the feedback for the next iteration by first computing the normalized a posteriori distribution in the linear domain, with $\forall k, \forall \alpha \in X$,

$$D_k^{(s)}(\alpha) = \exp(\ell_{D,k}^{(s)}(\alpha)) / \sum_{\alpha' \in X} \exp(\ell_{D,k}^{(s)}(\alpha')). \quad (2)$$

Next, the soft a posteriori symbol estimates $\mu_k^{d(s)}$ and variances $\gamma_x^{d(s)}$ can be computed with the moments of $D_k^{(s)}$:

$$\mu_k^{d(s)} = \sum_{\alpha \in X} \alpha D_k^{(s)}(\alpha), \forall k, \quad (3)$$

$$\gamma_{x,k}^{d(s)} = \sum_{\alpha \in X} |\alpha|^2 D_k^{(s)}(\alpha) - |\mu_k^{d(s)}|^2, \forall k, \quad (4)$$

$$\gamma_x^{d(s)} = K^{-1} \sum_{k=1}^K \gamma_{x,k}^{d(s)}, \quad (5)$$

The average variance $\gamma_x^{d(s)}$ enables the proper use of EP for FD equalization. Finally, the extrinsic soft feedbacks based on EP are obtained by performing a Gaussian PDF division:

$$x_k^{d(s+1)} = \frac{\mu_k^{d(s)} v_x^{e(s)} - x_k^{e(s)} \gamma_x^{d(s)}}{v_x^{e(s)} - \gamma_x^{d(s)}}, v_x^{d(s+1)} = \frac{v_x^{e(s)} \gamma_x^{d(s)}}{v_x^{e(s)} - \gamma_x^{d(s)}}. \quad (6)$$

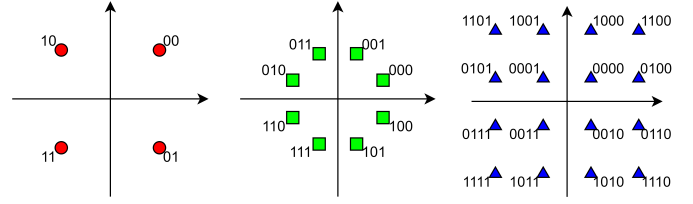


Fig. 2: Constellation bit values.

Exponential smoothing could be applied across self-iterations, as done in [5], for stabilizing convergence. But, in order to simplify this initial work, it is not considered.

At the last self-iteration $s = S$, only bit-wise extrinsic LLRs for soft decoding are computed [5]:

$$L_e(d_{k,q}) = \log \sum_{\alpha \in X_q^0} e^{\ell_{D,k}^{(s)}(\alpha)} - \log \sum_{\alpha' \in X_q^1} e^{\ell_{D,k}^{(s)}(\alpha')}. \quad (7)$$

It is important to note that the FD SILE algorithm is considerably less computationally intensive than alternative iterative equalizers in the time domain [2]. Nevertheless, logarithmic and exponential operations within soft mapping and demapping still pose a significant implementation challenge and scale poorly with the constellation size. To illustrate this point, the number of floating-point operations (FLOP) involved in the exact equalization, soft mapping, and soft demapping are provided in Table I. These numbers mostly depend on the constellation size and the number of self-iterations. They are obtained through the same approach as in [2], where operations such as addition, multiplication, and division operation are counted with weights.

III. ANALYTICAL APPROXIMATIONS

In this section, we discuss further simplifications of the complexity of EP-based soft feedback computation for practical constellations of QPSK, 8-PSK, and 16-QAM.

A. Simplified EP-based feedback computation

In [5], the use of the asymptotic a posteriori mean-square error (MSE) $\tilde{\gamma}_x^d$, as a function of v_x^e , instead of γ_x^d , is shown to reduce soft mapping complexity. Moreover, it also improves receiver robustness. In particular, when tabulating the auxiliary quantity $C_{EP}(v_x^e) = \tilde{\gamma}_x^d / (v_x^e - \tilde{\gamma}_x^d)$, the computational complexity can be further reduced through

$$v_x^{d(s+1)} = v_x^{e(s)} C_{EP}(v_x^{e(s)}), \quad (8)$$

$$x_k^{d(s+1)} = \mu_k^{d(s)} + C_{EP}(v_x^{e(s)}) (\mu_k^{d(s)} - x_k^{e(s)}), \forall k. \quad (9)$$

Although this alleviates part of the soft mapping complexity issue, the computation of a posteriori estimates μ_k^d and extrinsic LLRs $L_e(d_{k,q})$ still remains computationally intensive.

B. Simplified soft demapping

In [5], piece-wise linear approximations of $\mu_k^{d(s)}$ as a function of $x_k^{e(s)}$ were proposed to lower the computational complexity of $\mu_k^{d(s)}$ with small performance degradation. However,

Const.	S	Equ.	Exact		Simplified	
			Demap.	Map.	Demap.	Map.
QPSK	0	74	58	0	3	0
	1	153	58	105	6	26
	2	231	58	210	9	53
8-PSK	0	74	195	0	12	0
	1	153	195	185	24	33
	2	231	195	370	36	67
16-QAM	0	74	548	0	14	0
	1	153	548	345	28	40
	2	231	548	690	42	81

Table I: Computational complexity of components of FD SILE in FLOP/symbol.

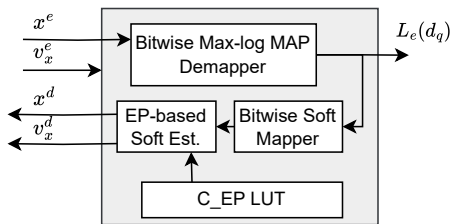


Fig. 3: Simplified bitwise soft demapper.

this approach is limited to square QAM constellations, and it is too complex for turbo-equalization. In this work, a *new simplified computation of EP-based feedback is proposed* based on bitwise soft demapping, followed by bitwise soft mapping, for computing both $L_e(d_q)$ and μ^d . This structure is illustrated in Fig. 3. The symbol index k and the iteration index s have been dropped for the sake of readability.

A widespread means of carrying out soft demapping with reasonable complexity is through the simplification of the log-sum-exp, twice used in eq. (7). Indeed, one can replace this function with a maximum (max-log-MAP) [7], and remains optimal for the QPSK constellation. However, some performance loss can be expected for higher-order constellations.

Besides, the max-log-MAP demapper remains prohibitive for high-order constellations. With M being the constellation size, for each symbol, it requires computing M squared-distances and performing M comparisons for each of the $Q = \log_2 M$ bits. Various proposals in the literature provide direct linear approximations of max-log-MAP LLRs $L_e(d_q)$ as a function of x^e and v_x^e for each q , computed through the geometric properties of each constellation. Indeed, some practical implementations in the literature [8] rely on analytical expressions of the extrinsic max-log MAP LLRs. In particular, there are closed-form analytical equations for Gray-mapped QAM constellations [9]. Proposed expressions for the QPSK and 16-QAM constellations are provided in Table II.

But regarding non-square constellations, as the 8-PSK, the geometric characterization of max-log MAP LLRs does not systematically have closed-form expressions. For such Gray-mapped PSK constellations, [10] exploits labeling properties of the constellation, and the hard decision on the equalized symbol to compute only two distances per LLR. This method performs exact max-log-MAP by exploiting the properties of

Constellation	Bitwise Log-Likelihood Ratios
QPSK	$L_e(d_1) = 2\sqrt{2}R(x^e)/v_x^e$, $L_e(d_2) = 2\sqrt{2}I(x^e)/v_x^e$
16-QAM	$L_e(d_1) = 4d(2d - I(x^e))/v_x^e$
	$L_e(d_2) = 4d(2d - R(x^e))/v_x^e$
	$L_e(d_3) = \begin{cases} 4dI(x^e)/v_x^e, & I(x^e) < 2d \\ 8d(I(x^e) - d)/v_x^e, & I(x^e) > 2d \\ 8d(I(x^e) + d)/v_x^e, & I(x^e) < -2d \end{cases}$
	$L_e(d_4) = \begin{cases} 4dR(x^e)/v_x^e, & R(x^e) < 2d \\ 8d(R(x^e) - d)/v_x^e, & R(x^e) > 2d \\ 8d(R(x^e) + d)/v_x^e, & R(x^e) < -2d \end{cases}$

Table II: Bitwise soft demapping expressions.

LUT _{8PSK}	$\Delta_{\alpha^*,1}$	$\Delta_{\alpha^*,2}$	$\Delta_{\alpha^*,3}$
α_0	1.0824 - 1.0824j	2.6131 - 1.0824j	0.0000 + 1.5307j
α_1	1.0824 - 1.0824j	1.5307 - 0.0000j	-1.0824 + 2.6131j
α_2	-1.0824 - 1.0824j	2.6131 + 1.0824j	0.0000 + 1.5307j
α_3	-1.0824 - 1.0824j	1.5307 - 0.0000j	1.0824 + 2.6131j
α_4	1.0824 + 1.0824j	2.6131 + 1.0824j	0.0000 + 1.5307j
α_5	1.0824 + 1.0824j	1.5307 - 0.0000j	1.0824 + 2.6131j
α_6	-1.0824 + 1.0824j	2.6131 - 1.0824j	0.0000 + 1.5307j
α_7	-1.0824 + 1.0824j	1.5307 - 0.0000j	-1.0824 + 2.6131j

Table III: Look-up-table content for 8-PSK demapping.

Gray labeling for finding the likely closest symbol from the set opposite to the hard decision. However, the arithmetic computation of the opposite symbol and the computation of the formula with Euclidean distances still have a significant weight within the overall computational complexity.

Here we propose to further simplify the computation of 8-PSK LLRs in [10], by applying a semi-analytical approach [11]. Indeed, the max-log-MAP LLR is given by

$$L_e(d_q) = -(1 - 2\hat{d}_q^*)(|x^e - \alpha^*|^2 - |x^e - \alpha_q^*|^2)/v_x^e, \quad (10)$$

where α^* is the closest constellation point to x^e , with q^{th} bit of the α^* 's label being denoted \hat{d}_q^* . Furthermore, α_q^* is the constellation point that corresponds to the closest symbol to α^* that has the opposite value on the q^{th} bit.

Instead of computing $\alpha_q^*, \forall q$ with Q^2 additions as in [10], we rewrite the expression of the max-log-MAP LLR as

$$L_e(d_q) = (R(x^e)R(\Delta_{\alpha^*,q}) + I(x^e)I(\Delta_{\alpha^*,q}))/v_x^e, \quad (11)$$

where $\Delta_{\alpha^*,q} = 2(1 - 2\hat{d}_q^*)(\alpha^* - \alpha_q^*)$. Hence, $\Delta_{\alpha^*,q}$ can be precomputed and stored in a LUT, as shown in Table III, for each $\alpha^* \in X$ and $q = 1, \dots, Q$:

$$(\Delta_{\alpha^*,1}, \Delta_{\alpha^*,2}, \Delta_{\alpha^*,3}) = \text{LUT}_{8\text{PSK}}(\alpha), \alpha \in X. \quad (12)$$

To access the LUT, a hard decision has to be made through comparisons on x^e , to compute the symbol label m in decimal:

$$m = 4(I(x^e) < 0) + 2(R(x^e) < 0) + (|R(x^e)| < |I(x^e)|). \quad (13)$$

C. Simplified soft mapping

To simplify the computation of the soft symbol estimate μ^d from (3), analytical bitwise soft mapping can be applied. This enables to take into account probabilities on symbols through bitwise LLRs $L(d_q)$ and also to compute μ^d without an intermediate step. Thanks to Gray mapping, assuming that bits within a symbol are independent, we obtain

$$\mathbb{P}(x = \alpha) = \prod_{q=1}^Q \mathbb{P}(d_q = \phi_q^{-1}(\alpha)), \quad (14)$$

Constel.	Soft Estimates	
QPSK	$R(\mu^d) = p_1/\sqrt{2}$	$I(\mu^d) = p_2/\sqrt{2}$
8-PSK	$R(\mu^d) = (b_8 + a_8 p_1)p_2$	$I(\mu^d) = (b_8 - a_8 p_1)p_3$
16-QAM	$R(\mu^d) = (2 - p_2)p_4/\sqrt{10}$	$I(\mu^d) = (2 - p_1)p_3/\sqrt{10}$
Params.	$a_8 = \sqrt{(2 - \sqrt{2})/8}$, $b_8 = \sqrt{(2 + \sqrt{2})/8}$	

Table IV: Bitwise soft mapping expressions.

where $\phi_q^{-1}(\cdot)$ yields the q^{th} bit of $\alpha \in X$. In addition, as $\mathbb{P}(d_q = b) = (1 + (1 - 2b)p_q)/2$, where $p_q = \tanh(L(d_q)/2)$, one can exploit the geometry of the constellations with respect to real and imaginary parts and the labeling, to derive expressions for $\mu_k^{d(s)}$ as a function of soft bits p_q . Note that, in our case, LLRs for soft mapping are extrinsic $L(d_q) = L_e(d_q)$. Nevertheless, this approach can be readily generalized to a turbo-equalizer if a priori LLRs $L_a(d_q)$ from a soft output decoder are available with $L(d_q) = L_e(d_q) + L_a(d_q)$.

Such soft mapping techniques have been previously applied in [12] and [3] for APP-based and EP-based soft feedback, respectively. However, in this study, these formulas are only required for the mean of soft APP estimates, as the EP-based variance is handled through the tabulation technique of [5], with C_{EP} as stated earlier in Section III-A.

In addition, for the mean estimates, the computation of the hyperbolic tangent could be further simplified, by a piece-wise linear approximation, where all the slope and bias coefficients are powers of two. This enables a more efficient fixed-point implementation, as expressed below:

$$\tanh(x) = \begin{cases} x, & |x| < 0.5, \\ 0.5x + 0.25\text{sign}(x), & 0.5 \leq |x| < 1.0, \\ 0.25x + 0.5\text{sign}(x), & 1.0 \leq |x| < 2.0, \\ \text{sign}(x), & \text{otherwise.} \end{cases} \quad (15)$$

The complete expressions of soft estimates for constellations of interest are provided in Table IV. This concludes the algorithmic simplifications in soft mapping and demapping, and the resulting algorithmic complexity is given in Table I.

IV. FIXED-POINT CONVERSION ANALYSIS

Fixed-point conversion of the soft mapping/demapping algorithms was done using Fxpmath [13], a Python library for fractional fixed-point (base 2) arithmetic and binary manipulation with Numpy [14] compatibility. The focus of the conversion was on the calculations for bitwise max-log MAP demapper, bitwise soft mapper, and EP-based soft estimates (see Fig. 3), to facilitate the soft mapper/demapper architecture design.

For each variable of the different functions, we determined whether the variable is signed ($Q_S = 0$ or 1), the number of integer bits Q_I , and the number of fractional bits Q_F . The number of integer bits was determined by analyzing the maximum absolute value of the variable while operating in different Signal-to-Noise Ratios (SNRs) and scenarios. Then, an empirical approach was applied thanks to the py-AFF3CT environment. Indeed, this toolbox enables to rapidly estimate if reducing the number of bits would impact the Bit Error Rate (BER). A similar process was carried out for the fractional bits,

comparing the impact on BER of different sizes of fractional parts to achieve the minimum size with negligible loss. The total bit size of a variable is given by $Q_T = Q_S + Q_I + Q_F$.

As an example, consider the equalized symbol estimates $x_k^{e(s)}$, which are used in the simplified soft demapping (Sect. III-B). For the case of the Proakis-C channel with AWGN for QPSK, this variable has a maximum value of around 6.3 at 0dB, 3 at 10dB, and 2.2 at 20dB. Therefore, the performances were compared for the cases of having many bits for the fractional part Q_F (16 bits) while having 3, 2, 1, and 0 bits for the integer part Q_I .

The tests showed that with $Q_I = 0$, a loss of around 0.5dB at BER 10^{-3} is introduced. For the other values, there is negligible loss when using 1 integer bit compared to 2 and 3. This is due to noise amplitude having a more important range than the normalized signals at low SNRs. As for the fractional part, for QPSK, there is not a clear loss introduced with 3 bits. However, for 8-PSK, the use of only 3 fractional bits introduces a loss of around 1dB at BER 10^{-3} . With $Q_F = 4$, there is a smaller but still perceptible loss of around 0.1dB.

Considering these empirical observations, 2 bits were allocated for the integer part and 5 bits for the fractional part, as a safe margin for other channels and scenarios, and 1 bit for the sign. In the end, $Q_T = 8$ bits were assigned to the representation of the symbol estimates. The sizes of all the other variables were chosen with a similar process. All the named variables were successfully converted to $Q_T = 8$, while some internal calculations need up to 10 bits.

The performances in terms of Bit Error Rate (BER) for the original algorithm, the simplified algorithm, and its fixed-point version are shown in Fig. 4. The examined channel was the challenging Proakis-C. We focused on six different Modulation and Coding Schemes (MCS): the three presented constellations, using the LTE turbo code and rate matching with code rates 1/2 and 3/4. All the simulations were done considering one self-iteration ($S = 1$). The standard linear MMSE equalizer performance (given for $S = 0$) is provided for reference. For all cases, the fixed-point version performs very similarly to the simplified floating-point one. For Proakis-C MCS 2, 5, and 6, the original algorithm performs significantly worse than the simplified version at high SNR. In fact, bad interference patterns can make some observations close to wrong constellation points. In such situations, the original EP receiver generates an over-optimistic EP variance, and the EP feedback will be considered as correct while it is not. On the other hand, the simplified receiver calculates the EP variance independently of (possibly wrong) observations, through the C_{EP} LUT. This generates a more conservative feedback, thus avoiding the BER degradations.

As for the small gain of the fixed-point version, this observed behavior can be attributed to the inherent quantization noise introduced by the fixed-point representation. Interestingly, this noise can induce perturbations that effectively reduce the occurrence of unfavorable interference patterns, thereby enhancing the robustness of the algorithm in challenging scenarios.

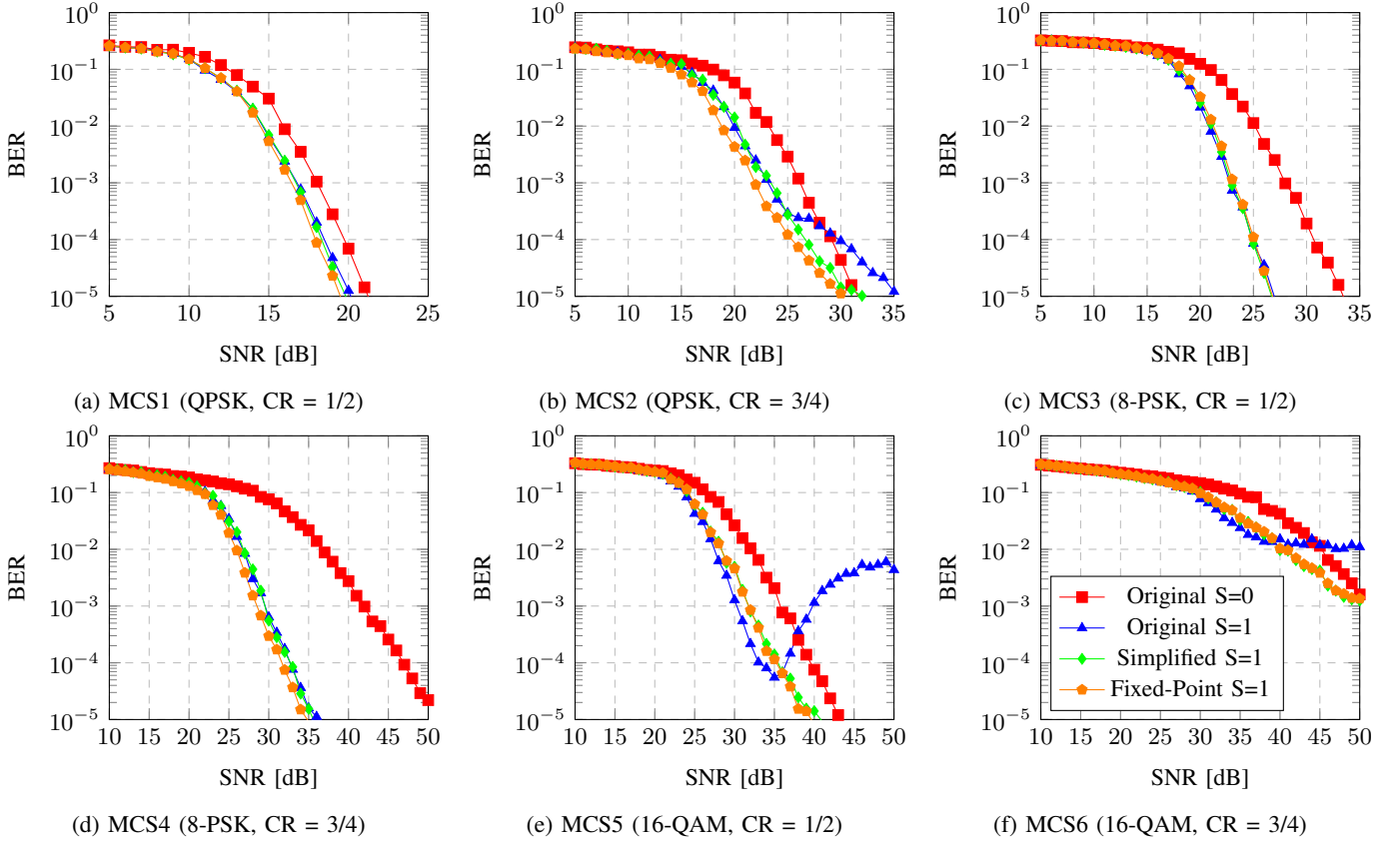


Fig. 4: Impact in terms of performance of simplification and fixed-point conversion.

V. FPGA IMPLEMENTATION AND PROTOTYPING

A. Experimental Setup

The experimental setup employs a Hardware in the Loop (HIL) configuration, involving a computer and a PYNQ Z2 board [15]. The computer runs py-AFF3CT, a Python wrapper for the Forward Error Correction Toolbox AFF3CT. The PYNQ Z2 board is a prototyping board based on the Xilinx Zynq System on Chip (SoC) with an ARM processor and an FPGA ZYNQ XC7Z020-1CLG400C. In our experimental setup, the board is connected to the computer via an Ethernet cable. The board's ARM processor forwards the data to the FPGA device via a Direct Memory Access (DMA). Moreover, it facilitates the Ethernet connection between the computer and the SoC device, acting as a passthrough.

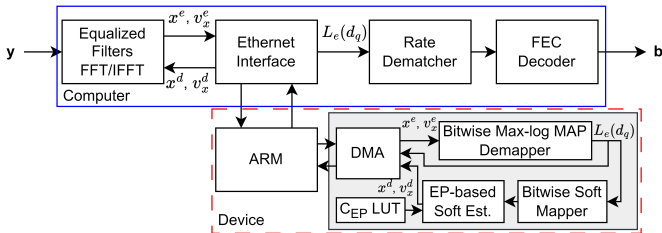


Fig. 5: Simplified EP-based FD-SILE FPGA and HIL Block Diagram.

Fig. 5 shows the block diagram of simplified EP-based FD-SILE with the HIL configuration. Within the FPGA, the three parts of the algorithm with analytical simplifications have been implemented: bitwise max-log MAP demapper (eq. (11) and Table II), bitwise soft mapper (Table IV) and LUT-based variance parameter (C_{EP} in section III-A), and EP-based soft estimates (eq. (8-9)). These implemented blocks of the algorithm perform essential computation for the Expectation Propagation-based receiver and are the focus of the presented work. The remaining parts of the receiver are executed thanks to AFF3CT on the associated computer. These software blocks encompass filtering, equalization, FFT and IFFT operations, rate dematching, and Forward Error Correction (FEC) decoding. This HIL setup is used to obtain the previously discussed fixed-point simulation results.

B. FPGA Implementation Results

Table V shows the total available and allocated FPGA resources for each of the three constellations that are considered in this article: QPSK, 8-PSK, and 16-QAM. The first row for each constellation is for the implementation of only FD-SILE without the HIL configuration, while the second row is for the FD-SILE with the HIL configuration, including the data exchanges to the ZYNQ Processing System and the DMA. The implemented architectures use a data width of 32 bits for the DMA connection, enabling to exchange two symbols with 8-bit real and imaginary parts.

Given the low resource usage for the analytical blocks, several calculations can be carried out in parallel in the proposed architectures. For QPSK and 16-QAM, the architectures are composed of four independent bitwise max-log MAP demapper blocks, as the real and imaginary parts are independent, and generates respectively one and two LLRs for each value. For 8-PSK, the proposed architecture processes two values (one symbol) to produce three LLRs, using two demapper blocks in parallel for the four values.

The process for the bitwise soft mapper is the inverse of this, using two LLRs per symbol for the QPSK, three for 8-PSK, and four for 16-QAM. The calculation of the EP-based soft estimates is the same for the three constellations, using four of these blocks in parallel.

XC7Z020-1CLG400C	LUTs		Flip-Flops		BRAMs		Critical Path (ns)	
	N ^o	%	N ^o	%	N ^o	%		
Resources	53200		106400		140		-	
QPSK	A	1035	1.95	198	0.19	0.5	0.36	9.418
	B	4204	7.90	5373	5.05	2.5	1.79	
8-PSK	A	1805	3.39	346	0.33	0.5	0.36	9.648
	B	4968	9.34	5521	5.19	2.5	1.79	
16-QAM	A	1448	2.72	340	0.32	0.5	0.36	9.738
	B	4654	8.75	5515	5.18	2.5	1.79	

A: FD-SILE without HIL configuration.

B: FD-SILE with HIL configuration.

Table V: FPGA Resources Table.

The FPGA implementation demonstrates efficient resource usage, as shown in Table V, with very limited occupation in terms of Look-Up Tables (LUTs) and Flip-Flops (FFs). The implementation of the analytical blocks consumes fewer resources than other resources that are necessary to communicate with the ARM processor. It is important to note that the implementation with the highest resource usage is the one for 8-PSK mapping. Indeed, this mapping uses a LUT-aided semi-analytical implementation instead of an analytical implementation. One can note that no DSP resources are assigned in the FPGA. This is due to the fact that all the arithmetic operations are applied on data represented by a limited number of bits, thanks to the proposed fixed-point analysis. Furthermore, all implementations achieve an execution frequency of 100MHz, given the critical paths below 10 ns.

VI. CONCLUSION

This paper has presented a comprehensive study and, to the best of our knowledge, the first hardware implementation of an EP-based FD-SILE for QPSK, 8-PSK, and 16-QAM constellations on an FPGA platform.

The results demonstrated that the fixed-point version performed comparably to the floating-point one, even helping to mitigate the negative impacts of bad interference patterns in the challenging Proakis-C test channel. The resource utilization for the analytical blocks was low, allowing the remaining resources to be used for other blocks of the receiver if necessary.

In future works, there are several promising possibilities. One such direction is the implementation of a flexible receiver

that can adapt to the mapping constellation. Another possibility is the integration of turbo iterations into the receiver design, which could further enhance its performance.

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