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Cleiton Marques, Frédéric Wrobel, Ygor Aguiar, Alain Michez, Frédéric Saigné, et al.. Evaluation of a Simplified Modeling Approach for SEE Cross-Section Prediction: A Case Study of SEU on 6T SRAM Cells. *Electronics*, 2024, 13 (10), pp.1954. 10.3390/electronics13101954. hal-04607285

HAL Id: hal-04607285

<https://hal.science/hal-04607285v1>

Submitted on 6 Nov 2024

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Article

Evaluation of a Simplified Modeling Approach for SEE Cross-Section Prediction: A Case Study of SEU on 6T SRAM Cells

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Abstract: Electrical models play a crucial role in assessing the radiation sensitivity of devices. However, since they are usually not provided for end users, it is essential to have alternative modeling approaches to optimize circuit design before irradiation tests, and to support the understanding of post-irradiation data. This work proposes a novel simplified methodology to evaluate the single-event effects (SEEs) cross-section. To validate the proposed approach, we consider the 6T SRAM cell a case study in four technological nodes. The modeling considers layout features and the doping profile, presenting ways to estimate unknown parameters. The accuracy and limitations are determined by comparing our simulations with actual experimental data. The results demonstrated a strong correlation with irradiation data, without requiring any fitting of the simulation results or access to process design kit (PDK) data. This proves that our approach is a reliable method for calculating the single-event upset (SEU) cross-section for heavy-ion irradiation.

Keywords: SRAM; single-event upset; cross-section; heavy ions; modeling



Citation: Marques, C.M.; Wrobel, F.; Aguiar, Y.Q.; Michez, A.; Saigné, F.; Boch, J.; Dilillo, L.; García Alía, R.

Evaluation of a Simplified Modeling Approach for SEE Cross-Section Prediction: A Case Study of SEU on 6T SRAM Cells. *Electronics* **2024**, *13*, 1954. <https://doi.org/10.3390/electronics13101954>

Academic Editors: Jérémy Postel-Pellerin and Vincenzo Della Marca

Received: 12 April 2024

Revised: 10 May 2024

Accepted: 15 May 2024

Published: 16 May 2024



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1. Introduction

As electronics technologies continue to shrink, they become more sensitive to faults due to external interactions such as temperature variations, noise, and especially radiation effects [1]. Electronic memories represent crucial components in systems on chips (SoCs), occupying a large part of an SoC area, reaching up to 90% of the total surface [2]. In particular, static random access memory (SRAM), among the best performing solid-state memories, is typically manufactured at the limits of the technology node, making it prone to single-event upsets (SEUs) [3]. For this reason, the occurrence of radiation faults in memory cells has been gaining increasing prominence [4–6]. However, evaluating the radiation effects and the robustness of SRAM cells directly with a radiation test in a particle accelerator facility is logistically complex and costly. Therefore, a preliminary assessment of the expected effects of radiation on the device can be carried out using approximation methods during the design phase and after production. These methods consist of the use of electrical models, circuit simulations, and tools dedicated to the emulation of radiation effects. In this sense, predictive and post-irradiation analysis is a crucial step, not only for sensitive estimation, but also for a better understanding of the fault mechanisms that operate at the circuit and transistor level.

Over the past few decades, several simulation tools have been developed with the objective of analyzing single-event effects (SEE). Monte Carlo (MC) simulations are being extensively used for this purpose [7–12]. Notable examples of MC simulation tools include SPENVIS [7], FLUKA [8], and G4SEE [9]. While FLUKA is a general-purpose MC tool, G4SEE focuses on SEE, and SPENVIS focuses on spacecraft dose calculation. There are also

TIARA [10], MRED [11], and MUSCA SEP3 [12], which are private-domain frameworks for SEE analysis. Most of these tools depend on the technology's process design kit (PDK) information. The PDK gathers a comprehensive set of files, libraries, and models that encapsulate the process parameters, electrical characteristics, and design (layout) rules related to a specific manufacturing process. These parameters provide a framework for simulating the behavior of electronic circuits, allowing engineers and researchers to predict their performance under various operational conditions. However, obtaining these parameters from manufacturers is generally not straightforward [13]. Consequently, when these parameters are inaccessible, simulations that are based on scarce technological information lead to results that may fail to meet expectations. Furthermore, even when these data are available, depending on the type of analysis, the tools need to solve complex transport and Poisson equations, extending the simulation time.

In this context, this work provides a novel simplified methodology that overcomes the aforementioned drawbacks related to the lack of technological information and simulation complexity, and predicts the SEE cross-section. This methodology is included in the PredicSEE tool, developed in our laboratory at the University of Montpellier. In this work, the tool uses Monte Carlo simulations to predict the SEU cross-section of a 6T SRAM cell under heavy-ion irradiation for 90 nm, 65 nm, 45 nm, and 32 nm planar-bulk CMOS technologies. We evaluate this multi-physics methodology in terms of accuracy through a comparison with experimental data and identify its limitations.

2. Circuit Modeling Background

Circuit-level modeling is crucial in the design and analysis of electronic systems. It enables the prediction and verification of circuit performance before fabrication, refining the production process. In SEE analysis, circuit modeling plays a vital role in understanding the impact of radiation effects on electronics, helping to develop robust designs and shielding techniques, and evaluating particle–matter interaction to ensure the proper function of systems in different environments, such as aerospace and accelerators [14,15].

One of the main drawbacks of circuit modeling is the difficulty of accurately predicting the behavior of circuits under radiation effects, as the models may only capture some of the complexities and nuances in particle interactions. Additionally, some physics-based SEE models are complex, hence extending the CPU time. While circuit-level modeling is valuable for predictive and post-irradiation analysis, it is essential to recognize its limitations and consider alternative or complementary approaches to ensure a comprehensive analysis of radiation effects on electronic devices and circuits.

2.1. Electrical Modeling

An electrical model represents or describes a circuit that captures its essential behavior, which may be conceptual or analytical, depending on the aspects under consideration. In this context, the Simulation Program with Integrated Circuit Emphasis (SPICE) tool is a cornerstone in electronic circuit modeling. SPICE employs mathematical models to represent the behavior of electronic components, capturing the complex interplay of electrical properties and enabling a detailed analysis of circuit performance under various conditions. However, accurately predicting radiation effects requires careful consideration of material composition and particle–matter interactions, and involves challenges related to the simulation methodology and experimental validation [9,16,17]. The number of parameters associated with a SPICE model can vary widely based on the component's complexity and specificity. A simple transistor can require hundreds of parameters. This complexity increases when we consider a complete circuit. An alternative solution is addressing this issue using a simplified approach without a detailed knowledge of the target technology.

The simplified model of transistors is based on the drain–source current (I_{DS}) versus the drain–source voltage (V_{DS}) for different gate–source voltages (V_{GS}), replacing the structure of the transistor with a current source [18]. To calculate the I_{DS} , we applied the

simplest first-order model for the MOSFET transistor, which gives three major regions of operation: subthreshold, triode, and saturation. In this model the current through an OFF state transistor is 0. When the transistor turns ON, the gate attracts carriers to create the channel. The carriers drift from source to drain at a rate proportional to the electric field between these regions. The I_{DS} is a function of the gate capacitance (C_{ox}), channel width (W), channel length (L), carrier mobility (μ_n for electrons and μ_p for holes), threshold voltage (V_T), channel length modulation (λ) and supply voltage (V_{dd}). The C_{ox} can be deduced from the oxide thickness (T_{ox}). For carrier mobility, normally, theoretical values based on the doping concentration of the technology are used. Considering the above parameters, the I_{DS} can be approximated via the following analytical expressions [18]:

- Subthreshold if $V_{GS} < V_T$:

$$I_{DS}(V_{GS}, V_{DS}) = 0 \quad (1)$$

- Triode if $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$:

$$I_{DS}(V_{GS}, V_{DS}) = \mu C_{OX} \left(\frac{W}{L} \right) (1 + \lambda V_{DS}) \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \quad (2)$$

- Subthreshold if $V_{GS} < V_T$:

$$I_{DS}(V_{GS}, V_{DS}) = \frac{\mu C_{OX}}{2} \left(\frac{W}{L} \right) (1 + \lambda V_{DS}) (V_{GS} - V_T)^2 \quad (3)$$

The parameters at the base of these equations are known, at least in terms of their average values, for each technology node, as shown in Table 1. These parameters represent the minimum required to start our proposed simulation methodology. The exact values of these parameters may not be precisely known for specific devices, but we will show that it is sufficient to feed our simulation tool with just the order of magnitude of the exact values.

Table 1. Simplified model; basic parameters for different technologies [18].

Node (nm)	Q_{crit} (fC)	T_{ox} (nm)	W/L (nm/nm)	V_T (V)	V_{dd} (V)
90	1.2	2.0	180/90	0.40	1.0
65	0.8	1.8	120/65	0.42	1.2
45	0.6	1.8	90/45	0.46	1.0
32	0.4	1.6	64/32	0.63	1.0

2.2. SEE Triggering Models

In SEE modeling, identifying a fault is challenging due to complex radiation interactions with electronics, such as ionization physics, charge collection processes, and particle–matter interactions [17]. The Monte Carlo approach is a widely used method for SEE analysis, where the characteristics of each impinging particle are known, and a given criterion can be applied to verify single- or multi-event triggering. One of the most common methods used in Monte Carlo simulations is the rectangular parallelepiped (RPP) [17,19,20], which characterizes the sensitive volume of the circuit. This method simplifies modeling by creating a box-like shape in a part of the circuit, where only radiation interactions inside this volume and with a deposited energy greater than the critical energy of the device are considered. While the RPP provides a simplified geometric representation, it may not always accurately correspond to the actual physical structure of complex devices.

A more physical criterion, the diffusion–collection model, estimates the shape of the transient current generated in the drain of the sensitive transistor. In this method, the collected charge is modeled considering two mechanisms: drift and diffusion [16,21]. The drift is where charge carriers move primarily due to the electric field generated by the voltage applied to the transistor gate. On the other hand, diffusion represents the carriers

that move due to the carrier concentration in the semiconductor material, creating a flow from regions of higher concentrations to regions of lower concentrations.

Considering spherical diffusion, in Figure 1a, we present the scheme of the carriers arriving to the OFF-state drain at a given time, t , and a given distance, r , from the ion generation point. To calculate the total charge, $n(t)$, arriving to the drain, the diffusion-collection model breaks down the ion track into n -segments, dl , determining the average linear energy transfer (LET) value for each segment, as shown in Figure 1b. In this sense, the electron-hole pairs' density reaching a specific part of the sensitive surface for each segment can be calculated via the following:

$$n(t) = \iiint LET(l) \frac{e^{-\frac{r^2}{4Dt}}}{(4\pi Dt)^{\frac{3}{2}}} dx dy dl \tag{4}$$

where D is the ambipolar diffusion constant.

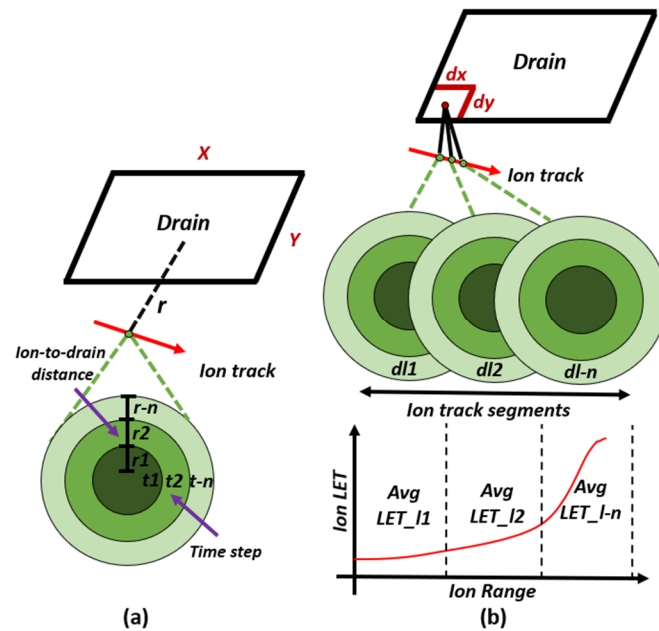


Figure 1. The diffusion-collection model: (a) the carriers arriving to the OFF-state drain at a given time, t , and a given distance, r , of the ion generation point; (b) segmentation of the ion track and the drain surface.

Subsequently, due to the charge collection, a parasitic current will appear in the drain. The drain current, $I_d(t)$, can then be approximated as follows:

$$I_d(t) = \int \int_{drain} qn(t)v dS \tag{5}$$

where q is the elementary charge constant, v is the average velocity of the collected carriers, and dS is the drain surface element.

For ion tracks crossing the sensitive region, a specific LET value is identified as a threshold value able to trigger a fault. This criterion has been validated in [16].

Once the transient current is calculated with Equations (4) and (5), it may either be used as an input for SPICE simulations or dealt with using a criterion such as the I_{MAX} - T_{MAX} criterion [15,16]. In the first case, the computational time could be high since a new SPICE simulation has to be run for each particle belonging to the pool of impinging particles considered in the simulation. For the second case, the I_{MAX} - T_{MAX} refers to the maximum transient current (I_{MAX}) and the time needed to reach the maximum transient current (T_{MAX}), which is simulated with SPICE or TCAD prior to MC calculations [18].

Consequently, these approaches may not be satisfactory when a realistic PDK model is not available.

3. The Proposed Methodology

Considering all the pros and cons of the methodologies mentioned above, we propose applying the parasitic current calculated by the diffusion–collection model with the simplest first-order CMOS model, for which the electrical solution can be analytically calculated. The diffusion–collection model is more accurate for predicting SEE in electronics than the RPP model. However, it has some drawbacks. The diffusion–collection model can lead to higher computational time and a need for more detailed information at the layout level. The impact on the number of resources required to run the modeling can be mitigated using a simplified transistor model. The layout information, when not available in detail from the manufacturer, can be generally found in the literature, as was the case in this work, although the literature may not have precise details either.

Differently from previous works [17,18], we propose fitting the parameters of Equations (1)–(3) using basic SPICE simulations to obtain simplified transistor characteristics in a more realistic way and without the need for the end user to have prior access to the PDK technology. In our approach, we use an open-access predictive technology model (PTM) [22] to characterize the behavior of the NMOS and PMOS transistors separately. The PTM bridges the process/material development and the circuit simulation through a compact device model. This model aims to evaluate the potential and limitations of new technologies and to support early design analysis. The PTM includes a set of information related to the technology process and physical parameters. Its values are empirically fitted from published data available in the literature. This methodology was developed at Berkeley University using BSIM4 or other standard formats as a basis [22].

We use a simple SPICE simulation to obtain the I_{DS} vs. V_{DS} curves for different values of V_{GS} . Using these curves as a base, it is possible to extract the approximate values for the parameters of Equations (1)–(3). Thus, the behavior of the simplified transistors would be much closer to the one provided by actual SPICE models. This simplification leads to a reduction in simulation time, since all subsequent analyses use analytical equations of the simplified model. The SPICE simulations are run only at the beginning of the execution to extract the simplified model parameters. Figure 2 shows an example of the I_{DS} vs. V_{DS} curves calculated using this simplified approach for a 65 nm NMOS transistor.

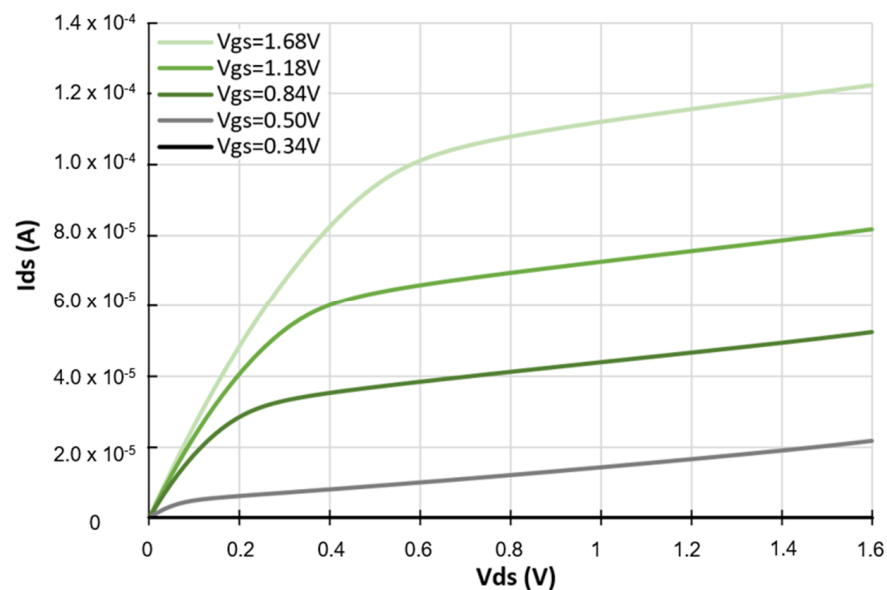


Figure 2. Example of the I_{DS} vs. V_{DS} curves for different V_{GS} values of the simplified NMOS transistor with $W/L = 1$.

Considering the case of a classic six-transistor (6T) SRAM cell, depicted in Figure 3, the voltage variation of nodes Q and Qb can be expressed as a function of six currents, $I_{d_n1}(t)$, $I_{d_n3}(t)$, $I_{d_p1}(t)$, $I_{d_n2}(t)$, $I_{d_n4}(t)$, and $I_{d_p2}(t)$, calculated with the diffusion–collection model, and six currents, $I_{n1}(V_{GS}, V_{DS})$, $I_{n2}(V_{GS}, V_{DS})$, $I_{n3}(V_{GS}, V_{DS})$, $I_{n4}(V_{GS}, V_{DS})$, $I_{p1}(V_{GS}, V_{DS})$, and $I_{p2}(V_{GS}, V_{DS})$, corresponding to the transistors responses estimated with the simplified transistor model.

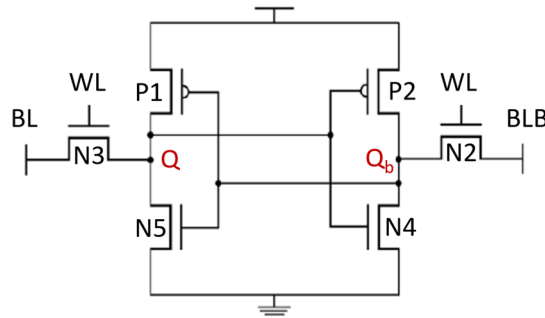


Figure 3. Standard 6T SRAM electrical diagram.

Differently from [17,18], in our approach, we consider all six transistors of the SRAM cell and not just the four transistors of the two-inverter loop in order to enhance the simulation accuracy. Additionally, for the same purpose, we take into account the layout of the cell. Equations (6) and (7) represent the voltage for nodes Q and Qb . The polarity of the input currents depends on the value stored in the cell.

$$C_N \frac{d(V_Q)}{dt} = I_{d_n1}(t) + I_{d_n3}(t) + I_{d_p1}(t) + I_{n1}(V_{GS}, V_{DS}) + I_{n3}(V_{GS}, V_{DS}) + I_{p1}(V_{GS}, V_{DS}) \quad (6)$$

$$C_N \frac{d(V_{Qb})}{dt} = I_{d_n2}(t) + I_{d_n4}(t) + I_{d_p2}(t) + I_{n2}(V_{GS}, V_{DS}) + I_{n4}(V_{GS}, V_{DS}) + I_{p2}(V_{GS}, V_{DS}) \quad (7)$$

The solution of this set of equations yields the transient voltage from the transient current induced by a particle and, consequently, the state of the circuit after the event. Based on these assumptions, the order of magnitude of the SEE cross-section of a given SRAM device can be computed. This proposed methodology is included in the PredicSEE tool. PredicSEE has been developed in our lab at the University of Montpellier for decades. The previous published version was MC-Oracle [17]. Differently from MC-Oracle, PredicSEE provides a straightforward interface with input parameters familiar to the end users. Moreover, PredicSEE varies the thickness of the depletion layer dynamically based on the potential at the node. In PredicSEE, the Monte Carlo simulations run to inject the selected particles randomly across the device area. The simulation ends when one of the stopping criteria is reached: Monte Carlo accuracy or the fluence of particles. To reduce the CPU time dependence, PredicSEE uses the DHORIN code [23] that provides a wide range of particle–matter interactions pre-calculated for protons and neutrons. For the ions, primary and secondary ion transport and their ionization are obtained through the SRIM [24]. Ions, neutrons, and protons can be considered, and their resulting ionization (direct and indirect) is simulated using the diffusion–collection model, simplifying the collection and transport of carriers after the interactions. Figure 4 displays a flowchart of the PredicSEE code.

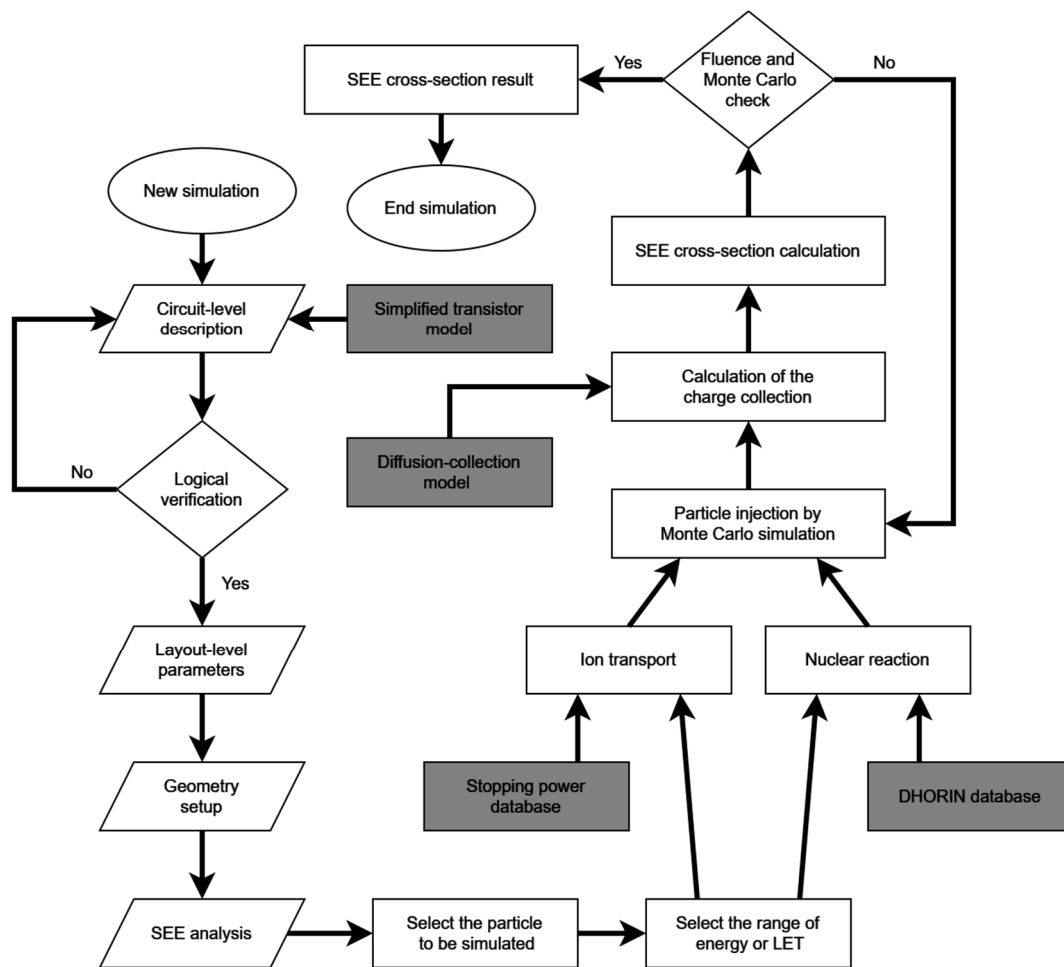


Figure 4. Simplified flowchart of PredicSEE code.

4. Simulation Setup

To validate the proposed methodology, we evaluated the 6T SRAM cell at four technological nodes: 90 nm, 65 nm, 45 nm, and 32 nm of planar bulk CMOS technology. Our analysis explores the heavy-ion cross-section, considering the beam orientation at a normal angle of 90° (the beam direction is perpendicular to the chip). The MC simulations were performed with a confidence margin of 95%. The results will be compared with experimental data.

4.1. Circuit-Level Description

The first simulation step consists of describing the circuit schematic to be evaluated. Using PredicSEE, we add the transistors, wire connections, voltage sources, signals, and node capacitances. After describing the circuit, we define the technology node through the available PTM reference. The SPICE model will be used to facilitate simplified modeling. Finally, it is necessary to define the size of the transistors by the width (W)/length (L) ratio. To choose and justify these parameters, it is important to understand how the SRAM circuit works. Access to the cell is enabled during write/read operations and is controlled by the wordline (WL) signal. The access transistors (N3-N4, in Figure 3) rule the connection between the bitlines (BL-BLB) and internal cell nodes (Q-Qb). The two PMOS (P1-P2) and two NMOS (N1-N2) transistors complete the feedback inverters.

In order to perform the write and read operations successfully, it is essential to size the transistors of the cell. For this purpose, the cell ratio (CR) is defined to improve the read operation, $CR = (W_{N1}/L_{N1})/(W_{N3}/L_{N3})$, and the pull-up ratio (PR) is defined to improve the write operation: $PR = (W_{P1}/L_{P1})/(W_{N3}/L_{N3})$ [25]. In this work, the design

choices are $CR = 1.5$ and $PR = 1.0$. The minimum W/L used for each technology follows an approximate ratio of 2. This size and ratio are based on standard choices to keep the cell area small, achieve good static and dynamic noise margins, and minimize the access times [25,26]. However, it is essential to note that different values can be used depending on the cell design requirements. The other common technology parameters have already been presented in Table 1. After describing the circuit, the tool performs logical characterization to confirm that there are no implementation problems, such as impossible outputs or circuit shortcuts.

4.2. Layout-Level Parameters

The next simulation phase is to define the layout parameters. PredicSEE automatically generates the 2D geometry of each transistor. Based on this, the user must arrange the transistors in a way to adhere the basic layout rules of the target technological node. The layout of commercial SRAM cells is rarely available, and different layouts can be used for the classic 6T cell. Depending on the structure of the cell, the array can have a good or a bad match with the address decoders, more or less of the metal layers needed for the cell layout, impact cell stability, and affect the bitline capacitance and thus access time [25,26]. Figure 5 shows three of the main layout options in the literature [25,27,28].

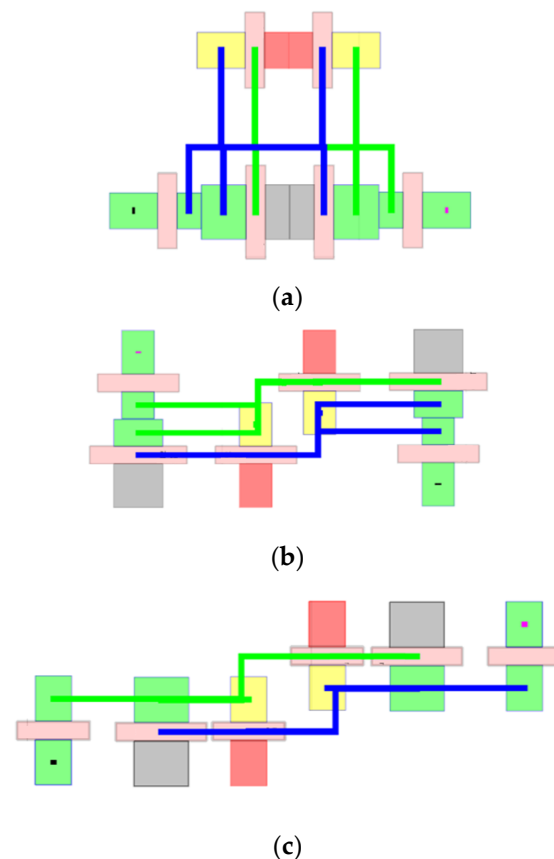


Figure 5. Three different layout designs that can be applied to the 6T SRAM cell: (a) “tall” design [27]; (b) “thin” design [25]; (c) “ultra-thin” design [28].

Figure 5a is compact, widely used until the 90 nm generation, and is compatible with 65 nm design rules [27]. In Figure 5b, the diffusion areas work vertically, while the polysilicon tracks are strictly horizontal. The cell is longer and “thin”, which reduces the critical capacitance related to the bitlines [25]. In Figure 5c, the cell is “ultra-thin”, with lower bitline capacitance, reducing the metal layers’ complexity, reducing the mismatch with the decoders, and adapting scaling/lithographic restrictions [28]. Due to the difficulty of finding information related to the layout used in actual commercial SRAM design, we

decided to use Figure 5b as a reference for our study. The layout rules adopted were obtained from the literature [27,29–31]. Furthermore, to complete the needed input data, it was necessary to determine the doping values for N+/P+ regions and the N/P wells since the doping profile significantly impacts the SEE impact. In this work, the doping profile was set in terms of the order of magnitude based on PTM values [22].

In addition to the design rules and the doping profile, an important parameter is the drain area. The diffusion–collection model requires this crucial input, which is generally not known precisely. However, considering a simple MOS structure, it is easy to notice that the width of the channel is also the width of the drain. Moreover, drawing rules generally determine the length of the drain as around $2.5\times$ the channel length [18].

4.3. SEE Analysis

SEE analysis consists of two stages: the first is to define the geometry setup, and the second is related to particle injection parameters. For the geometry, the layers of material that make up the device are very important for modeling the nuclear and ionizing interactions that occur in the path of the incident particle. As the composition of the BEOL is generally not known, the material composition was simplified considering the following layers: the 8 μm silicon dioxide (SiO_2) layer, the 20 μm bulk silicon (Si) layer, and the 3 μm borders around the DUT. Figure 6 shows a 3D visualization of the simulation, highlighting the material layers, the device under test (DUT) position, and the particle beam angle.

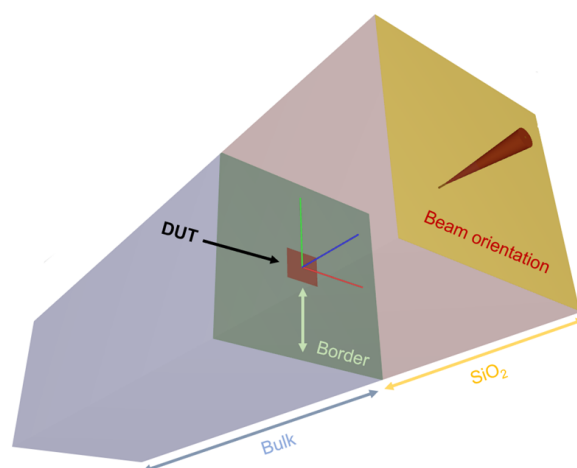


Figure 6. PredicSEE view of the simplified 3D structure used in the simulations. The BEOL is modeled with SiO_2 .

For particle injection, the simulation was performed using the Texas A&M Cyclotron Facility (TAMU) heavy ion 15 MeV/u database and the RADiation Effects Facility (RADEF) heavy ion 16.3-MeV/u database. The simulated fluence used was 1×10^{13} ions/ cm^2 , since we included low-LET ions in the analysis. For this low-LET range, a greater number of injections is necessary to be able to observe enough events. However, it is important to note that for high-LET conditions, the fluence will not reach this value, as the simulation will converge to MC accuracy first. During the simulation, the selected particles will be injected randomly inside the total area (layout area + borders area) according to the MC simulation. In this work, our simulation only considered the surface of one cell, not the complete array of multiple cells. Finally, the tool generates the SEE cross-section with a Weibull function fit.

5. Experimental Data vs. Simulation Results

In this section, the SEU cross-section results are compared with the experimental data obtained from the literature [27,32–34]. It is important to note that no fitting of the results was performed. The simulation setup followed the same procedure as that for experimental irradiation, using the same incidence angle and supply voltage. The simulation of

one SRAM cell applying 12 different LET values (15 MeV/u TAMU cocktail) in parallel took approximately 40 h using a conventional laptop. The ions below $10 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ demanded a significant part of this effort due to the infrequent occurrence of events. Conversely, ions with LET values exceeding this range required only about 20 h of execution, as the simulation converged more quickly to the desired Monte Carlo accuracy. It is worth noting that the runtime can increase to a couple of days in some methodologies where complete SPICE modeling is adopted [12,15,17]. This increase in the runtime can limit the evaluation of more complex circuit structures.

Results for the 90 nm 6T SRAM are shown in Figure 7. Despite the lack of complete information from the transistor technology, the simulation is in good agreement with the experimental data, with an overall discrepancy of $\sim 20\%$. However, in the region of saturation of the cross-section curve, the simulation results underestimate the values by about $\sim 50\%$, which can be considered rather acceptable, especially knowing the amount of approximations carried out. Experimental data demonstrate that the SEU cross-section is strongly dependent on the circuit design [35]. This discrepancy in the saturation region can be associated with the estimated layout structure, which may not contain the correct dimensions for the 90 nm technological node used in [32]. This behavior is further discussed in Section 6 of this work.

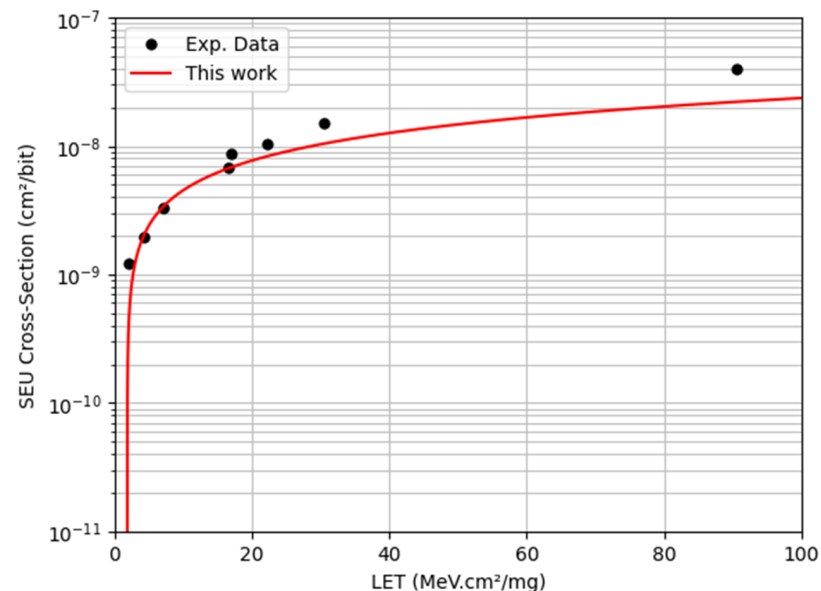


Figure 7. Heavy-ion SEU cross-section for 90 nm SRAM. Experimental data taken from [32].

For the 65 nm SRAM, a better agreement with the experimental data was found, even in the saturation region, with a difference of less than 15%. The results are available in Figure 8. In this case, the worst discrepancy was found in the LET range close to the threshold LET (LET_{TH}) region in the curve. We did not observe upsets for LETs below $1.3 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, which would have caused the Weibull curve to be underestimated for these points. This may have been related to the value used for SiO_2 thickness in the back-end-of-the-line (BEOL) layer and the doping profile, which was estimated with the precision of the order of magnitude. Both parameters are related to LET, as if LET is lower, fewer events occur, which can impact the accuracy of the simulation in the lower LET ranges.

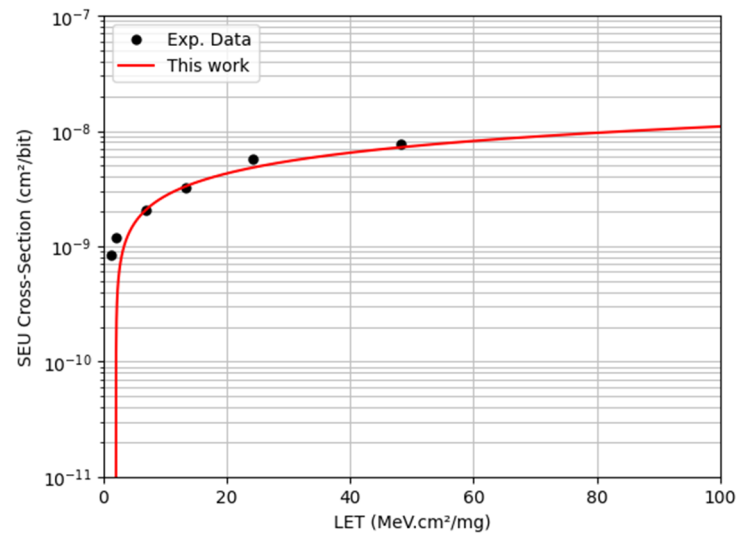


Figure 8. Heavy-ion SEU cross-section for 65 nm SRAM. Experimental data taken from [27].

The 45 nm SRAM showed even better agreement than that observed for the larger technology nodes. The results are shown in Figure 9. The prediction discrepancy was $\sim 10\%$ when we did not consider the two points near the LET_{TH} range. For these two points, the simulations showed an overestimation compared with the experimental data. This difference is related to the same reasons highlighted for the 65 nm process. However, for 45 nm, the parameter approximation was better.

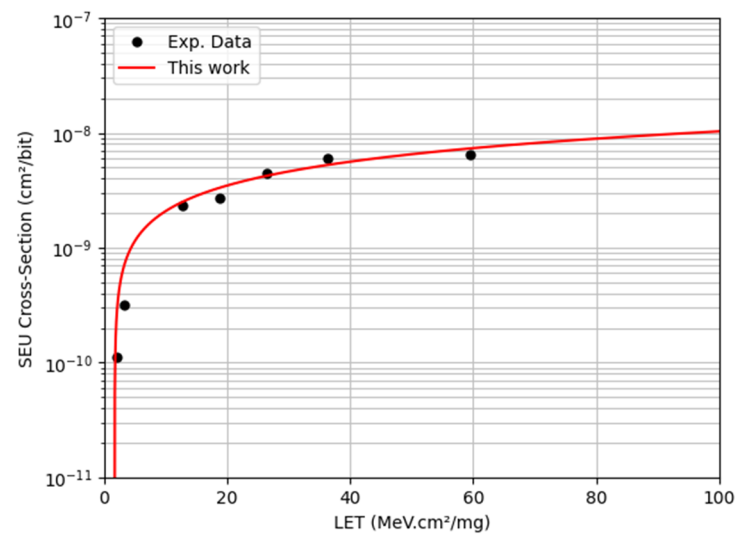


Figure 9. Heavy-ion SEU cross-section for 45 nm SRAM. Experimental data taken from [33].

A similar trend was observed for the 32 nm SRAM cell, where the simulation accuracy reduced with the reduction in particle LET, as shown in Figure 10. The simulation results are in the same order of magnitude as the reference points but without an acceptable level of agreement. The predictions in the LET range of 1–20 MeV.cm²/mg show average discrepancy by a factor of $\sim 3\times$. However, we obtained a result with only a $\sim 10\%$ difference in the saturation region. For this technological node, neither circuit nor layout information was found in abundance in the literature. Furthermore, most experimental cross-section data available are in arbitrary units, which made the comparison difficult.

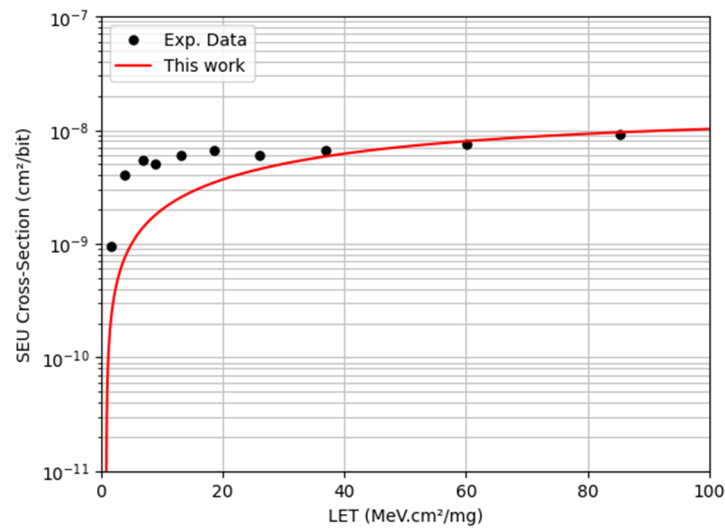


Figure 10. Heavy-ion SEU cross-section for 32 nm SRAM. Experimental data taken from [34].

Another critical point is investigating the model's viability for different supply voltage values. For this analysis, we reduced the supply voltage gradually from the nominal value (1.2 V, as shown in Table 1) to sub-threshold values. Given the availability of experimental data, we decided to evaluate the 6T cell using 65 nm technology. Figure 11 shows the cross-section for five different voltage values from simulation and experimental data.

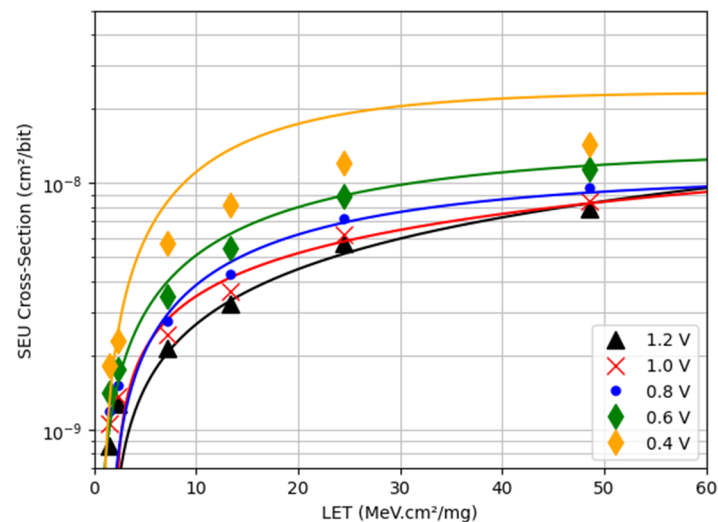


Figure 11. Heavy-ion SEU cross-section for 65nm SRAM considering the voltage scaling situation. Experimental data taken from [27].

The simplified models proved to be excellent options for predicting the cross-section at medium–high LET values for the supply voltage over the transistor threshold voltage (0.42 V, as shown in Table 1). However, the simulation accuracy dropped slightly in the LET_{TH} region. As discussed above, this behavior can be explained by the lack of information regarding the BEOL thickness and doping profile. Also, the low number of faults found at a low LET affected the LET_{TH} calculation. The critical point of this analysis is in the sub-threshold voltage (0.4 V), where the simulations presented an overestimation in relation to the experimental data. This behavior is related to a limitation of the model to operate at the sub-threshold region in an ideal way and needs further investigation.

6. Impact of the Input Parameters

The proposed methodology proved to be an excellent option for predicting the behavior at a medium–high LET above the transistor threshold voltage. The results show good agreement with the experimental data, showing that we can accurately predict the SEU mechanism. However, even if fitting had not been performed, discussing the impact of input parameters on the simulation result is essential. The number of parameters was reduced and simplified in each modeling phase, using available or approximate values based on the literature. The objective of the proposed methodology was to estimate the cross-section in order of magnitude, even without access to all parameters and characteristics of the device. However, even when available, the device characteristics vary depending on the manufacturer and application. Figure 12 compares the SEU cross-section calculated for the 6T SRAM with 65 nm bulk CMOS using the input parameters proposed in this work as golden results (standard simulations) with variations in some specific parameters.

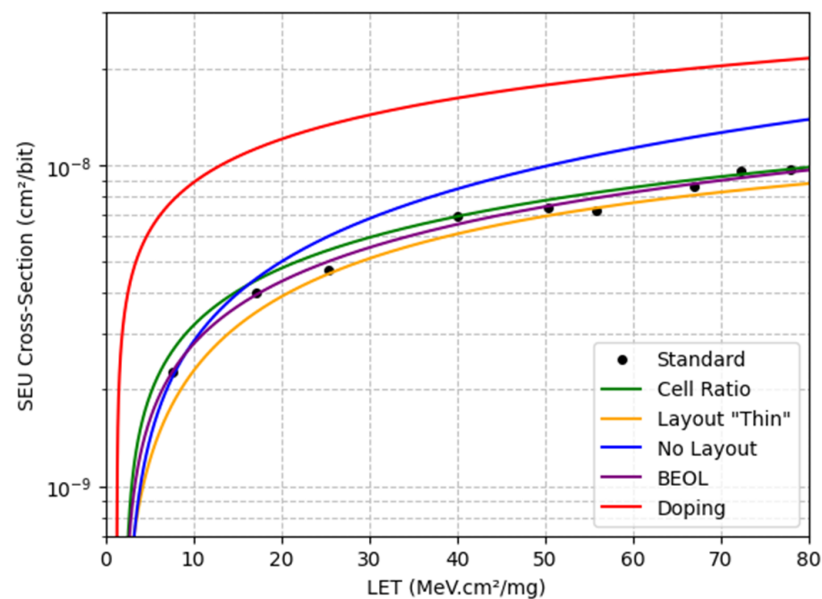


Figure 12. Heavy-ion SEU cross-section for 65 nm SRAM with variations in different input parameters. The standard plot is the golden result obtained using the following input parameters: CR = 1.5; layout = “Tall”; BEOL = 8 μm ; and doping = 10^{18} atoms/ cm^3 . For the other curves, we only show one of the parameters and indicate the simulation response. The cell ratio curve applies CR = 2.0. The layout curve uses the “Thin” layout approach. The no-layout curve does not follow a layout structure, only spacing the transistors apart from each other. The BEOL curve applies a BEOL thickness of 3 μm . The doping curve uses N-P WELL = 10^{17} atoms/ cm^3 .

Considering the CR of the SRAM cell, this ratio typically varies between 1.0 and 2.5 in bulk CMOS technology, depending on the application [25]. Figure 12 compares CR = 1.5 in the standard simulation with the “Cell Ratio” curve that uses CR = 2.0. When we compare these results, we observe that as the CR increases, the cross-section also increases. However, the variation between the results is still at a reasonable level. This information is vital for the end user, who can safely use these CR ranges if data are unavailable.

The layout of the SRAM cell can also present different approaches, resulting in variations in the cross-section. Figure 12 compares the standard simulation that uses the “Tall” layout with a simulation using the “Thin” layout (see Figure 4). Also, we included a simulation that does not follow the layout rules, spacing the transistors apart from each other. Based on the results of this analysis, the variation between layout approaches presents an acceptable margin of error. This is valid because we are not investigating multi-cell upsets (MCUs). For MCUs, depending on the layout, the proximity between neighboring cells is different, and the charge sharing between them can change the MCU cross-section

result. On the other hand, when we do not consider the position of the transistor in a layout structure, the SEU cross-section changes completely. This result demonstrates that depending on the accuracy needed, it is important for the end user to define and follow a primary or approximate layout structure.

Another parameter that must be observed is the thickness of the BEOL. This parameter mainly affects the simulation results for low LET values. When the ion crosses the BEOL, the energy loss can affect the number of events observed, directly affecting the statistics and simulation accuracy. In Figure 12, we compare the thickness of the standard BEOL of 8 μm with a simulation that uses a BEOL with a thickness of 3 μm . The variation observed was minimal for a large part of the curve. The most significant impact was on the simulation time, which needed higher fluences to reach Monte Carlo accuracy. This result shows that slight variations in the thickness of the BEOL (simplified structure) for heavy ions have no significant impacts on the cross-section result. This is explained by the fact that minor variations do not change the energy of the incident ion significantly, at least when the ion energy is not too low.

Finally, the doping profile can also vary significantly depending on the manufacturer, and there is no straightforward way to obtain it. For the doping parameters in this work, we used approximate values in order of magnitude based on information in the literature and predictive models. Figure 12 compares the standard simulation with N-P WELL doping in the order of 10^{18} atoms/ cm^3 with a simulation with N-P WELL doping in the order of 10^{17} atoms/ cm^3 . The doping profile is directly related to the device's sensitivity, demonstrating a drastic change in the SEU cross-section. Among all the parameters discussed here, doping is the one that requires the most attention from the end user.

7. Conclusions

We proposed a framework based on a multi-physics methodology that applies simplified electrical modeling combined with the diffusion–collection model and MC simulations to calculate SEE cross-sections for impinging heavy ions, by using the PredicSEE tool developed in our laboratory. The standard 6T SRAM cell served as the DUT for SEU evaluations across 90 nm, 65 nm, 45 nm, and 32 nm bulk CMOS technologies. The proposed modeling approach and methodology demonstrated a strong correlation between simulation and actual irradiation data, without requiring any fitting of the simulation results or access to PDK data. The analysis explored different technology nodes, voltage scaling, and a wide range of LET for impinging particles. This proves that our approach is efficient for calculating the SEU cross-section for heavy-ion irradiation. Finally, the impact of input parameters was evaluated to demonstrate the critical points to be focused on by end users.

Most of the divergences found in the results can be improved by improving input data quality owing to the following aspects: (1) predictive SPICE models were used to extract basic information from the technologies due to the general lack of actual industrial data; (2) the sizing of the SRAM cell transistors was standardized in a fixed ratio for the simulations, but can vary a lot in commercial cells depending on the design requirements; (3) the design rules and doping profile used in the simulations in relation to the tested commercial cells, which may show differences depending on manufacturers.

It is important to note that the methodology presented is restricted to static analysis. To evaluate more complex circuits, it is necessary to consider different input vectors to obtain more realistic SEE cross-section behavior.

In this work, we evaluated bulk planar CMOS technology, but the same methodology could be also applied to other technologies, such as the fully depleted silicon on insulator (FDSOI) or the fin field-effect transistor (FinFET). For this purpose, the challenge would be developing a charge collection model compatible with these device structures.

Author Contributions: Conceptualization, C.M.M. and F.W.; data curation, Y.Q.A.; formal analysis, C.M.M. and F.W.; funding acquisition, F.S. and L.D.; Investigation, C.M.M., F.W. and Y.Q.A.; methodology, C.M.M. and F.W.; project administration, L.D. and R.G.A.; resources, Y.Q.A., F.S. and R.G.A.; software, F.W.; supervision, F.W. and A.M.; validation, C.M.M., F.W., Y.Q.A. and A.M.; visualization, C.M.M., F.W., Y.Q.A., A.M., F.S., J.B. and R.G.A.; writing—original draft, C.M.M.; writing—review and editing, F.W., Y.Q.A., A.M., F.S., J.B., L.D. and R.G.A.. All authors have read and agreed to the published version of the manuscript.

Funding: This project received funding from the European Union’s Horizon 2020 research and innovation program under grant agreement No 101008126.

Data Availability Statement: Data are contained within the article.

Conflicts of Interest: The authors declare no conflicts of interest.

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