Decentralized Control for a Fault-Tolerant, Fully Scalable Microprocessor Power Supply for Spacecraft Applications

Gregory Almeida, Marc Cousineau, David Le Bars, Frederic Pecourt, Philippe Ayzac

Decentralized Control for a Fault-Tolerant, Fully Scalable Microprocessor Power Supply for Spacecraft Applications

Gregory Almeida
LAPLACE
Université de Toulouse,CNRS, INPT, UPS
Toulouse, France
gregory.almeida@ieee.org

Marc Cousineau
LAPLACE
Université de Toulouse,CNRS, INPT, UPS
Toulouse, France
cousineau@laplace.univ-tlse.fr

David Le Bars
Electronic Product Line
Avionic, Power & TMTC
THALES Alenia Space
Toulouse, France
david.le-bars@thalesaleniaspace.com

Frederic Pecourt
Electronic Product Line
ASIC & FPGA
THALES Alenia Space
Toulouse, France
frederic.pecourt@thalesaleniaspace.com

Philippe Ayzac
Electronic Product Line
ASIC & FPGA
THALES Alenia Space
Toulouse, France
philippe.ayzac@thalesaleniaspace.com

***Abstract*—This paper presents a decentralized control method applied to a multiphase synchronous buck converter powering a microprocessor for a space application. The main objective is to remove the classic centralized controller which represents a single point of failure and to offer full modularity/scalability for the converter design. The complexity of the control part to address a large number of converter phases is simplified and the system is able to reconfigure itself with a different number of phases easily. This control method increases the level of functional safety of the converter and guarantees full availability of the delivered power if a fault occurs. The principles of the proposed solution are presented and a description of the analog building blocks of the controller implemented into an Application Specific Integrated Circuit (ASIC) is provided. Then, early-stage analyses of the voltage loops, the balancing functions, and the control signal interleaving are introduced taking into consideration the performance of the converter. Simulation results using Cadence™ OrCAD PSpice tool for the study of a 12V/1.2V 40A 250 kHz 4-leg multiphase converter are shown. They demonstrate the stable operation of the converter, the large bandwidth obtained for the regulating loops, and the possible reconfiguration modes offered by the scalability of the system.**

***Index Terms*—Multiphase, DC-DC Converters.**

I. Introduction

Since 1970-1980, power electronics for spacecraft applications, especially DC-DC converters including Buck, Boost, Buck-Boost, Weinberg, Venable, and others, is a leading topic in scientific laboratories worldwide [1]–[3]. The DC-DC converter module design was included in the roadmap for solutions involving high-density interconnect (HDI) and ASIC technologies since the 2000s [4], where different architecture/design methods have been studied. Along with these aspects, modern spacecraft are following the trend of voltage regulator modules (VRM) in the commercial roadmap to increasingly have their microprocessors fed with lower voltages and higher currents [5], [6].

The centralized architecture for the power supply and distribution system of the power conditioning unit based on a sequential switching shunt regulator (S3R) introduced in [7] has been widely used in spacecraft [8], [9]. However, the S3R fault-tolerant mechanism cannot be directly considered for modern low-voltage regulators, such as Point-of-Load. Additionally, due to issues in obtaining radiation-hardened circuits and more reliable DC-DC converter systems, space agencies such as the European Space Agency (ESA) and French Space Agency (CNES) proposed better solutions leading to some efforts as observed in [10]–[14].

There is an increasing preference for a decentralized architecture for converter control rather than a centralized one. This way, the decentralized modular control approach in multiphase interleaved DC-DC converter, described in [15]–[17], is an attractive solution for microprocessor satellite's power supply. Their main benefits are scalability, and fault-tolerant capability with easy reconfiguration modes.

This paper introduces investigations of the decentralized control approach in a multiphase synchronous buck converter for microprocessor power supplies to be applied in satellites (spacecraft). The work is part of the European project SCOPS (Scalable COntroller for Power Sources) involving satellite manufacturer teams as well as scientific partners. The following sections present the description of the control method, modeling, design guidelines, stability analyses, simulation results, and conclusions.

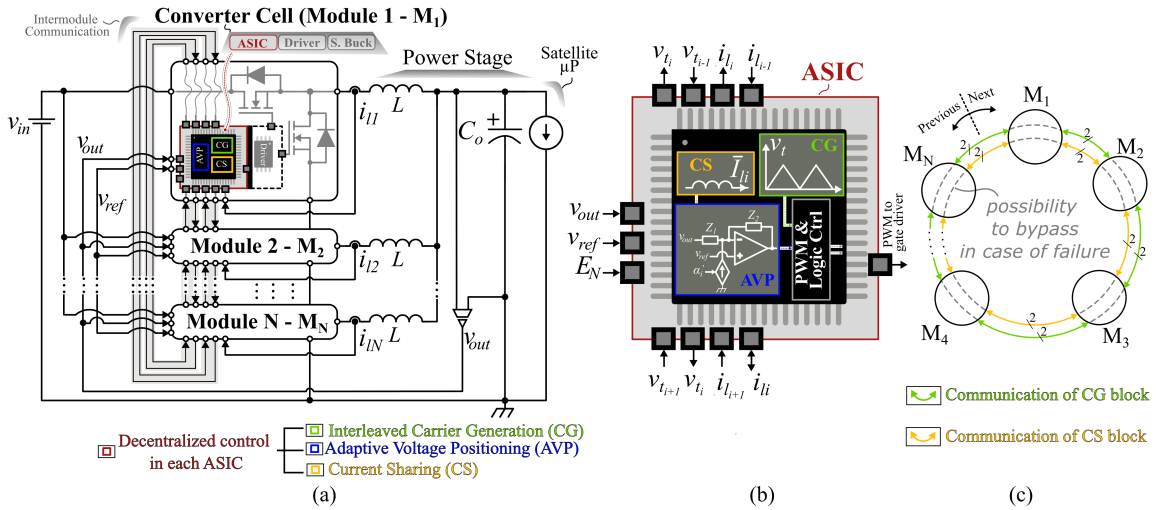

Fig. 1. Proposed decentralized control method applied to a multiphase DC-DC converter for satellite embedded power supply. (a) Topology. (b) ASIC internal-view. (c) Circular chain of inter-module communications.

II. System Description

Fig. 1 describes the basic principle of the decentralized modular control method. Fig. 1(a) presents the topology of a multiphase converter with N parallel identical modules, each including a local controller implemented in an ASIC, and two power MOSFET transistors with their drivers. The power stage includes output inductors, capacitors, and the load. There are three main blocks inside each ASIC: (i) interleaved carrier generation (CG) which has a self-alignment mechanism to provide interleaved carriers, (ii) Adaptive voltage positioning (AVP) which is essential to regulate the load voltage with good dynamic and smooth droop voltage control [18], [19], (iii) and Current sharing (CS) which improves the system performance by balancing, locally, the inductor currents (i_{l1}, i_{l2},...i_{lN}) in each phase. Fig. 1(b) shows a detailed and zoomed-view of one ASIC. Each module (or local controller) communicates with its adjacent modules in a circular and bidirectional communication chain, as shown in Fig. 1(c). Thus, in case of failure, the faulty module is bypassed maintaining the system's operation for functional safety purposes. This control method provides greater robustness and fault-tolerance capability for the system.

III. System Modeling, and Implementation of The Proposed Approach

This section briefly introduces the elementary blocks of the decentralized local controller and its modeling (i.e., basic principles, equations, and PSpice implementations). The early-stage design of a DC-DC multiphase converter for spacecraft applications may be challenging due to the harsh operating environment in space. To deal with this issue, SPICE-based modeling with analog behavioral modeling (ABM) blocks can be considered as an option. The three functions included in each local controller (the ASIC) are described in detail.

A. Interleaved carrier generation (CG) Block - Principle of self-alignment for interleaved carriers

Once N identical phases are parallel-connected, the interleaving of their carrier signals, providing the PWM signals to the drivers, is essential. It contributes to reducing drastically the size of the output capacitor C_o. The interleaved carrier generator implemented in the ASIC must ensure that the phase ϕ_i of the i^{th} carrier is equally shifted in phase in-between its adjacent carriers (i.e., the next carrier $\phi_{(i+1)}$ and the previous one $\phi_{(i-1)}$ as indicated in (1). Several methods can be used to obtain the generation of a carrier centered with its adjacent ones. Either methods based on digital calculations using phase shift information, or analog methods using specific operations on the exchanged signal waveforms. Ultimately, it is important that the inter-carrier phase shifts obtained $\phi_{\Delta t}$ meet equation (1).

$$\phi_{\Delta t} = \underbrace{\phi_{i+1}}_{\text{next}} - \phi_i = \phi_i - \underbrace{\phi_{i-1}}_{\text{prev.}} = \frac{2\pi}{N}. \tag{1}$$

Fig. 2 illustrates the fundamental principle and equilibrium challenges that an analog version of the self-alignment system may provide. To better understand its intrinsic convergence issues, Fig. 2(a) shows a pendulum analogy that is exactly what can arise for the CG block for different start-up conditions. The first equilibrium condition must be avoided and it can be effectively observed when all carriers are initialized at the same time, i.e. with a null phase-shift (no delay). On the other hand, the second equilibrium condition is the desirable one and it is reached when at least one carrier is initialized with a slight startup delay. The delay can be implemented with a simple RC network, to guarantee the convergence towards the second equilibrium state. Fig. 2(c) shows the interconnections and implementation of the CG block in each ASIC. A fault scenario can be emulated by disabling

the CG of the i^{th} faulty module (using the E_{N_i} pin). Further implementation details can be found in [20].

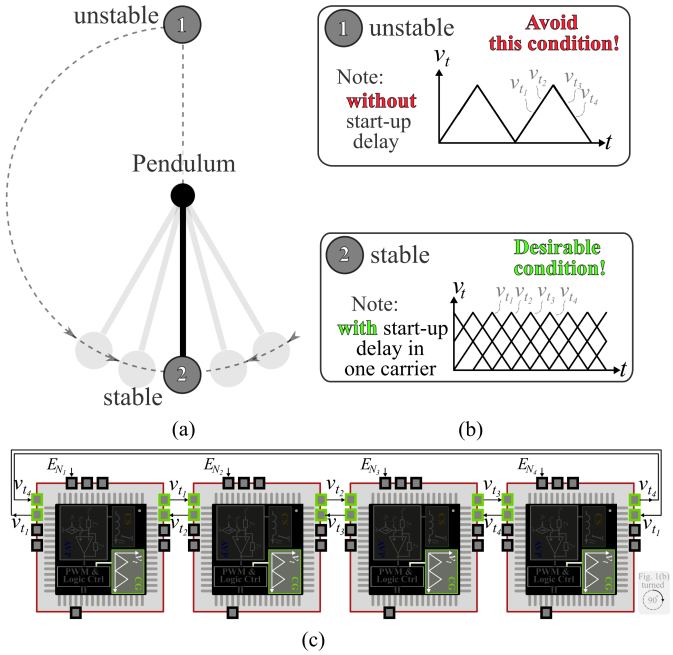

Fig. 2. Interleaved carrier generation (CG) principle (example with $N = 4$). (a) Pendulum analogy with two equilibrium states. (b) Steady-state waveforms. (c) Circular chain of inter-ASIC communications.

B. Adaptive Voltage Positioning (AVP) Block - Voltage regulation in a decentralized manner

The idea of a decentralized AVP consists of placing the voltage regulation loop at the module level (i.e., locally). Each module determines its own local duty-cycle (v_{D_i}). A parameter α_i for the inductor I_{l_i} current sensor is considered in the regulation loop such that in steady-state the relationship between the output voltage V_{out} and the reference voltage V_{ref_i} is maintained as in (2).

$$V_{out} = V_{ref_i} - \alpha_i.R.I_{l_i}, \tag{2}$$

where α_i is the current sensor sensitivity of the i^{th} phase, and $\alpha_i.R$ represents a virtual impedance provided by the local voltage loop.

Fig. 3(a) shows the principle of the AVP regulator included in each module. Note that a fraction of the inductor current ($\alpha_i.i_{l_i}$) is fed back into the impedance Z_{V1}. This has the effect of reducing the regulated output voltage as the current level increases. Then, each regulated phase of the converter operates as an ideal voltage source in series with a virtual impedance. Fig. 3(b) illustrates the Thevenin equivalent circuit obtained considering an AVP-type regulation loop included in each local controller of the N modules placed in parallel. The circuit of Fig. 3(b) shows a suitable and simplified view in terms of voltage regulation of how the studied system depicted in Fig. 1(a) behaves from a steady-state DC point of view. Fig.

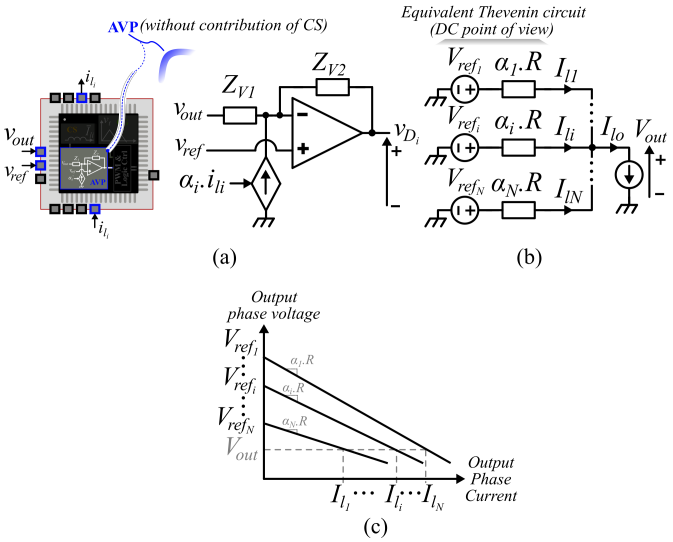

Fig. 3. AVP block. (a) Local AVP-type controller in one module. (b) Thevenin equivalent circuit (N modules) of the multiphase converter depicted in Fig. 1(a). (c) Output characteristic of the N regulated phases (scenario highlighting mismatches on circuit parameters).

3(c) shows the output characteristic associated with the Thevenin equivalent circuit using an AVP-type controller, with voltages regulated (locally) in each converter phase. This illustrates scenarios taking into account mismatches on circuit parameters (e.g., mismatches on op-amps offsets, on impedances Z_{V1} and Z_{V2}, reference voltages, and inductor current sensor sensitivities), leading to unbalanced inductor currents. When mismatches are critical, CS block is an effective way to address the problem. More details about this decentralized voltage regulation loop can be found in [21].

Concerning the design of the AVP controller, let $C_V(s)$ be the transfer function in the Laplace domain of the analog AVP-type controller. Depending on the requirements of the application, $C_V(s)$ can be either a simple proportional-integrator (PI) for normal bandwidth performances or a more sophisticated corrector like an integrator action plus one or two zeros compensations. For each phase, two feedback loops are involved, a fast current loop controlling the value of the phase inductor current and a slower voltage loop imposing the voltage across the load (i.e., the microprocessor). Thanks to the large bandwidth of the current loop, the system can be approximated to a simple voltage loop involving it a voltage-controlled current source imposing the value of the inductor current. For that reason, a controlled current source appears in Fig. 3(a). Thus, the transient response of the overall system (i.e., with power stage and controller) can be simplified from a 2nd-order system to a 1st-order one. The basic equation for the voltage-loop controller is presented in (3)

$$C_V(s) = -\frac{Z_{V2}(s)}{Z_{V1}(s)}, \tag{3}$$

where impedances $Z_{V1}(s)$ and $Z_{V2}(s)$ are implemented by

associations of resistors and capacitors.

Depending on the design requirements, $Z_{V1}(s)$ can be made either by using a simple resistor, $Z_{V1}(s) = R_{V1}$, or a capacitor with a resistor in parallel, $Z_{V1}(s) = R_{V1}/(1 + s.R_{V1}C_{V1})$ to provide a high frequency zero. $Z_{V2}(s)$ is made by a capacitor in series with a resistor, $Z_{V2}(s) = R_{V2} + 1/(C_{V2}.s)$, providing the integrator effect and the proportional gain R_{V2}/R_{V1}.

C. Current-sharing (CS) Block - The inductor current balancing method

The idea of the CS block is that to balance the several inductor currents of the converter, each local controller has to implement a local correction to cancel an error signal. An error exists if the inductor current of the i^{th} phase i_{l_i} is not rigorously equal to the average value of the currents of its adjacent phases, i.e. the next $i_{l_{i+1}}$ and the previous $i_{l_{i-1}}$ currents. Fig. 3(c) shows such a case where the phase currents are different due to mismatches, for instance. As a consequence, the CS block will act to balance phase currents by adjusting the relative position of their output characteristics to get a focal point for which all currents are equal. To do that, a local reference voltage correction v_{Δ_I} is applied.

Fig. 4 shows the basic principle involved in the CS block. Fig. 4(a) shows the ASIC implementing the local controller with the effective elements related to the current-sharing (CS) block. The controller $C_{\Delta i}$ in Fig. 4(a) can be either a simple proportional or a PI controller, which must be tuned to guarantee zero steady-state error and unconditional stability. Fig. 4(b) shows how the equivalent Thevenin circuit can be seen with the contribution of the CS block. Consequently, it will adjust locally the phase currents to reach the same steady-state point, as observed in Fig. 4(c). The interconnection of the CS block

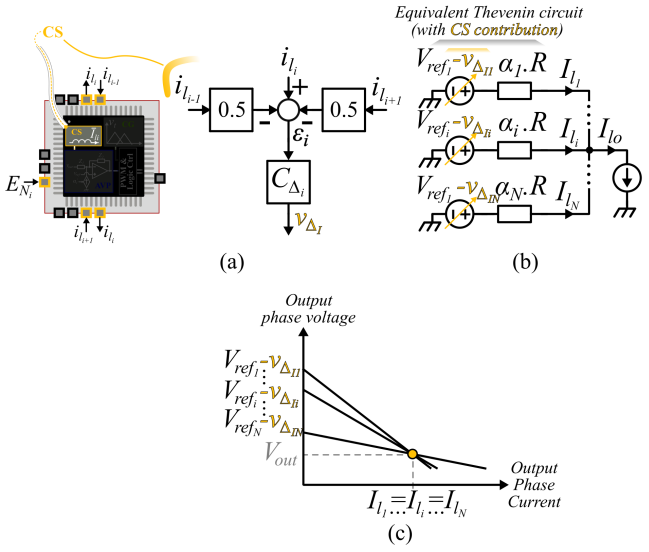

Fig. 4. CS block. (a) Function description for one module. (b) Equivalent Thevenin circuit with CS contribution. (c) The phase output characteristics of AVP with CS contribution.

follows a circular-chain structure. At last, this function is modular and scalable, and also it allows the system to reconfigure itself if necessary. Indeed, thanks to the ring communication, if one module is removed from the chain, one has just to connect the adjacent phases together to close the chain of communication and operate with $N-1$ modules. Each CS block is connected similarly as shown previously for the case of the carrier-generation (CG) block in Fig. 2(c).

It is worth noting that the CS block is responsible for balancing, locally, each current, whereas the AVP block adjusts the general duty-cycle to regulate the load voltage. The local error $e_i(t)$ computed in each local CS is shown on (4), whereas the CS controller $C_{\Delta_i}(s)$ expression is given in (5), as:

$$e_i(t) = i_{l_i}(t) - 0.5(\underbrace{i_{l_{i+1}}(t)}_{\text{next}} - \underbrace{i_{l_{i-1}}}_{\text{prev.}}); \tag{4}$$

$$C_{\Delta_i}(s) = \frac{V_{\Delta_{Ii}}(s)}{E_i(s)} = -K_{\Delta i}\left(\frac{1}{1+\tau_{\Delta i}.s}\right), \tag{5}$$

where $K_{\Delta i}$ is a proportional gain that allows adjusting the closed-loop time response, and $\tau_{\Delta i}$ is a time constant that should be tuned to guarantee the system stability.

More details of the current-sharing technique for decentralized control can be found in [22], [23].

IV. Design and Stability Analyses

A. Controller designs

The design of the controllers dedicated to the current and the voltage regulation loops is described by the control block diagram depicted in Fig. 5. It should be noted both controllers $G_V(s)$ and $G_I(s)$ are involved in the same circuit made by an opamp and external impedances $Z_{V1}(s)$ and $Z_{V2}(s)$ shown previously in Fig. 3(a).

The AVP-control method intrinsically has two loops involved, as discussed previously. In essence, the design should assume that the inner loop is much faster than the outer loop. In other words, a large bandwidth for the current loop is imposed. Then, in the frequency range of the voltage loop, a part of the circuit operates as a voltage-controlled current source. Such a hypothesis allows the simplification of the control block circuit, as depicted in Fig. 5(b).

Considering $Z_{V1}(s)$ is a simple resistor R_{V1} and $Z_{V2}(s)$ is made by a resistor R_{V2} in series with a capacitor C_{V2}, the bandwidths of the current f_{cI} and voltage loops f_{cV} are defined, respectively, by the following expressions:

$$f_{cI} = \frac{1}{2\pi}.\frac{V_{in}}{V_p}.\frac{\alpha R_{V2}}{L}, \tag{6}$$

$$f_{cV} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{N}{C_o}, \tag{7}$$

Knowing the system parameter values (e.g., f_{sw}, V_{in}, V_p, L, etc), and considering equations (6)-(7), a suggestion

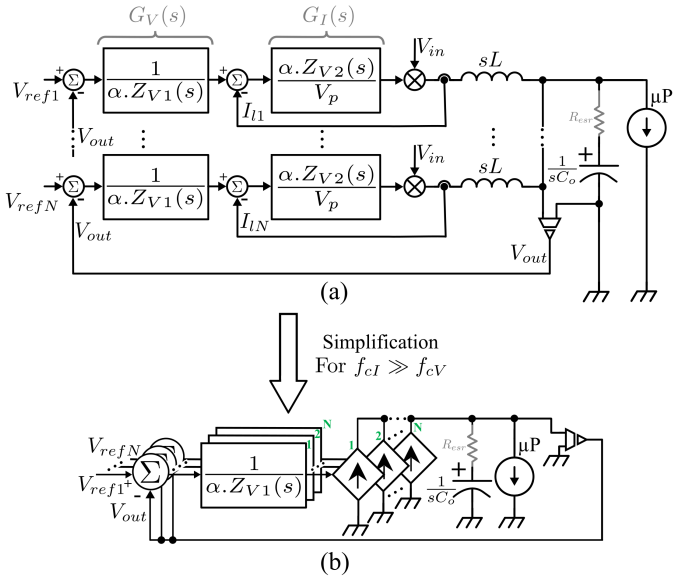

Fig. 5. Control block diagram description. (a) AVP-control block diagram for N-modules. (b) Simplified block diagram when $f_{cI} \gg f_{cV}$. The controllers impedances can be assumed as $Z_{V1}(s) = R_{V1}$ and $Z_{V2}(s) = R_{V2} + 1/(sC_{V2})$.

for the step-by-step process for the controller design is summarized as follows:

1) Set f_{cI} and f_{cV} as a function of the switching frequency f_{sw} such that:

$$f_{cI} = \frac{1}{3} f_{sw}; \qquad f_{cV} = \frac{1}{10} f_{sw}; \tag{8}$$

2) Determine R_{V1} from a given maximum output voltage droop ΔV, taking into acount the sensibility of current sensor α:

$$R_{V1} = \frac{1}{\alpha} . \frac{\Delta V}{I_{L_{Max}}}; \tag{9}$$

3) Determine C_o from (7), using R_{V1} and f_{cV} determined previously.
4) Determine R_{V2} from (6).

It should be noted that the design guidelines presented here are just recommendations and, depending on the case study requirements, other methods or rules-of-thumb to determine the compensator type as well as parameter values can be used, as in [24], [25]. Indeed, the regulation loop bandwidths can be chosen depending on various design factors and constraints related to end-user priorities.

B. Stability Analysis

The stability analysis is performed considering the phase margins obtained for the inner and outer regulation loops. In this case, the frequency response of the system can be done based on theoretical approaches detailed in [24]. A small-signal study using PSpice simulations is performed to observe the open-loop transfer functions in a Bode diagram and determine the phase margins. Then, it is necessary to open the loop at some specific points in the circuit. Details about the method used to open the loop can be found in [25]. The PSpice simulation circuit dedicated to the stability analysis is presented in Fig. 6(a) for the outer-loop and in Fig. 6(b) for the inner-loop.

Fig. 7 represents the bode diagram obtained with one and four modules (i.e., $N = 1$ or 4). The feedback loop bandwidths f_{cI} and f_{cV} correspond to (6) and (7) associated with controller designs. Considering the switching frequency f_{sw} equal to 250 kHz, it can be seen that the inner-loop and outer-loop present positive phase margins of more than 60 degrees. Then, it can be assumed that stability is guaranteed. It is worth noting that the number of modules N has a strong impact on the resonance frequency f_n position which requires attention in terms of the damping factor for load transient responses. Further analysis with modal responses can be found in [26].

Considering the inner-loop, it can be observed that the number of modules N has no impact on its bandwidth

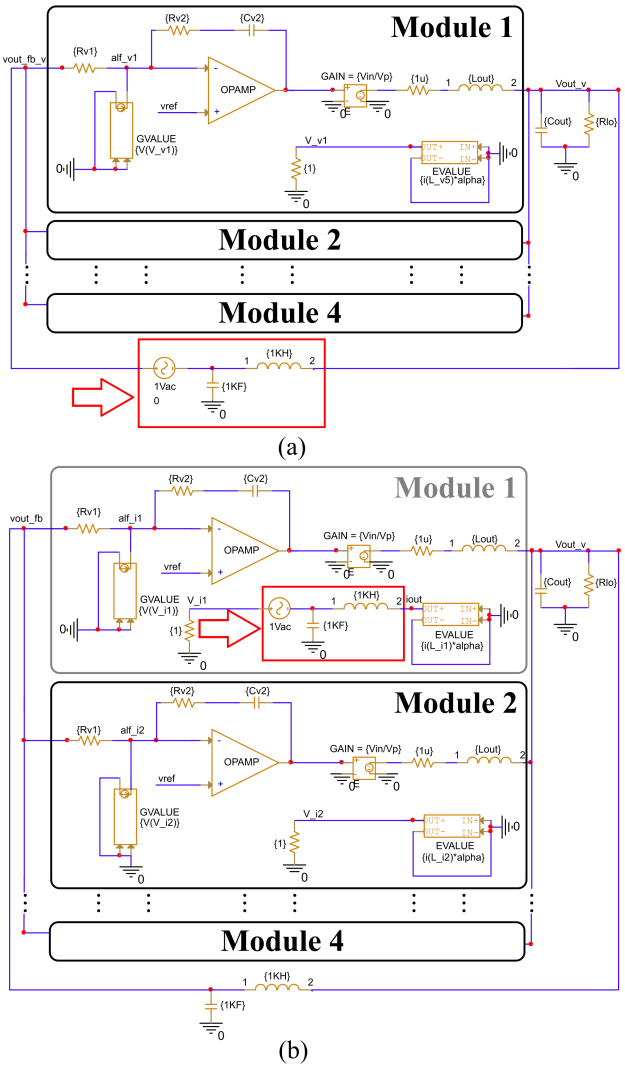

Fig. 6. Transfer functions and stability analysis using OrCAD-PSpice simulator. Opening the loop for analyzing the: (a) outer-loop, and (b) inner-loop. The red box indicates AC excitation and the opening point in the schematic.

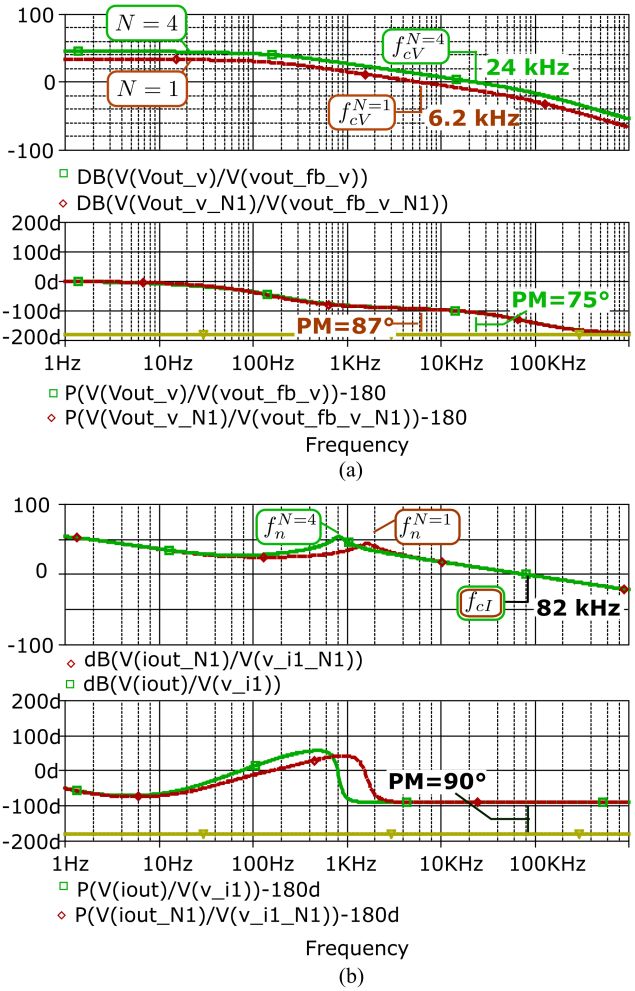

Fig. 7. Simulation results for the stability analysis with $N = 1$ and $N = 4$. (a) The transfer function of the Outer-loop. (b) The transfer function of the Inner-loop.

f_{cI}. On the other hand, for the outer-loop, the number of modules N has an impact on the gain of the open loop transfer function at low frequency as well as on its bandwidth f_{cV}. One way to keep f_{cV} constant is to consider the total output capacitor C_o is made of N different output capacitors $C_o^{'}$ placed in parallel (i.e., one per phase). By doing so, it is possible to cancel the factor N in (7) since $C_o = N.C_o^{'}$, leading to:

$$f_{cV} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{N}{N.C_o^{'}} = \frac{1}{2\pi}.\frac{1}{\alpha R_{V1}}.\frac{1}{C_o^{'}} \qquad (10)$$

This last consideration is interesting in terms of design because the analysis can be handled by considering only one single phase.

V. Simulation Results of The System

The decentralized control approach and its basic principles were validated by simulations using OrCAD-PSpice $v22.1$ tool. Table I lists the main parameters of the application.

The schematic overview of a 4-leg multiphase converter implemented into the simulator is shown in Fig. 8, which

TABLE I
Parameter values for simulation tests of the system.

Parameters	Value	Description
f_{sw}	250 kHz	Switching frequency
N	4	Number of Phases
I_{out}	40 - 100 A	Output current range
I_{ph}	10 - 25 A	Phase current range
V_{out}	0.6 - 1.2 V	Output voltage range
V_{in}	3 - 12 V	Input voltage range
$\Delta_{V_{max}}$	30 mV	Maximum admissible output voltage range
α	0.01 m	Effective current sensor sensitivity
R_{V1}	100 Ω	AVP-Controller $Z_{V1}(s)$
R_{V2}	19.6 kΩ	AVP-Controller $Z_{V2}(s)$
C_{V2}	50 nF	AVP-Controller $Z_{V2}(s)$
αR_{V1}	1 mV/A	AVP Slope per phase

contains several blocks implemented into the simulator. Such blocks are related to the power part composed of a switching-cell, an output inductor, a current sensor (I-sense), the load with a voltage sensor (V-sense), and the control part composed of the ASIC which includes the AVP-controller (AVP), the interleaved carrier generator (CG) and the balancing current controller (CS).

Figs. 9 shows the simulation results related to the CG block behavior. The self-interleaving of the carriers during operation is observed, for the cases of three ($N = 3$) and four phases ($N = 4$), during the start-up and under reconfiguration procedures. Concerning the start-up, it needs less than 30 μs to reach the expected equilibrium state for which the carriers are well interleaved. In addition, when a reconfiguration event is forced by disabling a phase during operation (at 60 μs), i.e. reconfiguring from 4 to 3 phases, the CG block provides suitable self-alignment,

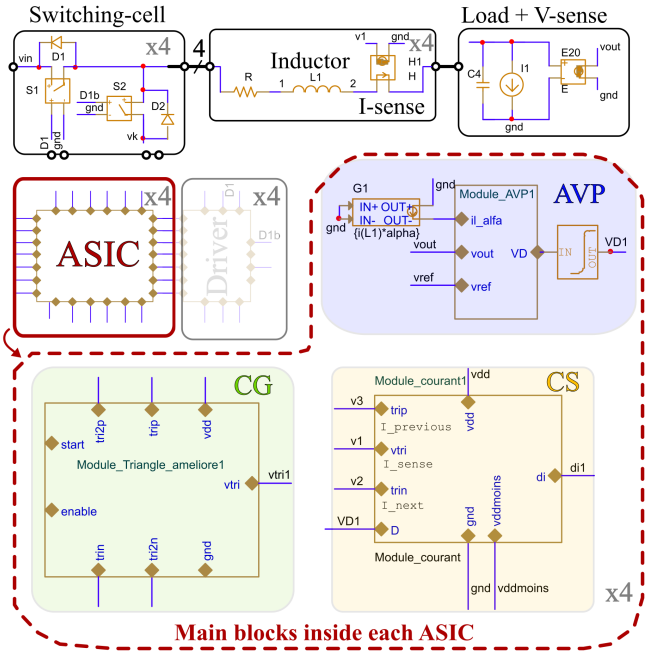

Fig. 8. The main blocks of the converter implemented with Cadence™ OrCAD-PSpice simulator.

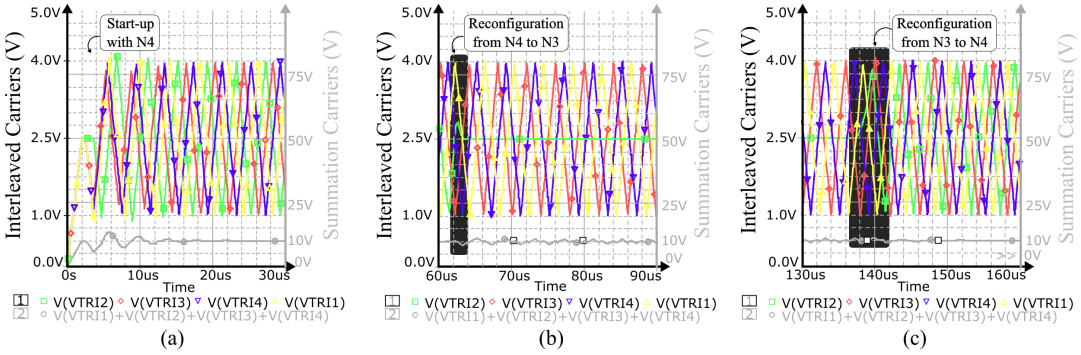

Fig. 9. Simulation result. (a) Start-up of the interleaved carriers. (b) reconfiguration from 4 to 3 phases, and (c) restoration from 3 to 4 phases. The summation of carriers is depicted in gray lines.

reconfiguring the phase shifts of the carriers properly. The summation of the carrier's waveforms provides a good indicator to quantify and validate the convergence of the interleaving. Indeed, in steady-state with an appropriate interleaving, this signal is either constant for N even or presents a frequency equal to $N.f_{sw}$ for N odd.

Fig. 10 presents the output voltage of the multiphase converter and both the phase and output currents in steady-state. One can observe the regulated voltage is well established within its minimum and maximum limits (i.e., respecting its maximum allowable voltage ripple), as shown in Fig. 10(a). Additionally, the droop of the voltage corresponds to the expected one (i.e., -10 mV). Indeed, note that each phase current is well balanced and operates properly with an average value close to 10 A per phase resulting in a load current equal to 40 A, as shown in Fig. 10(b).

Fig. 11 shows the load-transient response of the converter. A load current step from 0 A to 40 A is applied. Fig. 11(a) shows output currents, whereas the phase currents can be observed in Fig. 11(b). Figs 11(c) and 11(d) show a zoomed view of phase-currents before and after the transient, respectively. Note that the phase currents are well-balanced even during the transient. From Figs. 11(e) and 11(f), one can observe that the droop of the voltage Δ_V, after the transient, corresponds to the expected one (i.e., $\Delta_V \approx$-10mV) for a current load step of 40 A.

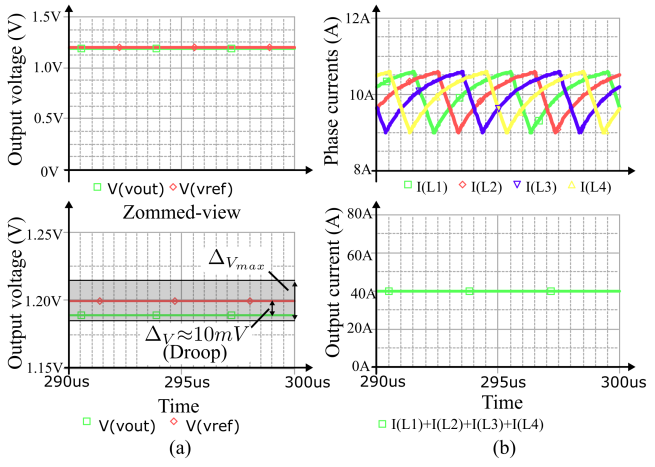

Fig. 10. Simulation result. Steady-state waveforms. (a) Output voltage. (b) Phase currents (on the top) and Output current (on the bottom).

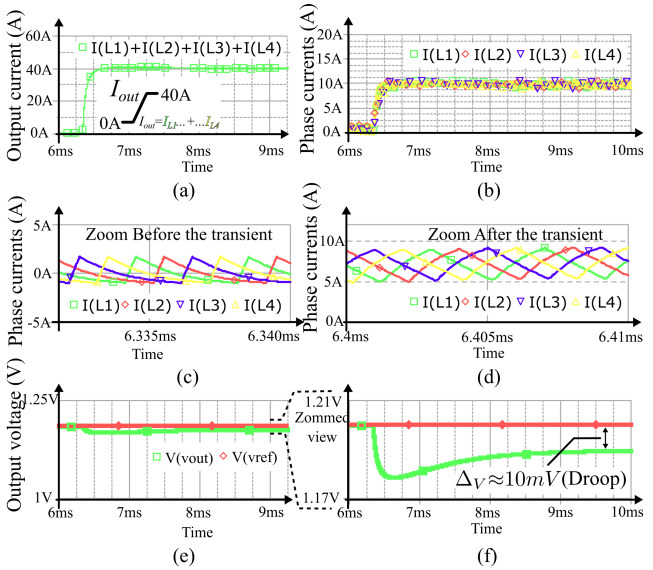

Fig. 11. Simulation result. Load-transient response of the converter. (a) Output current. (b) Phase currents. (c) Zoomed-view of phase currents before the transient. (d) Zoomed-view of phase-currents after the transient. (e) Output voltage and reference voltage. (f) Zoomed-view of output voltage and reference.

VI. Conclusions and Future Works

This paper has introduced a decentralized control method applied to a multiphase synchronous buck converter dedicated to supplying a microprocessor for a spacecraft application. A local controller is implemented in an ASIC and associated with each phase of the converter. It implements three basic functions: i) the phase control signal interleaving, ii) the output voltage regulation, iii) and the inductor current balancing. With this approach, no centralized controller is needed. The modularity/scalability of the resulting system leads to interesting properties in terms of functional safety. Indeed, the system is able to auto-reconfigure in case of failure occurring either in the power part or in the control part of the converter. Hence, it

is able to continue to operate with N-1 active phases. This is due to the usage of local controllers connected together in a circular chain of communications.

The simulation results validate the performance of the proposed method which can be seen as an effective solution to achieve the requirements of the embedded space system. This work is part of a European project involving satellite solution manufacturers and university partners. Due to confidentiality terms, some details and explanations are not included in this version of the article. Future works related to the ASIC characterization will provide experimental results to confirm simulation predictions. Moreover, other scenarios, as well as other alternative decentralized control methods based on current-mode control methods (e.g., peak or valley detection, or even by sensing the average inductor current) are currently under study and may be discussed soon.

Acknowledgment

This project has received funding from the European Union's Horizon Europe research and innovation program under grant agreement No 101082266. The authors acknowledge the active contribution of Thales Alenia Space, LAPLACE laboratory, Institut National Polytechnique de Toulouse (Toulouse-INP), and the other involved partners in the SCOPS project.

References

[1] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, 1976, pp. 18–34.

[2] A. Capel, "Charge controlled conversion principle in DC/DC regulators combines dynamic performances and high output power," in *1979 IEEE Power Electronics Specialists Conference*, 1979, pp. 264–276.

[3] R. P. Severns and R. E. Corbett, "Power Electronics in Space: A Review and Projection," *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-20, no. 4, pp. 493–499, 1984.

[4] A. Salim and G. Carr, "Power Electronics For The Next Century-First Step," in *2000 IEEE Aerospace Conference. Proceedings (Cat. No.00TH8484)*, vol. 5, 2000, pp. 335–339 vol.5.

[5] Stanford, "Microprocessor voltage regulators and power supply trends and device requirements," in *2004 Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs*, 2004, pp. 47–50.

[6] K. Radhakrishnan, M. Swaminathan, and B. K. Bhattacharyya, "Power Delivery for High-Performance Microprocessors—Challenges, Solutions, and Future Trends," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 4, pp. 655–671, 2021.

[7] D. O'Sullivan and A. Weinberg, "The Sequential Switching Shunt Regulator S3R," in *Proceedings of Third Space Power Conditioning Seminar*, no. ESA SP-126, 1977.

[8] F. Blaabjerg, *Control of Power Electronic Converters and Systems*. Academic Press, 2018, vol. 2.

[9] Z. Hong-yu, Z. Bo-wen, and Z. Dong-lai, "Overview of Architectures for Satellite's Regulated Bus Power System," in *2020 IEEE 1st China International Youth Conference on Electrical Engineering (CIYCEE)*, 2020, pp. 1–8.

[10] A. Amirahmadi, A. Barchowsky, C. Stell, E. Merida, A. Ulloa-Severino, and G. Carr, "Design and Optimization of Radiation-Hardened Isolated Converters for Jovian Environments," in *2019 European Space Power Conference (ESPC)*, 2019, pp. 1–5.

[11] F. Stoegerer and T. Panhofer, "Low Power DC-DC Converter Based on Automotive-Grade Components Featuring Maximum SEE Immunity," in *2019 European Space Power Conference (ESPC)*, 2019, pp. 1–6.

[12] D. Schofield, "Design and Implementation of a COTS, GaN–based Power Converter for Spacecraft Applications," in *2019 European Space Power Conference (ESPC)*, 2019, pp. 1–4.

[13] Silva and B. Tavares, "DC-DC Converter for Aerospace Industry," 2014. [Online]. Available: https://fenix.tecnico.ulisboa.pt

[14] M. Notarianni, B. Messant, and P. Maynadier, "Using GaN HFET to replace MOSFET in DC/DC for space applications," in *2019 European Space Power Conference (ESPC)*, 2019, pp. 1–3.

[15] M. Cousineau, "Modular Static Converters with Parallel or Series Architecture and Decentralized Modular Control," France Patent WO 2014/005 973 Al, 1 9, 2014. [Online]. Available: https://patents.google.com/patent/WO2014005973A1/en

[16] M. Cousineau and B. Cougo, "Interleaved converter with massive parallelization of high frequency GaN switching-cells using decentralized modular analog controller," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 4343–4350.

[17] M. M. Hillesheim, M. Cousineau, and L. Hureau, "Reconfigurable Partial-Decentralized Control of a Multiphase Converter for Fail-Operational Automotive Processor Power Supply," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019, pp. P.1–P.8.

[18] K. Yao, Y. Ren, J. Sun, K. Lee, M. Xu, J. Zhou, and F. Lee, "Adaptive voltage position design for voltage regulators," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 1, 2004, pp. 272–278 Vol.1.

[19] K. Yao, K. Lee, M. Xu, and F. Lee, "Optimal design of the active droop control method for the transient response," in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03.*, vol. 2, 2003, pp. 718–723 vol.2.

[20] M. Cousineau, M. Le Bolloch, N. Bouhalli, E. Sarraute, and T. Meynard, "Triangular carrier self-alignment using modular approach for interleaved converter control," in *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, 2011, pp. 1–10.

[21] M. Cousineau and Z. Xiao, "Fully decentralized modular approach for parallel converter control," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 237–243.

[22] Z. Xiao, M. Cousineau, E. Sarraute, and T. Meynard, "Modular control of parallel isolated micro-converters dedicated to conversion network," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 2555–2562.

[23] M. Le Bolloch, M. Cousineau, and T. Meynard, "New Masterless Modular Current-Sharing technique for DC/DC Parallel converters," in *Proceedings of 14th International Power Electronics and Motion Control Conference EPE-PEMC 2010*, 2010, pp. T3–73–T3–80.

[24] R. Erickson and D. Maksimovic, *Fundarnentals of Power Electronics*, 2nd ed. Kluwer Academic Publishers Group, 2001.

[25] C. Basso, *Switch-Mode Power Supplies, Second Edition: SPICE Simulations and Practical Designs*, 2nd ed. McGraw Hill Professional, 2014.

[26] M. Mannes, M. Cousineau, M. Vivert, G. Aulagnier, and G. Gateau, "Eigendecomposition of a Digital Iterative Decentralised Interleaving for Multicellular Converters," *Elsevier Journal - Mathematics and Computers in Simulation*, vol. 184, pp. 82–105, 2021.