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Impact of the four French RISC-V Contests on Education and Research

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Abstract: We take stock of the four contests around the CVA6 processor organized in higher education in France. An analysis of the impact of these contests is drawn up and recommendations for potential organizers are provided.

1 Introduction

In France these last years the ecosystem around RISC-V and open hardware has grown including key industrial players such as Greenwaves, Thales, Dolphin, Bosch, Kalray and SiPearl, among others. At the same time, academic interest on RISC-V architecture has increased in the higher education and research sectors, indicating fertile ground for collaborative advances.

In response to this burgeoning interest, and to foster a synergistic environment between industry and academia, a contest has been initiated by Thales, with the support of the GDR SoC² (*Groupement de recherche* – research group of different labs) and the GIP (*Groupement d'intérêt Public*) CNFM, the National Coordination for Microelectronics Education. The main goal is to motivate students to deepen their understanding and expertise in processor architecture, based on the RISC-V instruction set architecture (ISA). In addition, the contest aims to broaden the adoption of RISC-V ISA in academia, thereby expanding the open hardware community in France. At the international level, the RISC-V community is very active but at the best of our knowledge there are only two similar initiative involving students in India and in China since 2019. At the European level, since 2022 the RISC-V ecosystem is on the priority axes of industrial development for the Chips Act, as part of the Strategic Research and Innovation Agenda for the Electronic Component and Systems community. Finally, the initiative aims to strengthen collaborative links between academia and industry, paving the way for innovative advances and knowledge exchange.

2 The French RISC-V Contests

The French RISC-V student contests are organized by:

- Thales, a large electronics company with stakes in research and open-source hardware;
- The GDR SoC², gathers 67 laboratories in embedded systems and systems on chip (SoC), supported by the CNRS¹ and associated with the Universities and Engineering Schools;
- The National Services of the GIP CNFM, that pools resources for teaching and research in the field of microelectronics.

Four annual contests have already been organized, based on the CVA6 open-source RISC-V application core which originates from ETH Zürich's ARIANE (Zaruba and Benini, 2019) and is now curated by members of the OpenHW Group. Every year, teams of 2 to 4 students have to address a specific challenge (see Table 1).

Academic year	Challenge	nb. of teams
2020-21	Performance & area optimization	12
2021-22	Energy efficiency optimization	12
2022-23	Defeat cyber-attacks under Zephyr OS	19
2023-24	Extensions to accelerate digit recognition	13

Table 1: The four annual contests on CVA6 processor

Each year, an open-source technical kit is made available by Thales in November and the students have six months to devise a solution to the proposed challenge. For each challenge, an objective criterion is used to rank the teams' results, e.g. the number of cycles to recognize a digit in 2023-24. The two best ranked teams get an award and a prize during a ceremony at the GDR SoC² annual symposium. Student teams have to be registered by their universities and supervised by a professor. Some universities include the contest in the tutorial hours of the curriculum. The other teams run the contest in their leisure time.

¹National Center for Scientific Research

3 Impact analysis

The impact of the RISC-V French contest is ensured by the support and collaboration of the organizers. The latter estimate that between 45% to 50% of relevant Universities Master degrees on Computer Science and Computer Engineering Schools have been involved in one or more contests over the four years.

After three successful contests, and the current one, with a significant participation of the French academic ecosystem, it is interesting to measure the impact of the contest on the stakeholders (universities, supervisors as well as the students themselves). For that purpose, the organizers submitted a questionnaire to all supervisors (48) who participated to at least one contest, resulting in 25 answers, which is significant to interpret the results.

A first set of questions dealt with the reasons why participating to the contest to analyze what would be the key elements for a successful edition. The motivation of the students is cited as the primary reason for the participation by the professors, with also the possibility to introduce different notions of computing using a real and complex project supported by an industrial company. The context on RISC-V is often considered as of great interest for participating, especially in universities with courses (or research domains) perfectly matching processor architectures. On the students viewpoint, some are interested in the RISC-V itself, or in processor architecture in general, but the specific subject of the challenge is also important for more than 60% of the participating supervisors. For example, the two last contests are more focused on applications (cybersecurity, AI) and specifically attracted students interested in these domains, while the first two were more dedicated to architecture (performance or energy optimization).

A second set of questions measured the impact of the contest on the universities, professors and students. For more than 30% of the responding supervisors, the contest favorably impacted their teaching/research activities (some reported the contest as a possible course project). This proportion is almost the same regarding the positive impact of the contest on the interest of the students for computing architecture and even higher (44%) regarding their professional integration (PhD or first job), no impact being only reported by 8%. Some professors highlighted the participation to the contest as a key point to mention during internship or job interviews. Additionally, some supervisors (four) with three participations are the ones for which the contests have the highest impact regarding teaching activities. Generally, positive impacts (teaching/research activities, professional in-

tegration, etc.) are more visible for universities with a higher number of participations.

4 Points of attention

Analyzing the four contests, and based on the feedbacks from both students and supervisors, the main difficulty is to set up the complete framework for using the CVA6 processor and the required tools. That's why we never changed the version of tools and board from one year to the next to ease this setup for the returning universities. The second point of attention is the topic of the contest, that impacts the decision of students to attend the contest, but also on the goal of the contest. This contest targets the computer architecture and the open-source approach, not the application. This point also has an impact on the regulation of the contest (how the teams are evaluated), and on the preparation of the first technical kit furnished at the beginning of the contest. In addition, it is recommended to choose the duration of the contest as long as possible (e.g. 6 months) to accommodate the academic calendars. Finally evaluating teams requires a last effort in order to validate in the strictly same environment the results announced by the teams. It means that all solutions of the teams are re-implemented by the Thales in its own environment.

5 Conclusions

In order to promote computing architecture in French universities, extend the RISC-V community and reinforce the cooperation between industrial and academia, an annual French RISC-V contest is organized since four years by Thales, the GDR SoC² and the CNFM. The impact study reveals a very positive effect on education and professional integration, and the occurrence of participations reinforces this impact. This initiative could easily be extended to other countries, which would spark new vocations in computer sciences and help promoting RISC-V around students, academia and industrials.

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