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SOI MOS technology for spin qubits

Louis Hutin
 CEA, LETI, Minatec Campus,
 F-38054
 Grenoble, France
 louis.hutin@cea.fr

Benoit Bertrand
 CEA, LETI, Minatec Campus,
 F-38054
 Grenoble, France
 benoit.bertrand@cea.fr

Yann-Michel Niquet
 CEA, INAC-MEM,
 F-38054
 Grenoble, France
 yann-michel.niquet@cea.fr

Jean-Michel Hartmann
 CEA, LETI, Minatec Campus,
 F-38054
 Grenoble, France
 jean-michel.hartmann@cea.fr

Marc Sanquer
 CEA, INAC-PHELIQS,
 F-38054
 Grenoble, France
 marc.sanquer@cea.fr

Silvano De Franceschi
 CEA, INAC-PHELIQS,
 F-38054
 Grenoble, France
 silvano.defranceschi@cea.fr

Tristan Meunier
 CNRS - Institut Néel,
 F-38042
 Grenoble, France
 tristan.meunier@neel.cnrs.fr

Maud Vinet
 CEA, LETI, Minatec Campus,
 F-38054
 Grenoble, France
 maud.vinet@cea.fr

Abstract— We fabricated Si Quantum Dot (QD) devices using relatively minor adaptations of a standard SOI CMOS process flow. We demonstrated that the spin of confined charges could be controlled via a local electrical-field excitation, owing in the case of electrons to a geometrically-enabled tuning of the valley splitting and inter-valley spin-orbit coupling. We discuss improvement paths such as extending the spin coherence time by using epi-layers of nuclear-spin-free ^{28}Si (99.992%) as a device template, and developing novel 3D architectures compatible with topological quantum error correction schemes.

I. SOI CMOS-DERIVED SPIN QUBITS

We aim to engineer a device for the coherent manipulation of information encoded as a quantum superposition of basis states, *i.e.* a quantum bit (qubit). In particular, the qubit state is mapped to the spin of a charged particle confined in a Quantum Dot (QD) [1]. We focus on QDs defined in a silicon lattice [2]. A popular way of isolating charges starts with forming a 2-Dimensional Electron Gas (2DEG) at the interface of a heterojunction (Si/SiGe), and obtain lateral confinement through depletion-mode Field-Effect Gates [3]-[7]. Alternately, charges can be confined at MOS interfaces [8],[9]. In our case (Fig.1), we accumulate holes or electrons below MOS Gates wrapping around mesa-etched Si NanoWires (NW) [10],[11]. In fact, the main difference versus a standard SOI NWFET process flow is the spacer width preventing doping between densely patterned Gates (pitch 65nm), forming 1D arrangements of nearest neighbor-coupled QDs. Coherent control and dispersive readout of hole spin qubits were recently demonstrated in such CMOS-compatible devices [12],[13].

II. CORNER DOTS AND SPIN-VALLEY-ORBIT MIXING

Surprisingly, we also observed spin transitions in MOS Gate-confined electrons using only E-field excitations [14], without resorting to co-integrated micro-magnets [15]. The underlying mechanism is based on the interplay between Spin-Orbit Coupling (SOC) and the multi-valley structure of the Si Conduction Band, and is enhanced by the “Corner Dot” device geometry [16]. By offering the ability to break and restore the confinement symmetry at will, the SOI Back-Gate permits fast programming in valley mode, and information storage in spin mode (Fig. 2) [17].

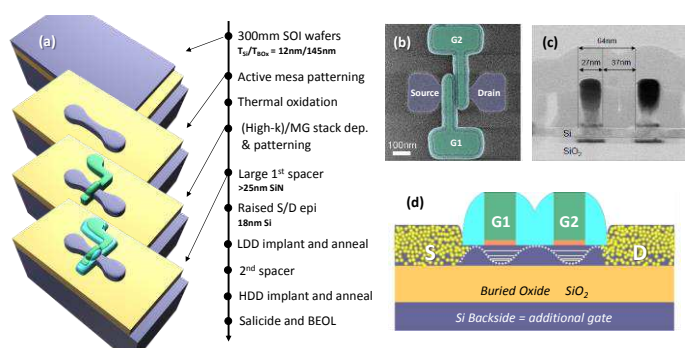


Fig. 1. (a) Simplified process flow of the SOI MOS QD devices with self-aligned reservoir doping. (b) Top view SEM micrograph and (c) transverse cross-sectional TEM view of a two-Gate device. (d) Potential wells are formed below the field-effect Gates, with the wide spacers protecting the inter-Gate regions from doping, thus enabling to define a potential barrier between the QDs.

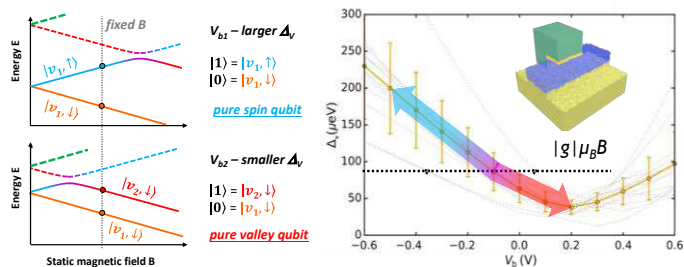


Fig. 2. (Left) Energy diagram showing the Zeeman splitting of the two low-lying valleys in two V_b configurations. Depending on the relative values of the valley splitting (Δ_v) and the Zeeman energy ($E_Z = |g|\mu_B B$) at a given magnetic field B , the qubit can be encoded by a superposition of (long-lived, E-field insensitive) spin or (short-lived, E-field addressable) valley states. (Right) Δ_v vs. applied back-Gate voltage V_b in an SOI corner dot device, including the impact of local surface roughness variability (rms: 0.4nm) [17].

This functionality could alleviate the trade-off between fast manipulation and long coherence time, thereby improving the outlook for compact, scalable and fault-tolerant quantum logic circuits. Considering the valley-splitting-dependent resonance frequency for driving coherent oscillations of the qubit, it is probable that separate back-Gates should be defined in order to calibrate each device to a common operating point.

III. ISOTOPICALLY PURE ^{28}Si THIN FILMS

Hyperfine interactions with nuclear spins in the host crystal can limit the coherence time of an electron spin qubit. The most abundant Si isotope (^{28}Si : 92.23%) carries no nuclear spin, but ^{29}Si (4.67%) does. Increasing the relative ^{28}Si content by has led to some of the best performing single and two-qubit gates [5],[8],[9]. We have grown epilayers with a ^{28}Si isotopic purity greater than 99.992% on 300 mm natural abundance silicon ($^{\text{nat}}\text{Si}$) crystals. The quality of the mono-crystalline isotopically purified epilayer conforms to the same drastic quality requirements as the natural epilayers used in our pre-industrial CMOS facility [18]. Fig. 3 shows the ^{29}Si concentration depth profile in a $^{28}\text{Si}/^{\text{nat}}\text{Si}/^{28}\text{Si}$ stack and its diffusion for various annealing conditions, indicating thermal budget restrictions may be needed during device processing (e.g. dopant activation, wafer bonding), in the case where a $^{\text{nat}}\text{Si}$ seed should remain in the top SOI film.

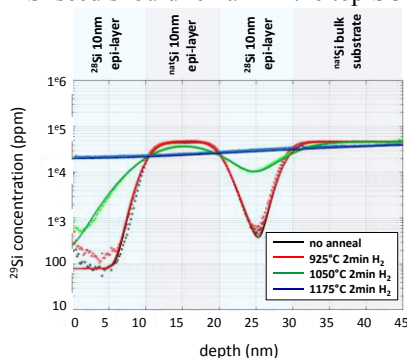


Fig. 3. SIMS data (symbols) and simulation results (lines) of ^{29}Si concentration depth profile vs. annealing conditions in a ^{28}Si 10nm / $^{\text{nat}}\text{Si}$ 10nm / ^{28}Si 10nm / bulk $^{\text{nat}}\text{Si}$ stack [18].

IV. 3D ARCHITECTURES FOR FAULT-TOLERANT COMPUTING

The surface code scheme [19] is nowadays one of the preferred approaches to Quantum Error Correction (QEC) due to its relatively high error threshold. It topologically requires that each individually addressable qubit should be coupled to four adjacent qubits, and hence naturally leads to 2D arrays of coupled QDs. Note that such an arrangement is no longer compatible with a conventional transistor geometry or process flow. Recent architecture proposals have emerged, relying on crossbar addressing of the QDs and tunnel junctions in order to reduce the number of I/Os [20],[21]. Our proposed 3D architecture features two stacked layers of active Si. A large 2D array of QDs is tunnel-coupled by Si pillars to charge-sensing QDs on a lower tier, in order to enable fast initialization and readout [22].

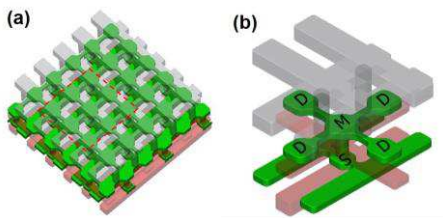


Fig. 4. (a) 3D array of coupled Si QDs and (b) 3D elementary cell composed of six dots; four Data Dots, one Measurement Dot and one Sensing Dot connected to the top tier by a crystalline Si pillar. The topology is designed for the implementation of surface code, with an auxiliary bottom tier for sensing and fast initialization of the charge occupancy in the top tier [22].

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