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► **To cite this version:**

Mohammed Bououd, Yiyu Lai, Adrien Voldoire, Hoang Emmanuel, Olivier Béthoux. Mitigating reverse recovery power losses in MOSFET switching cell using extra Schottky diodes-Application to voltage source inverter. Power Electronic Devices and Components, 2024, 8, pp.100066. 10.1016/j.pedc.2024.100066 . hal-04591673

HAL Id: hal-04591673

<https://hal.science/hal-04591673v1>

Submitted on 29 May 2024

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Mitigating reverse recovery power losses in MOSFET switching cell using extra Schottky diodes—Application to voltage source inverter

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ARTICLE INFO

Keywords:

Reverse recovery
Switching cell
MOSFET
Body/Schottky diode
Stored charge
Voltage source inverter (VSI)

ABSTRACT

This article introduces a comparative study of the losses in Voltage Source Inverter (VSI) based on Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) depending on whether or not the latter are associated with antiparallel diodes. These diodes are optional because MOSFETs have an intrinsic diode capable of conducting reverse currents when their channel is in OFF state. However, it induces additional reverse recovery losses and damaging voltage overshoots. This undesired circumstance occurs during the mandatory switching cell dead-time and is accurately modelled and assessed in this study. Conversely, Schottky diodes feature almost zero reverse recovery losses. Hence, combining each MOSFET with an antiparallel Schottky diode may reduce the converter overall losses. To assess this strategy, an analytical model of the charge stored within the body diode is developed and then compared to experiments using the Double Pulse Test (DPT). It reveals accurate and well suited because it requires only two constant macro parameters which permits to forecast the reverse recovery losses over a wide range of operating conditions, namely switched current, current slope and dead time duration. The selected model is applied in the case where a Schottky diode is placed antiparallel to the MOSFET. It then appears clearly that the interest of such a combination depends on the static characteristics of both the MOSFET and the Schottky diode. This output is a noteworthy point for power electronics designers. Finally, the developed model is applied in the standard use case of the Voltage Source Inverter (VSI). The results reveal the advantage of the suggested model in this use case because the current evolves significantly over time. The outcome of this VSI analysis shows that a significant recovery losses decrease is achieved with good sizing fit between the MOSFET transistor and the additional Schottky diode.

1. Introduction

Within a switching cell, the power transfer management during the dead time between high side (HS) and low side (LS) switch conduction is a key point. The standard solution consists in adding a freewheeling diode in antiparallel with each cell transistor. Whatever the current direction, the additional diodes enable to conduct the output current when the 2 transistors of the cell are simultaneously in OFF state. These extra diodes may be unnecessary using Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technology. Indeed, these transistors have an intrinsic body diode. Their dynamic characteristics are quite poor but are constantly improving with new component designs. The recent advancements are, for instance, innovative packages such as

Quad-Flat No-leads (QFN) which enables using power MOSFETs in low voltage applications (Huesgen, 2022; Ostmann et al., 2009). New technological developments also concern high voltage applications: SiC MOSFETs can now replace IGBT transistors (Han et al., 2022). The growing adoption of MOSFET transistors within switching cells, driven both by their superior high-frequency performance and continuous enhancements in conduction efficiency, therefore enables new antiparallel diode-less switching cell designs for cost reasons.

Despite the fair conduction behaviour of the MOSFET built-in body diode, whether silicon-based (Si) or silicon carbide-based (SiC), it still has a major weak point, namely reverse recovery losses during turn-off (Saro et al., 1998). These reverse recovery losses, due to the bipolar nature of the body diode (Nayak et al., 2020), challenges the economic

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<https://doi.org/10.1016/j.pedc.2024.100066>

Received 5 December 2023; Received in revised form 5 February 2024; Accepted 15 April 2024

Available online 21 April 2024

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advantages of exclusively relying on body diodes for dead time management. Schottky diodes, on the other hand, are very attractive both regarding reverse recovery losses and conduction losses. This superiority therefore explains their use in anti-parallel with MOSFETs (Jahdi et al., 2015), as illustrated in Fig. 1. The objective of their use is clearly to mitigate the reverse recovery effects, i. e. power losses, current spikes, high frequency noise. Brown and Sarlioglu (2015), DeWitt et al. (2009) took the concept one step further by adding a pinch-off circuit that enables all of the current to flow directly into the extra Schottky diode thus eliminating any reverse recovery effect. However, each transistor requires its pinch-off circuit and the related control device, not to mention the additional conduction losses due to a MOSFET transistor in series with the main one. In more conventional approaches, experimental comparisons are performed in Nayak et al. (2020), Ahmed et al. (2017) for high voltage Silicon and SiC MOSFET. Authors in Nayak et al. (2020) introduce a widely used model both based on a switching cell parasitic element model and a reverse recovery waveform. The authors conclude on the benefits of an antiparallel SiC diode with a SiC MOSFET. Other works, as Naseri et al. (2019), use the softness factor S to compute the stored charge, but this parameter is assumed to be constant, while it obviously depends on the current slope and the switched current value (Chernikov et al., 2011; Jovalusky, 2008). Reference Nayak et al. (2022) depicts the influence of temperature on reverse recovery loss in SiC MOSFETs body diode. Authors in Tong et al. (2019) introduce characterization results of switching loss of SiC Schottky diodes, in the particular case of high switching frequencies. Reference Li et al. (2022) proposes a reverse recovery model for PiN diode and how to mitigate these losses using a snubber circuit. Authors in Eskandari et al. (2018) present a body diode reverse recovery model using parasitic capacitances and inductances. Reference Qian et al. (2023) investigates reverse recovery phenomenon for SiC MOSFET body diode in high temperature applications with numerous experimental characterizations. Few studies deal with the behaviour of modern low voltage MOSFET body diode, and analytical models do not usually include physical elements related to the amount of stored charge as a function of current.

The present study aims at assessing the real impact of the reverse recovery losses on the overall switching cell power losses. The objective is to address any operating conditions, evaluating either the case of antiparallel diode-less switching cell or the option of using an additional Schottky diode. Furthermore, the third and main objective is to give practical guidelines for specific load profiles, such as in the case of sine inverter.

In this regard, the present study develops a quick analytical model of power losses in the MOSFET built-in body diode. Such an analytical model, operating whatever the switched current and the current slope imposed by the complementary controlled MOSFET does not exist to the best knowledge of the authors. Consequently, this study develops such a model thoroughly. It is based on physics consideration which enables to

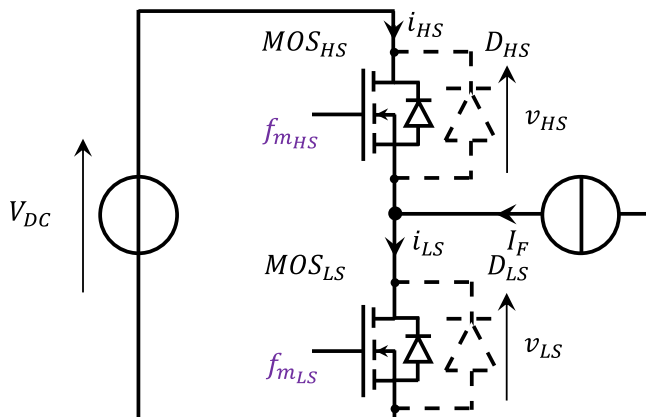


Fig. 1. MOSFET-based switching cell with potential additional Schottky diodes.

easily interpret its results. This model is compared and discussed using both LTspice simulations and experimental tests based on the Double Pulse Test (DPT) (Mondal et al., 2022). This validation step enables to use it in various cases. It permits to highlight that the reverse recovery phenomenon depends on the dead-time value. It mainly contributes to ascertaining the key Schottky diode choice to achieve a significative reverse recovery mitigation in the MOSFET switching cell. This attractive output is confirmed by both DPT and LTspice simulations. Finally, the proposed analytical model is employed in a Voltage Source Inverter (VSI) use case to quantify the losses enhancement achieved by using additional Schottky diodes.

The novelty of this study lies in the use of a new physical analytical model to assess recovery losses in a set of parallel diodes, i.e. body and Schottky diodes. Furthermore, the application of this model to the VSI scenario presents an original challenge due to the large fluctuation of switched current during the low-frequency period. It also permits to address a very common use case, which is a very valuable outcome to the power electronics designer.

This paper is organized as follows. Section 2 recalls the behaviour of a switching cell undergoing a reverse recovery phenomenon due to a PiN diode. It then sets the framework for the current study. Section 3 investigates the physical phenomena involved during a PiN diode recovering while proposing an elementary analytical model of it. Section 4 presents the DPT and explains how the model macro parameters are identified. Section 5 compares the model results with both LTSpice simulations and DPT experiments. It thus validates it. The proposed approach enables to simulate accurately various scenarios whatever current value or current slope. This technique permits to investigate in Section 6 the impact of an additional antiparallel Schottky diode regarding reverse recovery power losses which take place in the switching cell. This issue is addressed comprehensively regarding diodes static characteristics or dead time value. This study enables highlighting the key parameters permitting to achieve a significant power losses enhancement. Section 7 addresses the VSI use case. The suggested model permits to give convincing responses to a case which is one of the main fields of power electronics application. Finally, Section 8 concludes and outlines possible perspectives.

2. Diode recovery in a switching cell - study framework

Forward recovery occurs when a diode goes from the OFF state to the ON state. Reverse recovery occurs when a diode goes from the ON state to the OFF state (Fig. 2). These transitions are associated with losses. Usually, forward recovery losses are negligible while reverse recovery losses induce a significant part of the losses in the diodes (and this even more so as the switching frequency is high). Therefore, this article focuses on the reverse recovery phenomenon. To introduce the two main parameters modelled in this study, this section first describes the case of the ideal diode and then defines that of the PiN diode. By comparison, this enables highlighting the PiN diode additional losses, called diode recovery losses.

2.1. Switching between a MOSFET and an ideal complementary diode

Switching always takes place between a controlled component and a passive one, in this case a MOSFET transistor and a diode. In the case of an ideal diode initially in conduction, the control of the MOSFET gate induces a current rise in the latter. Its slope di_T/dt depends on the gate resistance R_g . Consequently, the diode current decreases with the opposite slope. Considering the latter ideal, its voltage could be considered as zero. Therefore, the transistor supports the entire V_{DC} voltage. Temporarily, the two switches are in OFF state. The transistor imposes a current constraint to the diode while the latter constrains the transistor in voltage. Still under the assumption of an ideal diode, the diode stops conducting the current when it crosses zero. At this precise time, the transistor conducts the forward current I_F flowing through the

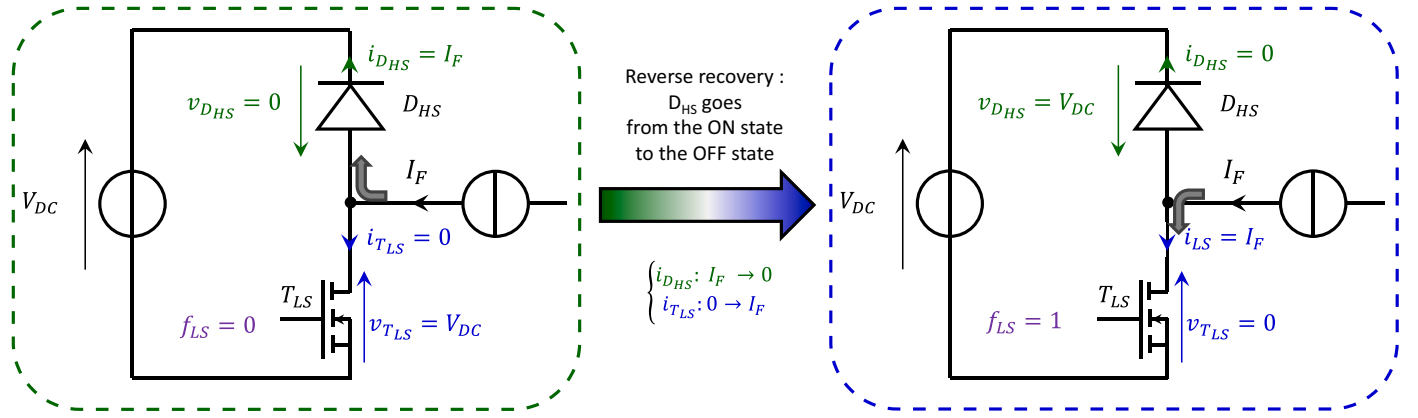


Fig. 2. A diode switching from the ON state to the OFF state.

diode before it turns off. From this moment, the MOSFET turn-on is complete. The corresponding waveforms are given in Fig. 3. It is possible to derive the ideal switching losses. The energy dissipated in the switching cell is given by the following equation:

$$E_{T_{LS},\text{turn-on}}(\text{ideal } D_{HS}) = \frac{V_{DC} \cdot I_F^2}{2 \cdot \left| \frac{di_{T_{LS}}}{dt} \right|} \quad (1)$$

Note that, in real circuits, the switching cell has a parasitic inductance l_s . In this case, part of the MOSFET turn-on energy (i. e. $(1/2) \cdot l_s \cdot I_F^2$) is stored in this inductor. However, this stored energy is then dissipated when the MOSFET turns off.

$$E_{T_{LS},\text{turn-on}}(D_{HS}, l_s) = \frac{V_{DC} \cdot I_F^2}{2 \cdot \left| \frac{di_{T_{LS}}}{dt} \right|} - \frac{l_s \cdot I_F^2}{2} \quad (2)$$

2.2. Switching between a MOSFET and a PiN diode

The ideal diode has a forward voltage of 0 V and a reverse current of 0 A. A real PiN diode induces the same phenomenon, except when the diode current I_D crosses zero, the diode remains in ON state. It still conducts a non-zero current for a duration called the reverse recovery time, and denoted t_{rr} . The latter is defined as the sum of times $t_a = t_2 - t_1$ and $t_b = t_3 - t_2$. Fig. 4 illustrates the associated waveforms. After the current passes through zero, the voltage across its terminals remains zero for a duration t_a and its current decreases to the maximum reverse current $-I_{RM}$ (I_{RM} is called the recovery current). The current in the

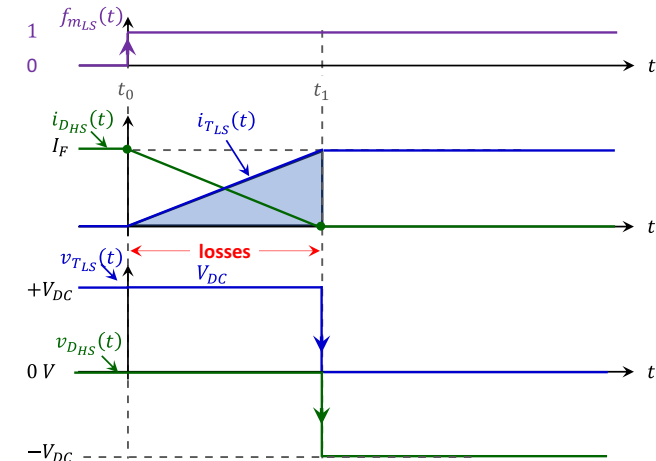


Fig. 3. Currents and voltages waveforms in the case where an ideal diode switches off.

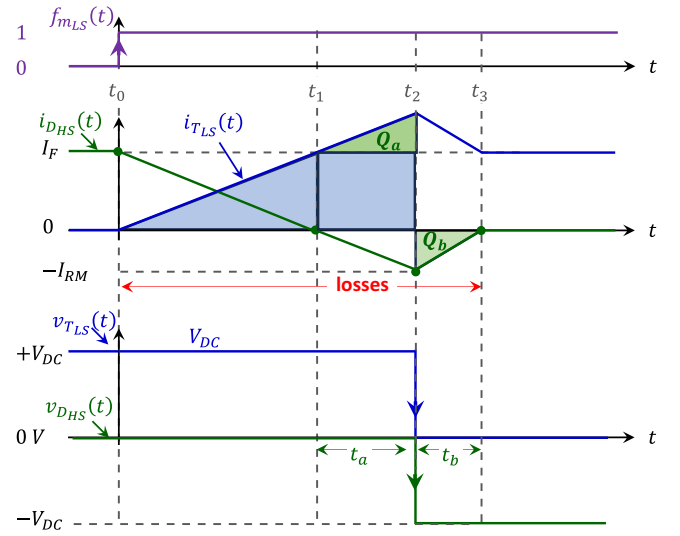


Fig. 4. Currents and voltages waveforms during PiN built-in diode reverse recovery.

transistor therefore rises to a value higher than the forward current I_F , namely $I_F + I_{RM}$. This phenomenon therefore generates additional losses in the transistor MOSFET channel. From this moment, the diode regains its ability to interrupt the current and faces a rapid voltage rise. The latter becomes equal to the DC bus voltage V_{DC} . The current gradually returns to zero over a period t_b : the diode current slope depends on the diode technology. This second phenomenon therefore causes extra losses in the built-in body diode of the MOSFET. Note that these extra power losses during t_a and t_b both occurs in the MOSFETs die active areas and hence contribute to their thermal heating. In unidirectional load current case, it may be important to distinguish between the two types of extra power losses. In sine inverter case, it is no use since thermal issue are low frequency phenomenon. In conclusion, the real energy dissipated in the switching cell, including the turn ON and the reverse recovery phenomena, is given by the following equation:

$$E_{T_{LS},\text{turn-on}}(\text{PiN } D_{HS}) = \frac{V_{DC} \cdot I_F^2}{2 \cdot \left| \frac{di_{T_{LS}}}{dt} \right|} + V_{DC} \cdot I_F \cdot \sqrt{\frac{2 \cdot Q_a}{\left| \frac{di_{T_{LS}}}{dt} \right|}} + V_{DC} \cdot Q_{rr} \quad (3)$$

Where the reverse recovery charge, called Q_{rr} , is defined as the integral of the current flowing through the diode during the time interval

t_{rr} and is thus the sum of the two stored charge Q_a and Q_b : $Q_{rr} = Q_a + Q_b$.

2.3. Relevant parameters to model

The reverse recovery losses are therefore expressed by the difference between Eq. (3) and Eq. (1). Hence the extra losses due to the PiN diode are expressed by:

$$E_{T_{LS},\text{turn-on}}(\text{recovery}) = V_{DC} \cdot \left(Q_{rr} + I_F \cdot \sqrt{\frac{2 \cdot Q_a}{\left| \frac{di_{T_{LS}}}{dt} \right|}} \right) \quad (4)$$

Obviously the reverse recovery losses depend on the two parameters Q_a and Q_b which are intrinsic characteristics of the diode D_{HS} as well as the circuit parameters, namely the bus voltage V_{DC} , the load current I_F and the slope $\left| \frac{di_{T_{LS}}}{dt} \right|$ imposed by the MOSFET control. Moreover, the other characteristics of the switching, i. e. t_a , t_b and I_{RM} , can be deduced from these two values Q_a and Q_b . This is the reason why the study addresses the prediction of these two values, based on a knowledge model, and associated with a very reduced number of experiments.

3. Reverse recovery losses modelling

As described in the previous section, any MOSFET has, by design, an intrinsic body diode, which provides freewheeling capability at zero cost. However, the use of this capability by a switching cell induces a higher current rating and additional losses in its MOSFETs. This can accelerate power converter degradation over time. It is therefore useful to establish the reverse recovery model to understand the use factors which reinforce it and those which reduce it, such as the use of an additional Schottky diode in antiparallel to each MOSFET.

For this purpose, the present study develops a simple knowledge-based model rather than an empirical one. It should both provide a clear connection between inputs and outputs and enable to anticipate the body diode behaviour in many use cases while based on a limited number of experiments.

The MOSFET body diode (Fig. 5), which is basically a PiN diode, is in OFF state when the junction between the p-doped and n-doped regions is depleted of charge carriers, i.e. without electrons or holes. In static conditions, this phenomenon is reinforced by a reverse bias voltage.

In addition to the switched current and the current slope, the doping concentration as well as the geometry of the regions are the key factors affecting the shape of the diode depletion region, either in static or dynamic characterization. Authors in Efthymiou et al. (2016) compare

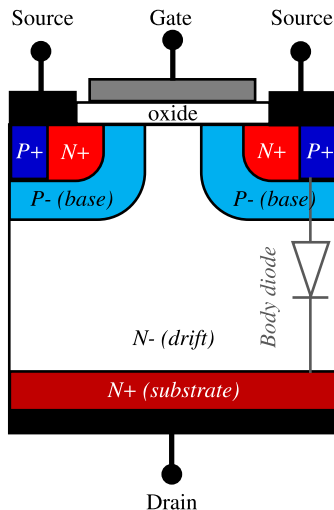


Fig. 5. MOSFET physical construction showing the intrinsic body diode (case of the planar MOSFET technology).

the reverse recovery phenomenon in two Schottky devices, with different doping material (SiC and GaN), and with different depletion region. Simulation and experimental comparisons highlight the differences. A modification of the depletion zone to reduce reverse recovery losses in PiN diodes is reported in Lutz et al. (2009), by compensation of the electric field at the nn+ junction. Authors in Chernikov et al. (2011) propose another way to increase the recovery softness of high voltage diode by proton irradiation during the manufacturing process, which results in a local reduction of life time in n part of layer adjacent to n+.

Conversely, when the MOSFET body diode is in ON state, the current flows both due to holes which are injected from the p-doped region into the n-doped region and similarly to electrons injected from the n-doped region into the p-doped region. These minority carriers have a specific lifetime τ_a which leads to a stored charge $Q_{S,a}$ in the depletion zone as well as an extra stored charge $Q_{S,b}$ in a region close to the depletion layer. These two charges $Q_{S,a}$ and $Q_{S,b}$ are described by the dynamic charge-control equations (Lopez and Alarcon, 2006; Tseng and Pan, 1997; Zhou et al., 2012).

The first one describes the evolution of $Q_{S,a}(t)$ as a function of the forward bias current $i_D(t)$:

$$\frac{Q_{S,a}(t)}{\tau_a} + \frac{dQ_{S,a}}{dt}(t) = i_D(t) \quad (5)$$

It shows two terms. The first one refers to the minority carriers which recombine in the depletion zone, while the second one represents the rate evolution of the depletion store charge. This equation illustrates that the latter is all the larger given that the forward current i_D and the minority carriers' lifetime τ_a are high. It also points out that the steady state occurs after a time roughly three-time larger than τ_a . In other words, the dead-time value may impact the stored charge (Polenov et al., 2009). Similarly, a very fast switching on of the complementary MOSFET leads to a high charge storage at zero current crossing (i.e. at time t_1), which reinforces the reverse recovery phenomenon (large I_{RM} and Q_{rr} values).

The second dynamic charge-control equation expresses the dependency of $Q_{S,b}(t)$ with the forward bias current $i_D(t)$ as follows:

$$\frac{Q_{S,b}(t)}{\tau_a} + \nu_a \cdot \frac{dQ_{S,b}}{dt}(t) = i_D(t) \quad (6)$$

It shows a second macro-parameter denoted ν_a and named the minority carrier viscosity. It acts as a damping factor ranging from zero to one and drives the stored charge $Q_{S,b}$ in the vicinity of the depletion zone. The larger this parameter is, the higher is the electric charge Q_b to be evacuated after the body diode switches to its reverse-biased mode, i. e. at time t_2 .

Time t_0 represents the end of the dead time. The controlled switch MOS_{LS} is turned on and its gate controller imposes a current slope $\left| \frac{di_T}{dt} \right|$, and consequently an opposite body diode current slope: $-\left| \frac{di_T}{dt} \right|$. As this switching slope is very large, the stored charges are gradually reduced between times t_0 and t_1 , but are not set to zero when the body diode current rolls off to zero (time t_1). To obtain the charges Q_a and Q_b which remain to be evacuated and which condition the value of the additional losses due to the recovery phenomenon, it is therefore necessary to solve the following system of differential equations on the interval $t \in [t_0, t_1]$:

$$\begin{cases} \frac{Q_{S,a}(t)}{\tau_a} + \frac{dQ_{S,a}}{dt}(t) = I_F - \left| \frac{di_T}{dt} \right| \cdot t \\ \frac{Q_{S,b}(t)}{\tau_a} + \nu_a \cdot \frac{dQ_{S,b}}{dt}(t) = I_F - \left| \frac{di_T}{dt} \right| \cdot t \end{cases} \quad (7)$$

Solving this equation gives the following temporal evolution for $Q_{S,a}(t)$ and $Q_{S,b}(t)$:

$$\begin{cases} Q_{s,a}(t) = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[1 - \frac{t}{\tau_a} - \exp\left(-\frac{t}{\tau_a}\right) \right] \\ Q_{s,b}(t) = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[\nu_a - \frac{t}{\tau_a} - \nu_a \cdot \exp\left(-\frac{t}{\tau_a \cdot \nu_a}\right) \right] \end{cases} \quad (8)$$

Time t_1 is defined by:

$$t_1 = \frac{I_F}{\left| \frac{di_T}{dt} \right|} \quad (9)$$

Hence the two stored charges to be extracted from the intrinsic diode are:

$$\begin{cases} Q_a = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[1 - \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} - \exp\left(-\frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|}\right) \right] \\ Q_b = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[\nu_a - \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} - \nu_a \cdot \exp\left(-\frac{I_F}{\tau_a \cdot \nu_a \cdot \left| \frac{di_T}{dt} \right|}\right) \right] \end{cases} \quad (10)$$

The latter equation represents the developed diode reverse recovery model. It is based on two analytic expressions that have the advantage of mathematical simplicity. Moreover, this approach has the benefit of relying on fundamental laws of physics and of limiting the use of data while being based on only two macro-parameters, namely τ_a and ν_a . The following section aims first to determine the latter with a basic experiment and then to validate the developed model.

The following hypotheses have to be taken into account before using the developed model :

- The developed model can be used for PiN diodes and MOSFET body diodes.
- The influence of temperature is not taken into account in the model. References [Nayak et al. \(2022\)](#) and [Jovalusky \(2008\)](#) specifically propose models for this influence.
- Reverse recovery losses are proportional to the switched voltage value.
- Minor carriers evolution is assumed exponential.

4. Experimental validation setup and models' parameters identification

To ensure the proposed approach credibility, an experiment setup has been developed. It is basically a Double Pulse Test (DPT) system ([Mondal et al., 2022](#)). This device is widely accepted in the field of power electronics ([Schweickhardt et al., 2021](#)) to characterize and assess the switching performance of semiconductor devices like diodes and transistors. Specifically, it is first used to determine the two macro parameters that the developed model put forward. In a second step ([Section 5](#)), it enables to validate the analytical model using various test conditions, i.e. various forward current I_F and different commutation speeds $|di_T/dt|$. Finally, [Section 6](#) uses it to confirm the analysis of the impact of adding a Schottky diode in parallel with the body diode.

4.1. Experimental setup

The experimental DPT setup and the related electrical diagram are presented in [Fig. 6](#) where the printed circuit (PCB) and the measuring probes can be seen. The basic switching cell is configured such as the high-side MOSFET channel is controlled to be open while the low-side MOSFET is driven by two pulses separated by a dead time. Indeed, with a gate-source voltage forced to zero voltage, the high-side transistor behaves as a body diode. Setting the first pulse duration enables to adjust the current source current value I_F . At the end of this first pulse, the body diode of the high-side MOSFET enables a freewheeling mode.

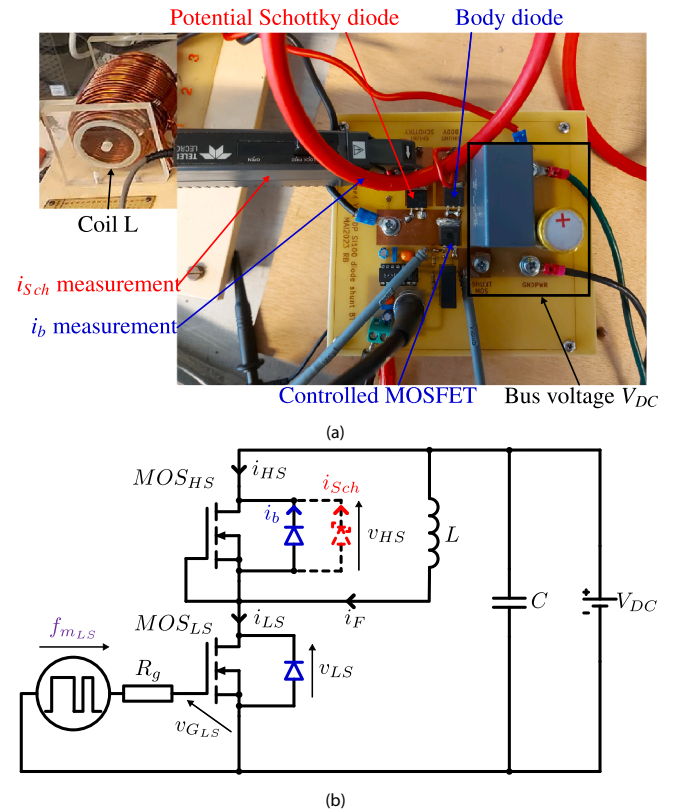


Fig. 6. Experimental setup developed in GeePs laboratory to experiment Double Pulse Test (DPT): (a) A picture of the Printed Circuit Board (PCB) and the measuring system; (b) The related electric diagram.

This sequence ends with the second pulse which enforces hard switching during which the reverse recovery phenomenon described above occurs. The current slope of this second phase is tuned by adjusting the gate resistance value R_g of the low-side MOSFET ([Teng et al., 2020](#)).

Technically, the tested component is the (100V, 137A) MOSFET IPB042N10N3 produced by Infineon manufacturer.

4.2. Model-specific parameter set identification

The DPT was performed in a single operating condition. Analysing the body diode current evolution over time enables to extract the two measured stored charge $Q_{a,m}$ and $Q_{b,m}$ and then to derive both parameters τ_a and ν_a .

4.2.1. Extracting $Q_{a,m}$ and $Q_{b,m}$ from a DPT Measurement

[Fig. 7](#) shows, in dark green solid line, the experimental measurements of current $i_{D,HS}(t)$ based on the practical tested switching cell. During the last time interval t_b of the reverse recovery phenomenon, the body diode current oscillates at roughly 8.5 MHz around the zero current value before stabilizing. These oscillations result from an exchange of reactive energy between the parasitic inductance of the commutation loop and the junction capacitance of the turned off body diode ([Kang et al., 2012](#)). Even if it does not directly impact the charge $Q_{a,m}$ assessment, it strongly disturbs the charge $Q_{b,m}$ estimation.

To address this issue, several techniques could be used ([Kang et al., 2012](#); [Kumar et al., 2017](#); [Makaran, 2015](#)). The present study focuses on the approach developed in [Kang et al. \(2012\)](#) because it finally turns out to be very effective. The strategy consists in comparing the actual measurement, that is to say taking into account the stray inductance, the junction capacitance and a resistor representing the recombination of charge carriers in the diode as well as the parasitic losses in the circuit, with an ideal scenario where the commutation loop inductance is

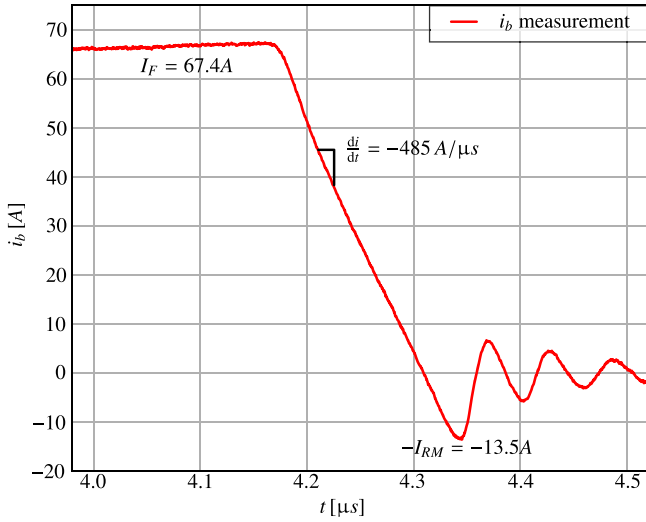


Fig. 7. Measured body diode current i_b during the turn-off, without using an additional Schottky diode.

negligible. This comparison enables to extract the theoretical curve of the current $i_{D,HS}(t)$ while the body diode switches off, as depicted in black dashed line in Fig. 8. Subsequently, it enables to derive, by integration, the recovered charges Q_a and Q_b that were actually stored in the semiconductor structure of the body diode. This strategy is used for specific values of I_F and $|di/dt|$ and proves invaluable for identifying the model parameter set as presented in the following sub-section.

4.2.2. Models' parameters identification

For a test on the body diode of the MOSFET IPB042N10N3 at $I_F = 20A$ and $di/dt = -223A/\mu s$, the charges $Q_{a,m}$ and $Q_{b,m}$ were computed using the outlined method above. This enables to obtain the two following values:

$$(Q_{a,m} = 106 nC ; Q_{b,m} = 56 nC) \quad (11)$$

By injecting the value of $Q_{a,m}$ into the equation (Eq. (12)), it is possible to compute the value of the average lifetime of the minority carriers of the body diode.

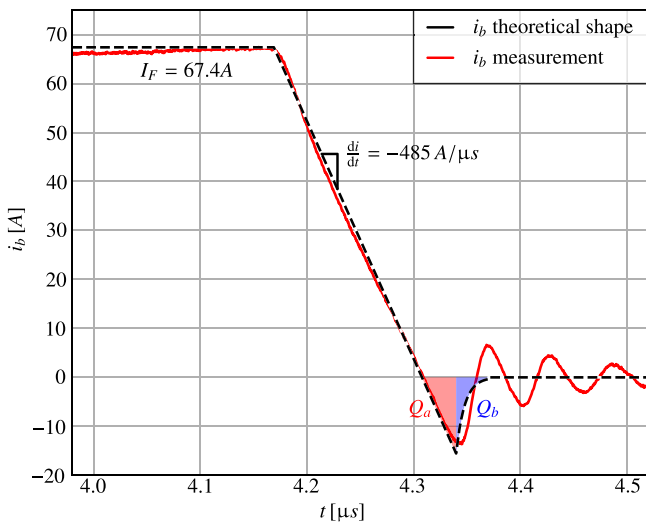


Fig. 8. Theoretical current curve i_b achieved by postprocessing the DPT measurement showing oscillations (method detailed in Kang et al. (2012)).

$$Q_{a,m} = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[1 - \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} - \exp \left(- \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} \right) \right] \quad (12)$$

After this step, using the values of $Q_{b,m}$ and τ_a enables to deduce the value of the second coefficient ν_a from the equation (Eq. (13)).

$$Q_{b,m} = \tau_a \cdot I_F + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \cdot \left[\nu_a - \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} - \nu_a \cdot \exp \left(- \frac{I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} \right) \right] \quad (13)$$

Finally, this calculation process enables to obtain the set of parameters of the MOSFET body diode, namely:

$$\begin{cases} \tau_a = 22ns \\ \nu_a = 0.52 \end{cases} \quad (14)$$

Although the parameter set is identified based on a single experiment, the obtained parameters remain constant since the junction temperature impact is not considered in this study. The constant parameter set will be used in the following sections, while modifying the switching current value I_F or the current slope $|di_{HS}/dt|$. The same applies when using an additional Schottky diode in parallel with the MOS_{LS} .

Using the softness factor, usually provided by manufacturers of PiN diodes and MOSFETs, would have been another way of estimating Q_b without the other way. Softness factor S is a parameter sometimes given by diode manufacturers. It is defined as:

$$S = \frac{t_b}{t_a} \quad \text{with} \quad t_{rr} = t_a + t_b \quad (15)$$

Unfortunately, as this parameter is not given for the considered body diodes, it is not possible to apply this simple model. In addition, for PiN diode, the softness factor value is usually constant, and does not consider the variation of switched current or current slope.

This result is attractive because it enables to overcome the "softness factor" generally provided in the datasheets by the manufacturers of PiN diodes and MOSFETs (Chernikov et al., 2011). Indeed, the softness factor strongly depends on the operating conditions (current, current slope, etc.) and it would be necessary to map all the possibilities of using the MOSFET to be able to use it. This parameter rather enables the designer a relative choice of one component compared to another.

5. Models validation

In this section, the proposed model is validated by both simulation and experimental measurements.

5.1. Validation of models through LTspice simulations

Simulations are conducted using the LTspice software to validate the new reverse recovery model proposed in Section 3. A comparison is made with LTspice's built-in reverse recovery model, which uses a dynamic approach as outlined in reference (Tseng and Pan, 1997).

The circuit shown in Fig. 9 is considered for the simulation. During the dead time, when the ideal switch K is OFF, a DC current source enforces the current I_F through the simulated body diode of the Si MOSFET IPB042N10N3. When the switch K is triggered, the current in it increases with a slope $|di/dt|$ set by the inductance l_μ according to Eq. (16). According to Kirchhoff law, the current in the diode decreases with the opposite slope $-|di/dt|$, which ultimately leads to a reverse recovery phenomenon.

$$\frac{di}{dt} = - \frac{V_{DC}}{l_\mu} \quad (16)$$

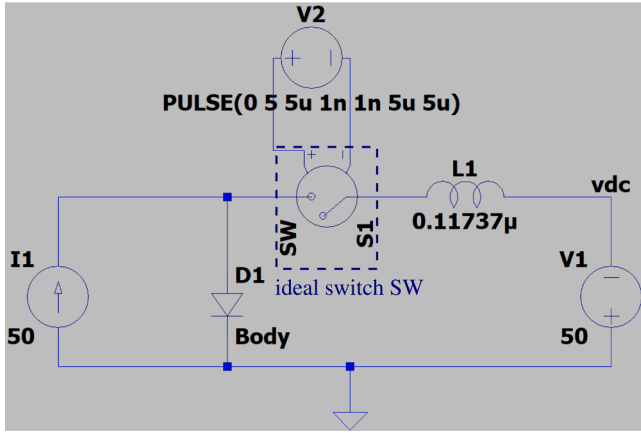


Fig. 9. LTspice Diagram of the Double Pulse Test.

The inductance l_i models the effect of the whole switching environment, including the gate resistance R_g and the stray inductance l_s of the DPT circuit. In this simulation circuit, the diode model includes the transit time TT and the viscosity v_p , with the values identified previously. TT and v_p , explained in Tseng and Pan (1997), are crucial parameters in LTspice to model the recovered charges Q_a and Q_b . According to the developed model and Tseng and Pan (1997), the estimated values for these parameters are determined as follows:

$$\begin{cases} TT = 30.5ns \\ v_p = 0.3 \end{cases} \quad (17)$$

Tests are carried out with different values of switched current I_F and different values of current slope di/dt , in order to reproduce different operating conditions. The reverse recovered charge Q_{rr} is measured by the charge extraction method (Kang et al., 2012). The simulation result is compared to the proposed model (with coefficient v_a) in Fig. 10.

Root Mean Square Error (RMSE) is chosen as a relevant parameter to compare the accuracy of the two models with the simulation (see Fig. 10). RMSE calculation is given in Eq. (18).

$$RMSE_{Q_{rr}} = \sqrt{\frac{\sum_{i=1}^N (Q_{rr(model)_i} - Q_{rr(sim)_i})^2 / N}{\sum_{i=1}^N Q_{rr(sim)_i}^2 / N}} \quad (18)$$

With a RMSE of 7% and 8%, the proposed model shows an overall correct accuracy. It can be noted that the proposed model overestimates slightly the stored charge when the switched current is low, but gives an accurate evaluation for high current values. This accuracy is possible because of the introduction of the viscosity parameter. Better results could be achieved for low current by refining the method of evaluation of the viscosity.

5.2. Proposed model experimental validation

In this second validation step, the results of the model are compared to the measurements of the experimental test bench enabling to carry out the Double Pulse Test. The Si MOSFET IPB042N10N3 is implemented with a zero gate voltage to use its body diode. The measurements from the experiment are also displayed in Fig. 10, and compared to the previous results from models and simulation. The gate resistance value R_g is modified to perform the two sets of measurements with two current slope values di/dt . It is worth mentioning that a current slope value di/dt variation is observed during the tests. Consequently, the mean value is used for all calculations.

Fig. 10 reveals few impacts of the value of switched current on the amount of stored charge for high switched current values. Indeed, for high switched current values, the depletion zone is completely saturated. Then, no more charge can be stored. On the other hand, for low values of switched current, results reveal a strong dependence of the stored charge with the current value. This can be explained by the models depicted in Eqs. (5) and (6), leading to an exponential increase of the amount of stored charge with the current.

The RMSE between the experiment and the model is 12% and 13% for the two di/dt values. Considering that the minimum error induced by the test bench is 5%, and considering the previous error of 7% and 8% between model and simulation, this difference of 12% and 13% is understandable. Measurements difficulties, induced by the high di/dt and low switched voltage, can explain some volatility on the results. However, the experimental curve shape matches the model, with a RMSE

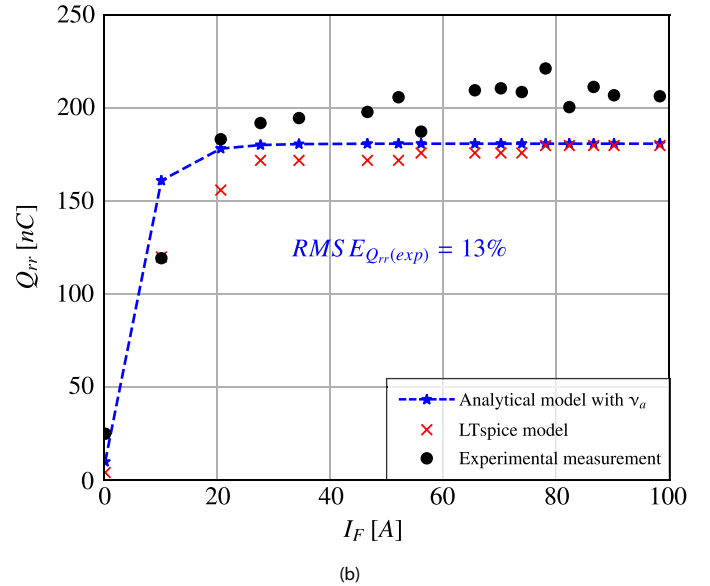
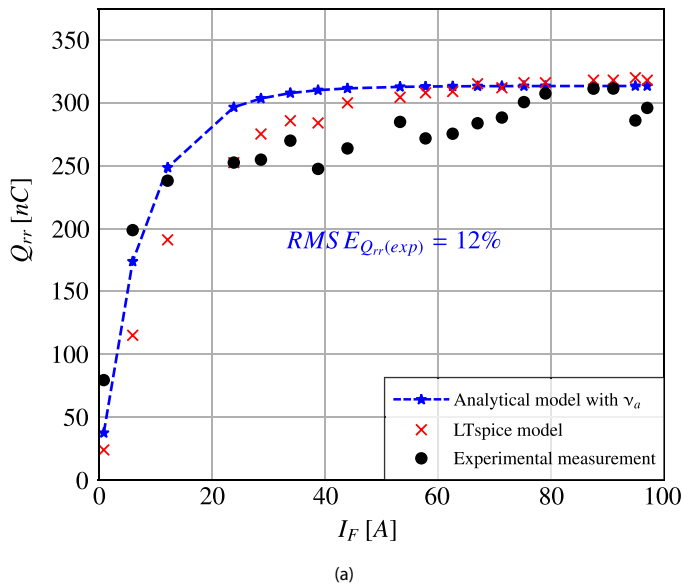


Fig. 10. Reverse recovered charge Q_{rr} as a function of the forward current I_F using the DPT experiment (shown by black points), LTspice simulation (illustrated by red crosses), and the analytical model based on the coefficient v_a factor (illustrated by a blue dashed line) for two current slope values: (a) current MOSFET slope value $di_T/dt = -426 A/\mu s$ using $R_g = 1.4 \omega$ and (b) current MOSFET slope value $di_T/dt = -246 A/\mu s$ using $R_g = 122 \omega$

judged as acceptable, because the advantage of the developed model is not on the accuracy. The advantage relies more on its ability to take into account easily different switched current, which is mandatory for the targeted case : the Voltage Source Inverter.

This analysis enables the validation of the model for different switched current and di/dt , which is the targeted goal.

5.3. Conclusion of the model validation phase

Validations using LTspice simulations, as well as experimental validation, demonstrate the accuracy of the proposed model. The introduced coefficient μ_a shows less dependency on the problem's given data (I_F and di/dt) and manages to describe the variation of the recovered charge Q_r as a function of the problem's data with an error limited to 13%. The test conditions, especially the pronounced oscillations in the current curve and the fluctuation of the current slope, permit the acceptance of this error for the proposed model.

The following limitations also have to be considered using the developed model:

- The model is not suitable for Schottky diodes.
- As the influence of temperature is not taken into account in the model, users should consider a constant junction temperature. Otherwise, users could extrapolate results from references [Nayak et al. \(2022\)](#), [Jovalusky \(2008\)](#) or [Eskandari et al. \(2018\)](#) in order to take into account this influence.
- The model needs to be fed by simulation or experimental data. Simulation data can be obtained in Spice based software considering precise data given by the manufacturer. Experimental data can be obtained with a test bench, such as a Double Pulse Test, an opposition method, or calorimetric test bench.

The next phase of this study uses this model to evaluate the impact of dead time duration as well as the effect of using a Schottky diode in parallel on the MOSFET.

6. Impact of Schottky diode and dead time duration on reverse recovery losses

The study of the recovery phenomenon has shown that the additional losses generated strongly depend on the operating conditions of the intrinsic diode of the MOSFET. The present section studies two situations more specifically. The first consists in reducing the dead time to limit the charge stored by the diode. The second is to reduce the current flowing through the intrinsic diode by adding a Schottky diode in parallel to the MOSFET. This action should also reduce the stored charge.

6.1. Impact of the dead time duration on reverse recovery losses

The intrinsic body diode is governed by the fundamental laws of physics (Eqs. (5) and (6)) explained in Section 3. In conduction mode, the minority charge carriers gradually accumulate in the depletion zone. The stored charge evolves dynamically with a time constant τ_a , namely minority carriers' specific lifetime. Hence, the stored charges Q_a and Q_b strongly depend on the conduction time t_{dt} (i.e. the dead time duration) when the latter is less than τ_a or of the order of a few τ_a . With current technologies, this pivot duration is about few tens of ns. Conversely, for dead time duration significantly larger than τ_a , the stored charges saturate at their steady state value, i.e. $Q_\infty = \tau_a \cdot I_F$.

Note that Sections 3 and 4 assume a steady state at the end of the dead time. Broadly speaking, it is mandatory to consider any dead time value and therefore recompute the true stored charges Q_a and Q_b when the diode current crosses zero (i.e. at time t_1). Eq. (10) is thus modified for a more general expression. Considering a constant value I_F during the dead time, the stored charges at the end of it are derived from Eqs. (5) and (6). It enables to obtain the initial values of the reverse recovery

phenomenon (i.e. at time t_0):

$$\begin{cases} Q_{a,init} = \tau_a \cdot I_F \cdot \left[1 - \exp\left(-\frac{t_{dt}}{\tau_a}\right) \right] \\ Q_{b,init} = \tau_a \cdot I_F \cdot \left[1 - \exp\left(-\frac{t_{dt}}{\nu_a \cdot \tau_a}\right) \right] \end{cases} \quad (19)$$

These values are then used to estimate the generalized expression of Eq. (10). The stored charges are computed with respect to the dead time value on which $Q_{a,init}$ and $Q_{b,init}$ depend explicitly.

$$\begin{cases} Q_a = \left(Q_{a,init} - \tau_a \cdot I_F - \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \right) \cdot \exp\left(\frac{-I_F}{\tau_a \cdot \left| \frac{di_T}{dt} \right|} \right) + \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \\ Q_b = \left(Q_{b,init} - \tau_a \cdot I_F - \nu_a \cdot \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \right) \cdot \exp\left(\frac{-I_F}{\nu_a \cdot \tau_a \cdot \left| \frac{di_T}{dt} \right|} \right) + \nu_a \cdot \tau_a^2 \cdot \left| \frac{di_T}{dt} \right| \end{cases} \quad (20)$$

Fig. 11 illustrates the impact of the dead time value on the reverse recovery losses. It shows the global reverse recovered charge Q_r computed using the above expressions (Eq. (20)) as a function of the diode forward current I_F for various values of t_{dt} . The MOSFET *IPB042N10N3*, characterized by ($\tau_a = 22ns$, $\nu_a = 0.52$) is still considered. This simulation points out that for small dead time values with respect to τ_a , the global reverse recovery charge (Q_r), which is a key device parameter for hard commutation ruggedness, exhibits a significant decrease signifying a substantial reduction in reverse recovery losses. However, for larger values of dead time, the influence of dead time diminishes. However, for higher values of dead time, the influence of dead time decreases, which corresponds to the above discussion. The charge storage process reaches a finite steady state at the end of a large dead time.

To sum up this subsection, dead time emerges as a potential parameter permitting to reduce reverse recovery losses. Its full use faces the switching cell safety requirement. Indeed, a large dead time avoids any highly undesired switching cell transient short circuit. It is for that reason that an external Schottky diode use is also considered in the next sub-section.

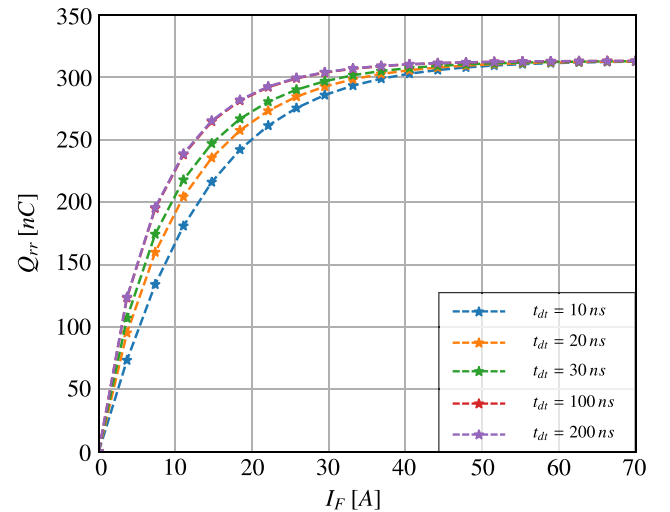


Fig. 11. Reverse recovered charge Q_r as a function of the forward current I_F in the studied body diode for various values of dead time t_{dt} (10ns, 20ns, 30ns and 100ns and perhaps 200ns) and respecting a constant current slope imposed by the complementary controlled transistor: $-426A\mu s$.

6.2. Impact of the Schottky diode on losses

The Schottky diode use aims at reducing the global recovery charge Q_{rr} and hence the recovery extra losses. Simulation studies have evaluated the addition of a Schottky diode in parallel with a MOSFET structure (Kong et al., 2021). These studies have demonstrated significant gains in terms of recovery losses while keeping standard switching losses constant. Furthermore, more specific experimental research on the parallel connection of discrete components has also highlighted these gains, while pointing out minor disturbances in classical switching losses due to the overall increase in junction capacitance (Nayak et al., 2020). The present study intends to both validate experimentally the impact of the Schottky diode use and provide additional and more detailed explanations. It is based on the previous development and the experimental DPT setup using the IPB042N10N3 MOSFET in combination with the RBQ30NS100A (100V, 100A) Schottky diode.

6.2.1. Body and Schottky diodes parallelisation modelling

The study assumes that the extra Schottky diode has no reverse recovery losses and that the body diode reverse recovery losses depend on the parameters I_F and $|di_b/dt|$ as computed and experimented in Section 4. Hence, the challenge is to define current distribution during the dead time between the intrinsic body diode and the extra Schottky diode. During the dead time, the load current I_F is distributed between both diodes based on the Kirchhoff's laws. Referring to Fig. 12, the intrinsic body diode current is expressed as:

$$\begin{cases} i_b = 0 & \text{if } I_F \leq \frac{V_b - V_{Sch}}{R_{Sch}} \\ i_b = I_F & \text{if } I_F \leq -\frac{V_b - V_{Sch}}{R_b} \\ i_b = \left(\frac{R_{Sch}}{R_b + R_{Sch}}\right) \cdot I_F - \frac{V_b - V_{Sch}}{R_b + R_{Sch}} & \text{otherwise} \end{cases} \quad (21)$$

Thus, the related intrinsic diode current slope is:

$$\begin{cases} \left|\frac{di_b}{dt}\right| = 0 & \text{if } I_F \leq \frac{V_b - V_{Sch}}{R_{Sch}} \\ \left|\frac{di_b}{dt}\right| = \left|\frac{di_T}{dt}\right| & \text{if } I_F \leq -\frac{V_b - V_{Sch}}{R_b} \\ \left|\frac{di_b}{dt}\right| = \left(\frac{R_{Sch}}{R_b + R_{Sch}}\right) \cdot \left|\frac{di_T}{dt}\right| & \text{otherwise} \end{cases} \quad (22)$$

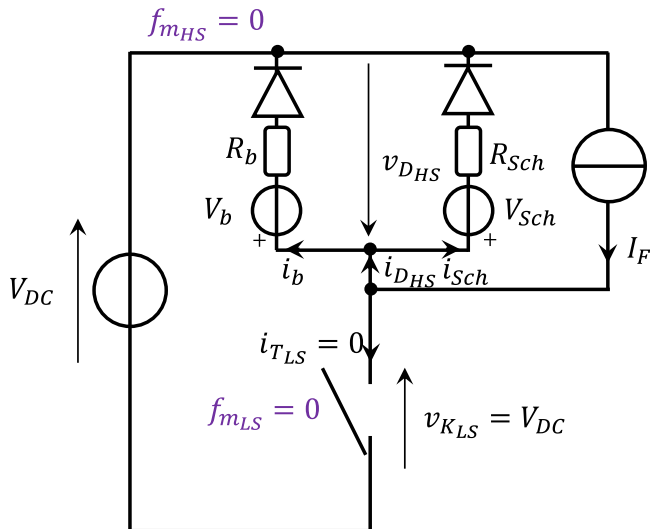


Fig. 12. Modelling of the current distribution between the body diode and the Schottky diode during dead time.

Usually, Schottky diodes have also lower threshold voltage than body diodes. Hence, the term $(V_b - V_{Sch})$ is always positive. Consequently, the second case rarely happens.

Similarly, the Schottky diode current is expressed as:

$$\begin{cases} i_{Sch} = I_F & \text{if } I_F \leq \frac{V_b - V_{Sch}}{R_{Sch}} \\ i_b = 0 & \text{if } I_F \leq -\frac{V_b - V_{Sch}}{R_b} \\ i_{Sch} = \left(\frac{R_b}{R_b + R_{Sch}}\right) \cdot I_F + \frac{V_b - V_{Sch}}{R_b + R_{Sch}} & \text{otherwise} \end{cases} \quad (23)$$

Based on these expressions, the charges Q_a and Q_b can therefore be calculated using either on the Eqs. (12), (13) (dead time large compared to τ_a) or on the Eq. (20) (dead time of the order of τ_a).

6.2.2. Experimental validation of the reverse recovery model using an extra Schottky diode

To experimentally validate the previous model, the Double Pulse Test is used with the Schottky diode implementation. The currents in both diodes (i_b and i_{Sch}) during dead time and reverse recovery, are measured and depicted in Fig. 13. This first shows that the Schottky diode has almost no current after it passes zero. It therefore validates the initial assumption according to which the Schottky diode faces almost no reverse recovery loss. Second, the chosen current divider model during the dead time ($i_b = 37.6A$ and $i_{Sch} = 21.4A$ for a total current $i_F = i_{tot} = 59A$) is quite accurate because the model results indicate: $i_{b(model)} = 32.7A$ and $i_{Sch(model)} = 26.3A$ (Table 1). Third, it also reveals that the choice of the body and Schottky diodes combination has to be made carefully. Indeed, in this occurrence, the global current I_F is distributed 64% in the body diode and 36% in the Schottky one which is a rather worst-case scenario for reducing extra switching losses.

The global reverse recovery charge Q_{rr} is measured following the previous described method (Section 4). It is also calculated using the analytical model developed in Section 6.2.1 while using an extra Schottky diode. It enables the model predictions to be compared with experimental measurements, as demonstrated in Fig. 14. Additionally, the same figure includes the theoretical model without the Schottky diode to outline the reduction in the reverse recovery losses achieved using an additional Schottky diode. Note that this model was previously validated in Section 4. Calculating the root mean square error (RMSE)

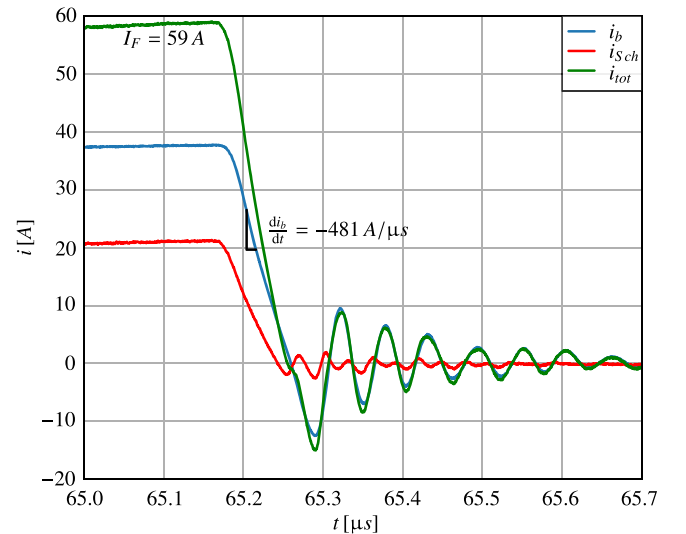


Fig. 13. Reverse recovery phenomenon at the end of the dead time while using an extra Schottky diode. Current in the body diode shown by the blue line, Schottky diode shown by the red line, and total current (sum of both) shown by the green line.

Table 1
Datasheet-based modeling of body diode and Schottky diode.

Body diode <i>IPB042N10N3</i>	$V_b = 0,54 \text{ V}$	$R_b = 7 \text{ m}\Omega$
Schottky diode <i>RBQ30NS100A</i>	$V_{Sch} = 0,4 \text{ V}$	$R_{Sch} = 14 \text{ m}\Omega$

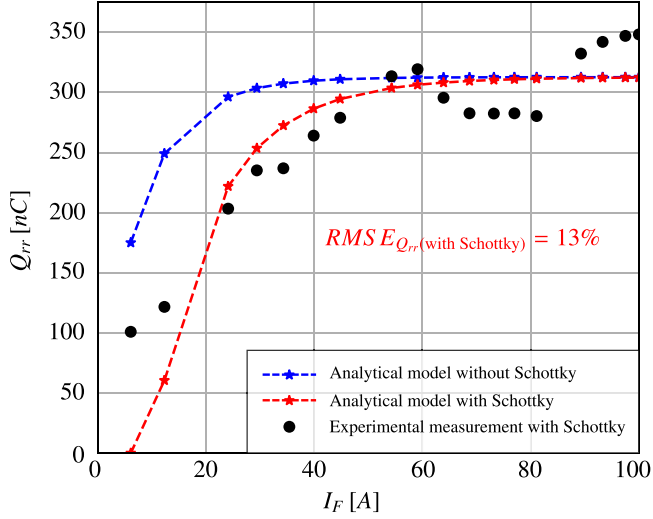


Fig. 14. Reverse recovered charge Q_{rr} in the body diode using an additional Schottky diode as a function of the forward current I_F . Respecting an average transistor current slope value $di_b/dt = -416 \text{ A}/\mu\text{s}$, the data computed with the developed analytical model are shown in the dashed red line and compared with the experimental measurement illustrated by the black points.

between the results of the analytical model and the experimental measurements gives an error of 12%, which corresponds to a value similar to the one computed for the reverse recovery loss model in a single body diode. This demonstrates that the current divider model accurately describes the impact of the Schottky diode on the current flowing through the body diode in these tests, where a large dead time value (on the order of $2\mu\text{s}$) is used.

Fig. 14 reveals that adding a Schottky diode across a body diode does not change the amount of stored charge in the body diode for high values of switched current. Indeed, even if the Schottky diode derives a significant part of the global current, the depletion zone is eventually saturated. Nevertheless, it requires a higher global current compared to the case without Schottky diodes. For low current values, the experiments and simulations reveal a drastic gain on the body diode recovery losses. This can be explained by two reasons. First, as the current is divided into two paths within the same dead time, the amount of stored charge in the body diode is lower. Second, as the Schottky threshold voltage is lower than the body diode threshold voltage in the selected example, current passes mainly in the Schottky rather than in the body for low current values. It should be noted that this analysis strongly depends on the characteristics of the two components.

7. Model practical implementation: reverse recovery losses in the 3-phase voltage source inverter use case

As shown in the previous sections, the variation of reverse recovery losses is non-linear with respect to the output current value. This statement makes unclear the real benefit of using an additional Schottky diode in the case of a specific mission profile. This section intends to address this issue, particularly relevant to power electronics designers. The MOSFET 3-phase Voltage Source Inverter (VSI) is chosen as a case study because it is widely used for various application such as motor drive systems or photovoltaic AC grid connection. This section is divided in three parts. First, the reverse recovery model developed previously is

applied in the VSI case, considering low frequency current variations. Second, the use of an extra set of Schottky diodes is considered and the related losses reduction is comprehensively assessed. Finally, several MOSFET - Schottky diode combinations are considered and discussed with respect to the ability to mitigate reverse recovery phenomenon.

7.1. Reverse recovery loss model

In a MOSFET 3-phase VSI, the reverse recovery phenomenon occurs either in the high-side or the low-side body diodes depending on the sign of the output current value. Indeed, when the load current is positive, reverse recovery occurs in the low-side diode. Conversely, a negative load current induces a reverse recovery phenomenon due to the high-side diode. As previously explained, this reverse recovery phenomenon is triggered when the complementary MOSFET is switched ON at the end of the dead time protecting each switching cell from a transient short-circuit. **Fig. 15a** and **b** illustrate this chronological sequence for a positive and negative load current, respectively. Note also that these figures show a single switching cell of a 3-phase VSI. Obviously, the other two behave similarly.

The load current exhibits a low frequency sinusoidal behavior. Hence, to assess the converter thermal behavior, it is necessary to compute the average reverse recovery losses over a VSI electrical period. The reverse recovery losses P_{rr} of a 3-phase VSI can be expressed as follows:

$$P_{rr} = 3 \cdot F_m \cdot \sum_{n=1}^m E_{rr} \left(\theta = \frac{2\pi n}{m} \right) \quad (24)$$

where

- F_s represents the switching frequency of the inverter,
- m denotes the modulation index which is calculated as the ratio of the carrier signal frequency F_s to the modulation signal frequency F_m ,
- E_{rr} refers to the reverse recovery energy of a single cell switching period, which occurs when the electric angle of the charging current θ is equal to $2\pi n/m$.

Technically, the fundamental harmonic of the first phase voltage, driven by the modulation function of the VSI, is expressed as follows:

$$v_L(\theta) = \hat{V} \sin(\theta) \quad (25)$$

In the common case where the switching harmonics are effectively filtered by the inductive load, the phase current is properly approximated by a sinusoidal time function with a phase shift ϕ relative to the phase voltage:

$$i_F(\theta) = \hat{I} \sin(\theta - \phi) \quad (26)$$

Substituting **Eqs. (4)** and **(26)** into **Eq. (24)** results in the reverse recovery losses model of a standard 3-phase VSI.

$$P_{rr} = 3 \cdot F_m \cdot \sum_{n=1}^m \left[V_{DC} \cdot \left(Q_{rr} \left(\theta = \frac{2\pi n}{m} \right) + I_F \sqrt{\frac{2 \cdot Q_{rr} \left(\theta = \frac{2\pi n}{m} \right)}{a \left(\theta = \frac{2\pi n}{m} \right)} \frac{di_{FS}}{dt}} \right) \right] \quad (27)$$

This model has to be compared to the one of the 3-phase VSI using extra Schottky diodes to determine the losses mitigating potential of the latter.

7.2. Power losses reduction through Schottky diode implementation

As described in **Section 6**, Schottky diode enables to mitigate the switching cell reverse recovery losses. It also helps reducing conduction losses during the switching cell dead time, by adding a second path for

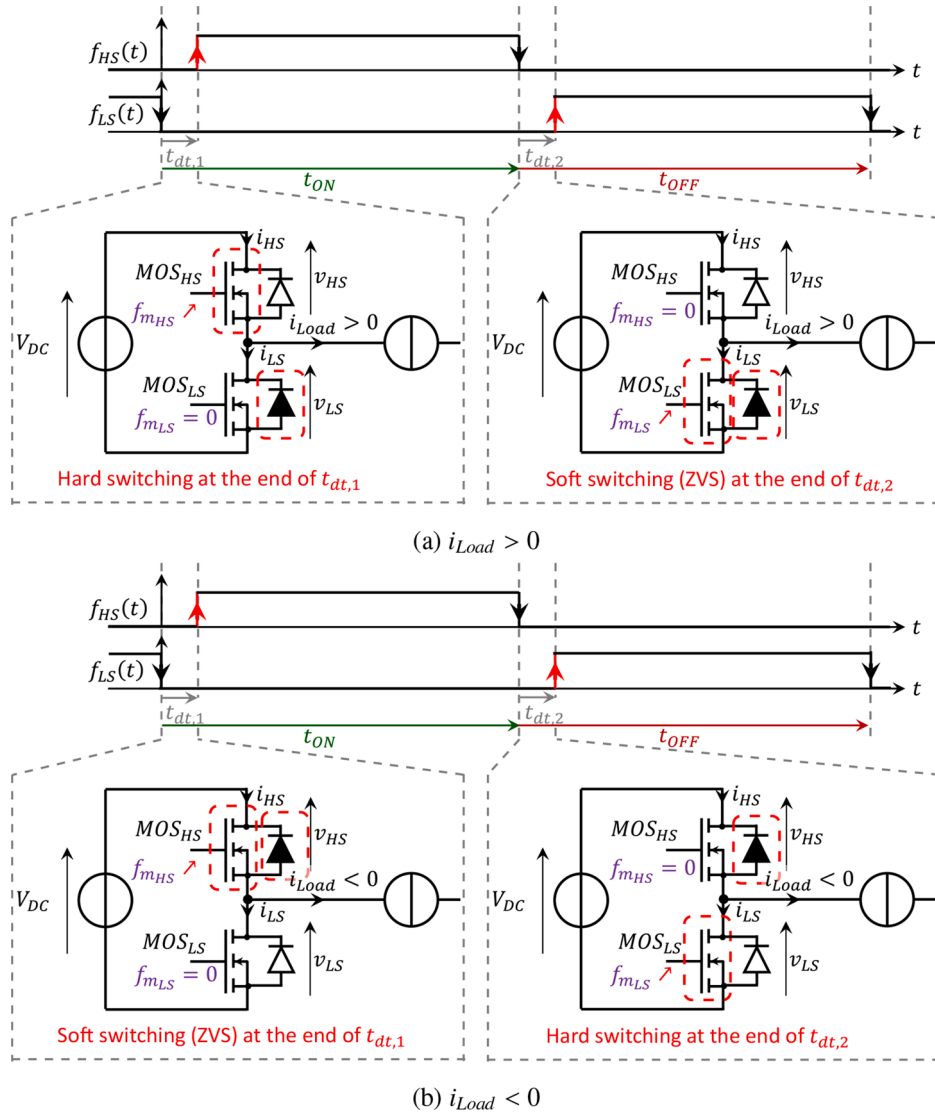


Fig. 15. Dead time and reverse recovery losses in a Three-Phase DC/AC Inverter.

the current in addition to that of the body diode. During this time interval, only the body diode and the Schottky diode conduct. Whatever the Schottky diode I-V characteristics is, the combined conduction losses of both diodes connected in parallel are therefore necessarily lower than the conduction losses without using a Schottky diode.

Technically, Eqs. (21) and (23) give the current distribution between the body diode and the Schottky diode. If the Schottky diode has characteristics, i.e. threshold voltage V_{Sch} and dynamic resistance R_{Sch} , of lower values than the body diode (V_b and R_b , respectively), then the conduction losses are significantly reduced. During a single dead time, the reduction in conduction energy losses can be determined using the following analytical model:

$$E_{cond(gain)} = \left(I_F^2 \cdot \frac{V_b + I_F \cdot R_b}{I_F} - I_b^2 \cdot \frac{V_b + I_b \cdot R_b}{I_b} - I_{Sch}^2 \cdot \frac{V_{Sch} + I_{Sch} \cdot R_{Sch}}{I_{Sch}} \right) \cdot t_{dt} \quad (28)$$

Based on this parameter set, the reverse recovery losses in the body diode when using an additional parallel Schottky diode $E_{rr(b)}$ is computed using Eqs. (4), (21), (22) and (24), the expression for $E_{rr(gain)}$ is as follows:

$$E_{rr(gain)} = E_{rr} - E_{rr(b)} \quad (29)$$

This computation is achieved in the realistic assumption that the extra Schottky diode generates no additional reverse recovery losses.

Considering a single switching cell of the 3-phase VSI, each switching period results in one reverse recovery energy losses occurring at the end of one of the two dead times and two conduction energy losses occurring during each dead time. Consequently, the overall expression for the reduction in three-phase VSI power losses is expressed as follows:

$$P_{(gain)} = 3 \cdot F_m \cdot \sum_{n=1}^m \left[E_{rr(gain)} \left(\theta = \frac{2\pi n}{m} \right) + 2 \cdot E_{cond(gain)} \left(\theta = \frac{2\pi n}{m} \right) \right] \quad (30)$$

7.3. Simulation results and model validation

A study is conducted on a three-phase VSI made up of six MOSFETs, specifically the model FDMC010N08C from the manufacturer FAIRCHILD. This VSI operates with a sinusoidal current waveform characterized by a 30A peak magnitude and a 200Hz modulation frequency.

The input power source of the VSI is a 50V DC voltage. A standard Sinusoidal Pulse Width Modulation (SPWM) is used to control the MOSFETs switching states (Hava et al., 1999). A dead time control circuit permits to implement a 60ns dead time at the input of the MOSFET gate drivers.

In a second step, Schottky diodes are added in parallel with each MOSFET to mitigate the reverse recovery loss in the body diode. Table 2 presents a comparison of the maximum ratings for the MOSFET and the selected Schottky diodes. Two Schottky diodes are compared, as illustrated in Fig. 16. The first one, namely the FAIRCHILD NTS10100MFS, exhibits superior conduction characteristics compared to the body diode under the operating conditions. Hence, during the dead time, it carries most of the switch current. In contrast, the second diode, namely the FAIRCHILD MBR10H100CT, falls short of the first Schottky diode performance inducing a low body diode current reduction especially at high load current. These characteristics are also compared with impedance of the MOSFET in ON state. This comparison reveals that negatives currents mainly pass in the MOSFET channel rather than in the diode. Then, adding a Schottky diode has minor impact on the conduction losses in the selected case.

Table 2 also features the parameters of the 1st order analytical model of both the MOSFET and the selected Schottky diodes. At ON state, a MOSFET behaves like a channel resistor denoted R_{ch} . At OFF state, its body diode is modeled as the combination of a resistor, a voltage source, and an idealized diode in series. Similarly, a Schottky diode is characterized by the same set of parameters but with different values. The body diode is characterized by R_b and V_b , while the Schottky diode is characterized by R_{sch} and V_{sch} . These analytical model values are obtained from the LTspice simulation models provided by their manufacturer, i.e. FAIRCHILD in the present case.

Based on LTspice model, the I-V characteristics of the MOSFET and Schottky diodes are depicted in Fig. 16 and compared to the 1st order model. The body diode characteristic, originally in the third quadrant, has been shifted to the first quadrant for comparison with the MOSFET channel and the Schottky diode. Obviously, the MOSFET channel exhibits higher conduction properties compared to all other components. As a result, during reverse conduction, the MOSFET channel carries the entire load current (in the case the MOSFET is in ON state). Analytical 1st order models for both the body diode and Schottky diodes are presented as dash-dotted lines.

Losses are computed for a range of switching frequencies, spanning from 10kHz to 500kHz, using both the analytical model and LTspice simulation. The results, as displayed in Table 3, illustrate the power losses reduction achieved by using additional Schottky diodes. A constant relative difference of approximately 20% is found between the model and simulation. This difference can be explained by the model hypothesis introduced in Eqs. (21) and (22). Even if the absolute power losses mitigation value is not fully accurate, the comparison reveals that the trends are in phase, which is the main goal of this study.

The gain highlighted in Table 4 comes from the dynamic characteristics of the diode, i.e. recovery losses, but also from the static characteristics, i.e. the conduction losses due to synchronous rectification and dead time conduction. In the proposed case, synchronous rectification benefit is minimal, because of the better I-V curve of the MOSFET as depicted in Fig. 16. Table 4 separates the impact of dead time conduction losses and recovery losses by an analytical calculation. Table 4 reveals that the benefits of adding a Schottky diode comes mainly from

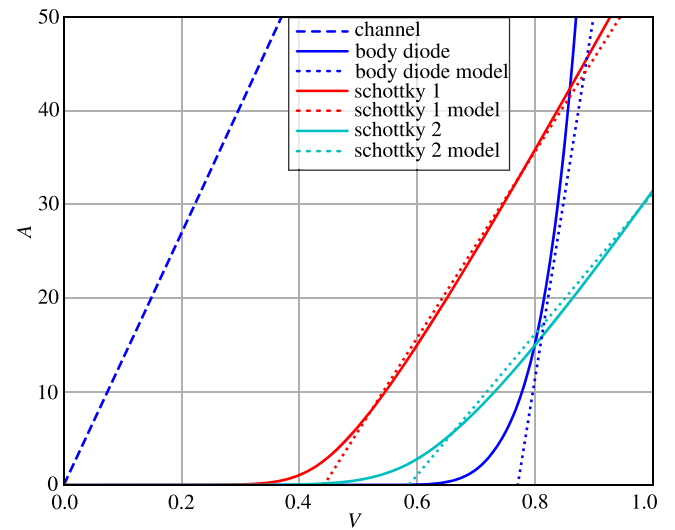


Fig. 16. Characteristics of the MOSFET body channel, the MOSFET body diode and the 2 tested Schottky diodes.

the recovery losses, which validates the developed analysis.

In Fig. 17, the total losses in the three-phase VSI are depicted both using and without using the Schottky diodes. On a global scale, it is obvious that total losses exhibit a linear relationship with the VSI switching frequency. To better understand this relationship, a first-order polynomial curve fitting has been applied to both cases. Notably, these two fitting lines intersect at the same point on the total losses axis. This intersection represents the total conduction losses in the inverter, which remain unaffected by the presence of the Schottky diode, as the MOSFET channel predominantly conducts outside the dead time.

A simulation is also conducted using an ideal Schottky diode ($R_{sch} = 1\mu\Omega$, $V_{sch} = 0V$), depicted by the black line in Fig. 17. The results delineate the maximum gain achieved by integrating a Schottky diode. Notably, the Schottky diode in this scenario exhibits superior characteristics compared to the MOSFET channel, contributing to a reduction in conduction losses outside the dead time of 2.5W (synchronous rectification). Then, at 200kHz, the addition of a perfect Schottky diode saves 31% of losses, including 20% from the recovery losses gain. These gains represent the absolute gain using a perfect diode. The gain is 14% with Schottky 1, and 8.8% with Schottky 2, which represents a substantial benefit considering the small effort of adding a diode.

As the switching frequency increases, the absolute power reduction becomes increasingly significant. This observation highlights the advantage of using high quality Schottky diodes in high switching frequency VSIs, as this provides more substantial power savings that are key points for thermal issue and hence system reliability and lifetime.

8. Conclusion and perspectives

A new methodology to estimate analytically the reverse recovery power losses is introduced in this work. The developed model is based on physical consideration and relies on only two macro parameters which are easy to identify. It is demonstrated that the developed analytical model is more accurate than standard model and does not require

Table 2
Studied MOSFET and Schottky diode parameters.

Parameters	MOSFET	Schottky 1	Schottky 2
Peak voltage	$\delta V_{DSS} = 80V$	$V_{RRM} = 100V$	$V_{RRM} = 100V$
Continuous current	$I_D = 51A$	$I_{F(AV)} = 10A$	$I_{F(AV)} = 5A$
Peak current	$I_D = 206A$	$I_{FSM} = 200A$	$I_{FSM} = 180A$
Model parameters	$R_{ch} = 7.419m\Omega$ $R_b = 2.571m\Omega$ $V_{sb} = 0.771V$	$R_{sch} = 10.051m\Omega$ $V_{sch} = 0.442V$	$R_{sch} = 13.275m\Omega$ $V_{sch} = 0.586V$

Table 3

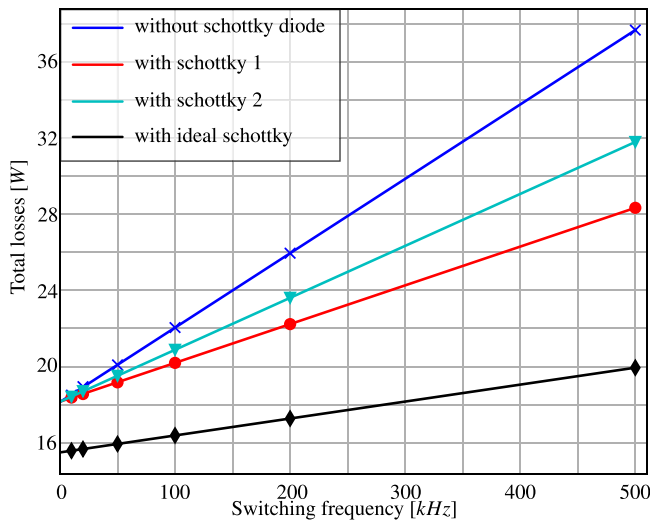
A comparative analysis between an analytical model and LTspice simulation.

F_s	$P_{(gain)}$ (W) Schottky 1			$P_{(gain)}$ (W) Schottky 2		
	LTspice	Model	ϵ	LTspice	Model	ϵ
10kHz	0.126	0.142	12.70%	0.085	0.092	8.24%
20kHz	0.389	0.292	24.94%	0.239	0.189	20.92%
50kHz	0.919	0.709	22.85%	0.574	0.462	19.51%
100kHz	1.856	1.426	23.17%	1.169	0.928	20.62%
200kHz	3.727	2.844	23.69%	2.344	1.851	21.03%
500kHz	9.340	7.097	24.01%	5.880	4.620	21.43%

Table 4

Gain in losses by adding a Schottky diode : impact of reverse recovery and dead time conduction.

F_s	Schottky 1			Schottky 2	
	$P_{rr(gain)}$ [W]	$P_{cond(gain)}$ [W]	$P_{rr(gain)}$ [W]	$P_{cond(gain)}$ [W]	
10kHz	0.131	0.010	0.086	0.003	
20kHz	0.262	0.019	0.171	0.006	
50kHz	0.656	0.049	0.429	0.015	
100kHz	1.313	0.097	0.859	0.029	
200kHz	2.625	0.195	1.716	0.059	
500kHz	6.563	0.487	4.289	0.147	

**Fig. 17.** Total power losses in a 3-Phase DC/AC inverter as a function of the switching frequency f_s using LTspice simulation.

extensive simulations or experiments. Additionally, it gives a good insight of the parameters impacting PiN diode losses. Apart from temperature, the switched current as well as the dead time value, i.e., the time during which it flows in the diode, are two key parameters.

The method, validated with both simulations and experiments, is applied to a MOSFET body diode. Then, a comparative study revealed the potential benefits of adding a Schottky diode in antiparallel with the MOSFET built-in body diode. It permits to decrease the total reverse recovery losses only if its static I-V characteristic is far below the body diode one. Even in these cases, however, the reverse recovery losses decrease is significant only in the case the dead time is large (hundreds of ns). This output is one of the main contributions of the article. Indeed, the suggested analytical model enables to give relevant guidelines to the power converter designer. The developed methodology can be summarized as:

1. Measurement of $Q_{a,m}$ and $Q_{b,m}$ from a Double Pulse Test measurement, for a given value of I_F and di/dt .
2. Determination of τ_a using Eq. (12) and the value of $Q_{a,m}$.
3. Determination of ν_a using Eq. (13) and the value of $Q_{b,m}$ and τ_a .

4. Use of Eq. (10) to compute Q_a and Q_b , the sum of which representing the total stored charge Q_{rr} , function of I_F and di/dt .
5. Use of Eq. (4) to compute the reverse recovery losses for different values of I_F and di/dt .

Finally, the suggested model reveals accurate and gives relevant results to assess properly the additional power losses of a VSI. This specific use case is of paramount importance because VSI are commonly used. To our best knowledge, this application could not be properly addressed using fast analytical model because the output current evolves deeply over time. Conversely, the present approach enables to explicit whether additional Schottky diodes are beneficial or not regarding power losses. The study case reveals substantial power loss savings when adding a high quality Schottky diode on a high switching frequency VSI. Beyond this specific result, the models and the methodology can be applied to other use-cases. Future works will include thermal modelling to assess the benefits in terms of reliability, a study on the voltage overshoot, as well as the application to the case of SiC MOSFET intrinsic body diode.

CRediT authorship contribution statement

Mohammed Bououd: Writing – original draft, Validation, Investigation, Data curation, Conceptualization. **Yiyu Lai:** Writing – original draft, Validation, Software, Formal analysis, Data curation, Conceptualization. **Adrien Voldoire:** Writing – original draft, Supervision, Methodology, Formal analysis, Conceptualization. **Emmanuel Hoang:** Supervision, Project administration, Methodology. **Olivier Béthoux:** Writing – original draft, Supervision, Project administration, Methodology, Investigation, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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