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***Abstract* — The use of a high energy X-ray generator for Total Ionizing Dose testing is studied on MOS capacitors. Several conditions were studied for the high energy X-ray irradiations (with aluminum and lead filters) and the experimental results are compared to Co-60 irradiations. The effects of both annealing and package lid are also studied. All the results are presented and discussed. It is shown that the simple BEOL stack (only one thin aluminum layer) has no effect on dose deposition in the oxide of MOS capacitors.**

***Index Terms*—Total Ionizing Dose, high energy X-ray, Cobalt-60, Dose testing, MOS Capacitor.**

I. Introduction

Over the past decade, efforts have been made to reduce the world's dependence on high-level radioactive sources, particularly Cobalt 60 (Co-60) and Cesium 137 [1-3]. These sources are used in commercial, medical, and research applications throughout the world. The main objective, as a security strategy, is to replace high-risk radioactive sources with less risky alternatives in order to enhance radiological security and to forestall an act of radiological terrorism. In the field of reliability of electronic components and systems, for space, military, accelerator and nuclear power plants applications, such radioactive sources are used for Total Ionizing Dose (TID) testing. These sources are used because they are recommended by current testing standards such as MIL-STD-883 test method (TM) 1019 for TID qualification and Radiation Lot Acceptance Testing (RLAT) [4], ESA ESCC Basic Specification No. 22900 [5], and ASTM F 1892 Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices [6]. These standards specify electronic devices testing using irradiation from photons sources, such as Co-60 γ irradiators, Cesium 137 γ irradiators, electrons beams, and low energy (approximately 10 keV) X-ray generators. However, Co-60 remains the most common radiation source used for total ionizing dose testing of electronic components and systems. Co-60 is usually considered as the reference ionizing radiation source to perform TID tests on electronic devices and systems. In order to meet the above requirements in terms of security, alternative solutions must be found.

The use of a high energy X-ray generator has recently been proposed to performed TID testing [7]. In the context of electronics, and in accordance with the above-mentioned standards, generators of over 100 kV are considered to be high-energy X-ray generators. Photons of 100 keV interact in a Compton predominant effect for the majority of elements making up electronic systems. X-ray generators are generally considered much more convenient for TID testing and offer many advantages: (1) safety and security issues are more easily managed with an X-ray generator than with radioactive sources, (2) the photon energies are low enough that it can be easily collimated that allows irradiating a single part on a board, (3) X-ray generator offers a relatively high dose rate, thus offering reduced testing time, and (4) X-ray generators are less expensive to purchase and maintain than radioactive sources. Moreover, high energy X-ray generators offer the possibility to test packaged devices due to high penetration depths.

In [7], high energy X-ray generator was used with a lead filter in order to attenuate low energy photons of the energy spectrum, i.e. reduce the photoelectric effect and get closer to Compton scattering processes. It has been shown (on Metal Oxide Semiconductor (MOS) and bipolar transistors) that, with such a lead filter, it is possible to approach the degradation obtained with a Co-60 irradiation and this is all the more true as the voltage of the tube (the maximum energy of the photons) is high. However, a gap in the observed degradation between high energy X-rays with a lead filter and Co-60 irradiations remains. This gap has been attributed to packaging or backscattered photons in Back-End-Of-the-Line (BEOL) stack (contacts, metal layers, insulating layers) that can have a significant TID contribution in the sensitive oxide of the investigated devices [8]. This stack of layers can also induce dose enhancement, which is function of the photon energy (with higher dose enhancement factor for low energy photons) and is larger for high Z elements [9-19].

Since dose enhancement occurs mainly with low-energy photons and metallization with high Z values, as shown in [12] where Oldham and McGarrity noted a strong dose enhancement effect with a 10 keV X-ray generator in MOS capacitors with Al metallization, we have decided to investigate in this work MOS capacitors with Aluminium metallization. We will show that dose enhancement effects can be reduced compared to [12] because the high-energy generator used in this work produces a spectra with a smaller proportion of <20 keV photons than the 10 keV generator in [12]. In addition, the use of filters makes it possible to limit the proportion of these low-energy photons even further

Vincent Girones, Jérôme Boch, Frédéric Saigné and Tadec Maraine are with IES, Université de Montpellier, CNRS, Montpellier, France. (e-mail: vincent.girones@umontpellier.fr).
Alain Carapelle is with Centre Spatial de Liège (CSL), 4031 Angleur, Belgium.
Arnaud Chapon is with ATRON METROLOGY, F-50130 Cherbourg en Cotentin, France.
Rubén García Alía is with the European Organization for Nuclear Research (CERN), CH-1211 Genève 23 Switzerland.

In the present work, we decided to pursue the comparison between high energy X-rays and Co-60 irradiations by studying MOS capacitors. The MOS capacitor studied in this work is a very simple Si/SiO_2 structure where only one metallization layer is deposited on the oxide. Aluminum (Z=13) was chosen for the metallization layer to reduce dose enhancement as much as possible.

The objectives of this work are the following: (1) show that the approach used in [7] and validated on MOS and bipolar transistors (the use of a high energy X-ray generator with a lead filter) is also applicable for MOS capacitors, (2) show that for a device with a minimum of layers above the sensitive area (only one aluminum layer on the top of the oxide) an high energy X-ray irradiation with a lead filter gives the same degradation as a Co-60 irradiation.

In section II, the experimental setup will be described. The investigated MOS capacitors and the irradiation facilities will be presented. Experimental results will be given in section III and IV. The effect of annealing, package lid, and bias are studied. Discussion of the obtained results and conclusions are given in part V.

II. Description of the Experimental Setup

In this section, the investigated MOS capacitors are described and the irradiation facilities are presented.

A. MOS capacitors

Specific capacitors have been manufactured for this study. This allows to control the manufacturing parameters (area, oxide and metallization thicknesses, doping). These samples were fabricated at LAAS (Laboratory for Analysis and Architecture of Systems) through the RENATECH network [20] in Toulouse (France). Two different dies with two SiO2 oxide thicknesses: 400 nm (Fig. 1a) and 100 nm (Fig. 1b) were manufactured on a p-type silicon substrate with a doping concentration between $1.1x10^{15}$ and $1.6\ x10^{15}$ at.cm^{-2} of 525 µm giving the Substrate Capacitance (SC). For each thickness (on each die) two capacitors of two different areas were designed. Twenty dies of each thickness are available for this study, which corresponds to 160 MOS capacitors. Each die was then mounted in a DIL (Dual InLine) package to facilitate irradiation and measurement, as shown in Fig. 1c. On the top of the oxide, contact metallization is realized with 1µm aluminum layer. All the MOS capacitor parameters are given in Table I.

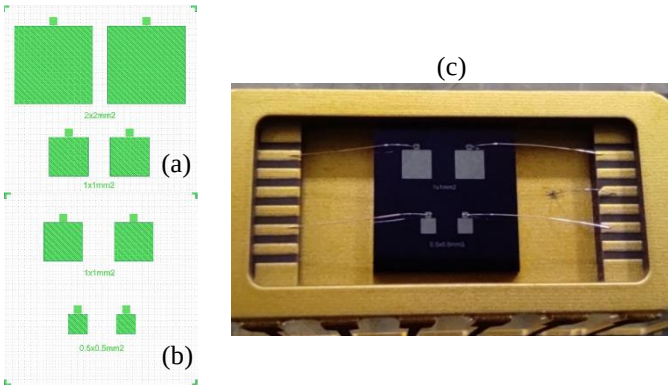

Fig. 1. (a) implantation plan of the 400 nm MOS capacitors, (b) implantation plan of the 100 nm MOS capacitors , (c) photograph of a 100 nm device without lid.

TABLE I
Mos Capacitor Parameters

Parameter	400 nm Large	400 nm Small	100 nm Large	100 nm Small
Size (mm²)	2x2	1x1	1x1	0.5x0.5
Area (mm²)	4.00	1.00	1.00	0.25
Al thickness (µm)	1.00	1.00	1.00	1.00
Ox. thickness (nm)	400.00	400.00	100.00	100.00
Ox. capacitance (pF)	345.15	86.29	345.15	86.29
SC thickness (µm)	525.00	525.00	525.00	525.00
SC capacitance (pF)	78.8	19.7	19.7	4.9

B. Irradiation facilities

All devices were irradiated with the PlatfoRm for the Study of the Effects of Ionising Radiation on Electronics (PRESERVE) at the Institut of Electronics and Systems (IES) in Montpellier, France. Two irradiation facilities are used in this work: a 60 curies Co-60 source and an 320 kV X-RAD320 X-ray generator. For dosimetry, two cross-calibrated (in Air) ionization chambers from PTW are used to measure dose rates: the TM30013 (with a 30 keV to 50 MeV energy range) connected to the Unidos E dosimeter for Co-60, and the TM7862 (with a 7.5 keV to 420 KeV energy range) for the X-ray. In all this paper, the dose has been corrected as a function of the energy spectrum of the facility and is given in Gy(SiO_2) [7].

The irradiation conditions are given in Table II. Five irradiation conditions are considered: Co-60 irradiation with three different dose rates, 320 kV X-rays irradiation with Al filter, and X-rays irradiation with Al + Pb filter. The Al filter allows to attenuate low energies below 15 keV so when we perform the dose rate measurement for X-ray with the Al filter, we are not limited by the TM7862 chamber whose limit is 7.5 keV. In our case the Co-60 source is is a panoramic irradiator in a large room, wich greatly reduces secondary photon generation,so filters are use for condition 1 to 3.

TABLE II
Irradiation conditions

Condition #	Source #	Filter #	Dose Rate Gy(Air)/h	length Source-target (mm)
1	Cobalt-60	None	5,28	330
2	Cobalt-60	None	0,62	920
3	Cobalt-60	None	0,15	1920
4	X-ray 320 kV 1.6 mA	2mm Al	30	400
5	X-ray 320 kV 11.4mA	2mm Al + 1mm Pb	30	400

It is also important to be in electronic equilibrium when testing total dose. This is difficult to achieve with commercial components due to the unknown BEOL. Our capacitors have the advantage of being metallized in Al (low Z), which reduces the effects of dose enhancement. [21]

Finally, it is essential to compare the degradation of components at equivalent doses. To do this we use conversion factors from dose(air) to dose(SiO2). Knowing the spectrum generated, the dosimetry (Gy(Air)) and the target (in SiO2). We can calculate a SiO2 dose by correlating each spectrum with the mass energy-absorption coefficient (µen/ρ) obtained from NIST database, as detailed in [7]. Factor are: Co-60: 1; Xray with Al filter: 2,25 ; Xray with Al+Pb filter: 1,15.

III. IRRADIATION RESULTS

In this section, the experimental data obtained on MOS capacitors submitted to Co-60 and X-Ray irradiation are given.

A. *MOS capacitors characterization*

Capacitance Voltage (C/V) characterizations were performed with B1500 semiconductor device parameter analyser from Keysight. These measurements were made at a frequency of 1 MHz with 30mV oscillations. The measurement voltage range was limited from -5 V to 5 V to reduce the risk of oxide capacitor breakdown. The voltage range was applied in the direction from -5 V to 5 V by step of +0.2 V each 100 ms.

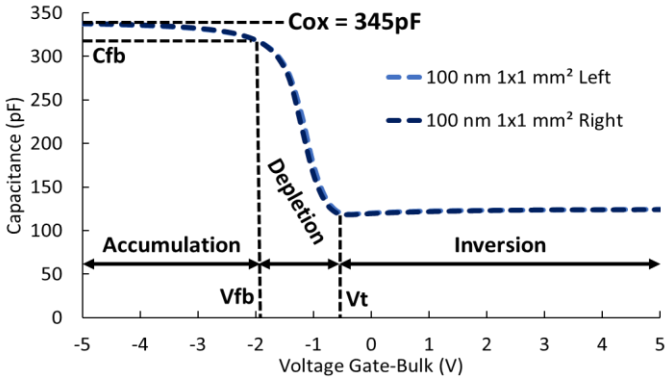

Fig. 2. Standard C/V on two 100 nm MOS capacitors with an area of 1x1 mm².

It is well known that for a MOS capacitor, the capacitance changes with an applied DC voltage between gate and bulk (Vgb). As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. In Fig. 2, a standard C/V is plotted, before irradiation, for two 100 nm MOS capacitors (on the same die) with an area of 1x1 mm².(the blue and the orange dashed lines) As the voltage increases from -5 V to 5 V, the MOS capacitor passes through accumulation, depletion, and inversion modes [22-24]. For a p-type MOS capacitor, the oxide capacitance (Cox) is measured in the strong accumulation region where the voltage is negative enough that the capacitance is constant and the C/V curve is flat. For exemple, in Fig. 2, the Cox value is 345 pF which is close to our theoretical values given in Table I (345.15 pF for 100 nm and 1x1 mm²).

Another important parameter is the flatband voltage V_{fb}. Flatband voltage and its shift (after irradiation) are widely used to extract oxide charges. The flatband voltage can be extracted from the C/V curve thanks to the capacitance method [22]: the flatband capacitance Cfb is calculated from Cox and the Debeye length, this Cfb capacitance is used to determine on the C/V curve the flatband voltage as depicted in Fig.2.

B. *Irradiation of MOS capacitors*

MOS capacitors (all oxide thickness and all area) were irradiated in the five conditions given in Table II. An example is plotted in Fig. 3. In this figure, a 100 nm capacitor with an area of 1x1 mm² is irradiated in condition 2 for a 600 Gy(SiO_2) total dose. The light blue solid curve corresponds to the prerad C/V and the dark blue curve corresponds to the C/V after 600 Gy(SiO_2). The darker blue curve is identical to the dark blue curve, but the C/V measurements were performed with decreasing Vgb. A dashed blue curve repeats the prerad curve ,but shifted, to highlight the change in slope.

From this Fig 3, the three main effects of TID on the C/V curve can be identified [22]. The first one corresponds to the shift of the flatband voltage (illustrated by the red arrow (1) in Fig. 3), and is due to oxide trapped charges. The second one corresponds to a widening of the depletion region, i.e. a reduction of the slope of the C/V curve (illustrated by the red arrow (2) in Fig. 3), and corresponds to interface trapped charges. The last red arrow (3) show the mobile charges in the interfacial zone due to impurities. These three main effects will be used in the remainder of this paper to characterize the degradation.

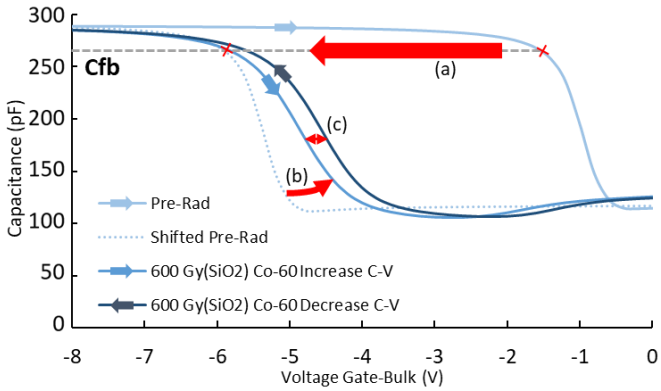

Fig. 3. Standard TID effect on C/V for a MOS capacitor. 100 nm capacitor with an area of 1x1 mm² irradiated in condition 2 (Co-60) (Table II) for a 600y(SiO_2) total dose. Sens!!!

For each irradiation condition 2 DIP packages were used: one with a 100 nm oxide thickness and a second one with a 400 nm oxide thickness. Each package contains 4 capacitors with a fixed oxide thickness (100 nm or 400 nm). These 4 capacitors are divided into pairs, 2 large surface area capacitors and 2 small surface area capacitors for each package. This gives an average of 2 capacitors with the same data sheet per irradiation condition. For each irradiation condition, it gives 8 capacitors.

Fig. 4 details all the C/Vs achieved for one irradiation condition, each C/V being the average of two capacitors as explained previously.

The charge trapping in the oxide is clearly visible for both oxide thicknesses. The thicker the oxide, the more flatband voltage shift. Fig. 4 (a) shows that from the second measurement the flatband voltage is outside the reading range of the B1500 (+/-10V) for the 400 nm capacitors, whereas the 100 nm capacitors remain analysable for all the steps made. We can also see that the slopes remain mostly parallel this indicates a low presence of trapped charge at the interface. Finally, the inversion zone is not perfectly linear for some of our C/Vs. The frequency chosen to carry out the C/Vs was not high enough. This will not be a problem for the rest of the study, as no parameter is extracted from this part of the curve.

The high oxide thickness of the 400 nm capacitor makes them more sensitive to dose deposition, resulting in greater degradation for the same dose. 400 nm capacitors are not adapted to our irradiation facilities. We can work with minimum steps of 10 Gy (1 krad). Therefore, in order to ensure a more reliable analysis, we will focus on the study of 100 nm capacitors of 1x1 mm² and 0.5x0.5 mm².

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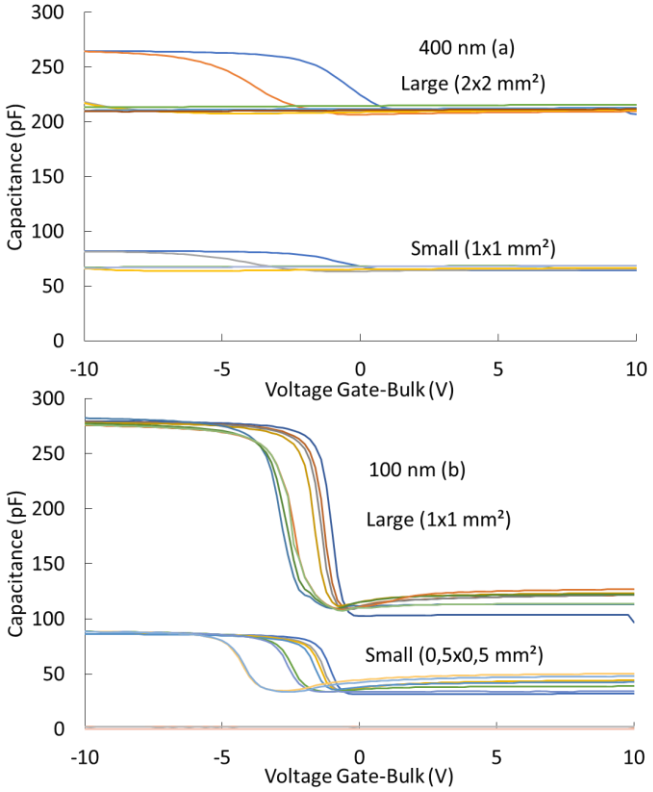

Fig. 4. Dose effect for irradiation condition 2 (Co-60) on 400 nm (a) and 100 nm (b) MOS capacitor with Large and Small area.

For the first part of the results analysis, all the components are irradiated at room temperature, and a maximum fixed time of 40 min has been defined to characterize the components and so limit annealing. It is well known that the degradation of such components is greater when a bias is applied during irradiation. Since the degradations obtained are already significant and enable us to highlight the desired effects, we chose not to apply a bias for this part to the MOS capacitor during irradiation.

A first detailed example is given in Fig. 5, where a 100 nm MOS capacitor with an area of 1x1 mm^2 is irradiated in condition 2 up to 253 Gy(SiO_2).

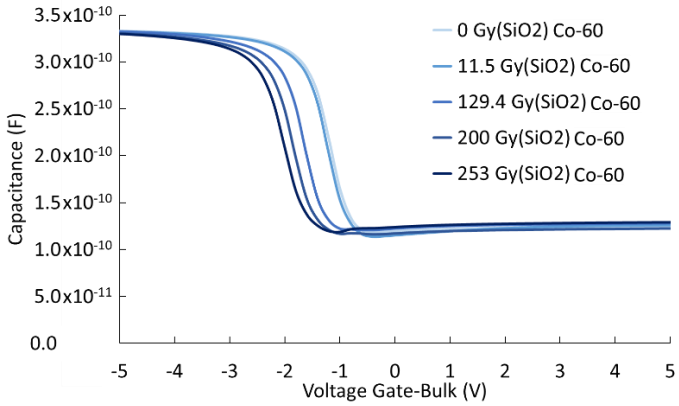

Fig. 5. Dose effect for irradiation condition 2 (Co-60) on a 100 nm MOS capacitor with an area of 1x1 mm^2 from 0 to 253 Gy (SiO_2), unbiased.

Fig 5. shows up the fact that at room temperature and with all the pins at ground, the main phenomenon is the shifting of the V_{fb} towards the left. This parameter will be extracted for the Co-60/X-rays comparaison.

C. *Annealing*

Since the X-rays irradiations are shorter than the cobalt irradiations, it is important to investigate annealing effects. Room temperature annealing have been then performed after X-rays irradiations. The obtained results are presented in the Fig. 6 and 7. For each irradiation condition presented above, measurements were taken 24, 48, and 168 hours after the last total dose step to study annealing at room temperatures. The devices used in the fig. 6 and 7 were irradiated at 590 Gy (SiO2) with Co-60 under condition 2. 15% annealing is observed and the majority of annealing takes place during the first 48 hours. There is less than 2% variation between 48h and 168h.

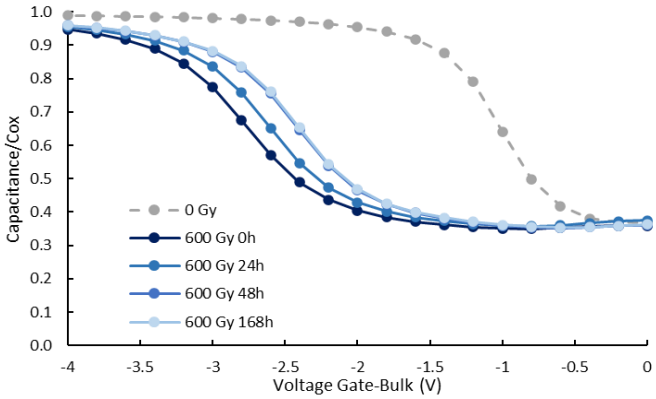

Fig. 6. Annealing effect for irradiation condition 2 (Co-60) at 590 Gy(SiO2) on a 100 nm MOS capacitor with an area of 0.5 x 0.5 mm^2.

We have seen that after 1 week of annealing at room temperature, the annealing effect is less than 2%. These measurements were therefore repeated for each experiment and then averaged. An average annealing of around +0.3 V for flatband voltage at 168 h was measured for Co-60 (conditions 1,2,3) and for aluminium-filtered X-rays (condition 4). For X-rays filtered with aluminium + lead (condition 5), the average annealing at 168 h was only +0.12 V. This is explained by the total dose received (and so degradation) being 2 times lower, only 253Gy compared with 600 Gy for conditions 2 to 4. We also extracted the standard deviation of the anneals to form the error bars which are stable whatever the dose deposited and conditions. These standard deviations are mainly due to the initial values of the capacitors.

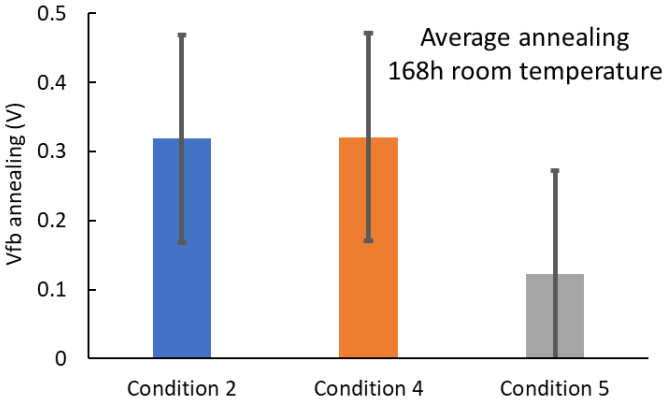

Fig. 7. Annealing effect for irradiation condition 2 (Co-60) 4 and 5 (X-rays) at 590 Gy(SiO2) for 1 and 4, and 253 Gy(SiO2) for condition 5 (Xray-Al+Pb). Error bars corresponds to 3 standard deviations.

D. Package Lid

Our components are delivered with a generic lid. In order to investigate the effect of such a lid, irradiations have been performed with and without lid. The case is a generic ceramic plate 1 mm thick which covers all the capacitors.

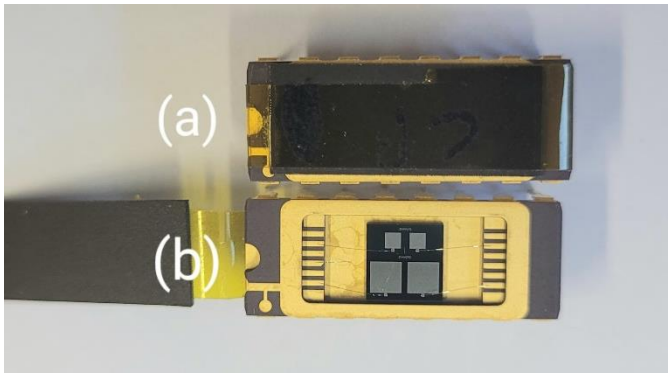

Fig. 8. 2 photographs of 400 nm devices with (a) and without (b) lid.

Experimental results are presented in Fig. 9 for 100 nm 1 x 1 mm² MOS capacitors irradiated with Co-60 (in condition 2). After irradiation, no significant difference is observed between the MOS capacitors irradiated with a lid (blue curves) and the ones irradiated without lids (oranges curves) in terms of V_{fb} variation. Measurements show a small gap for the V_{fb} and a major difference in the inversion zone. These deviations are mainly due to the gap between each device.

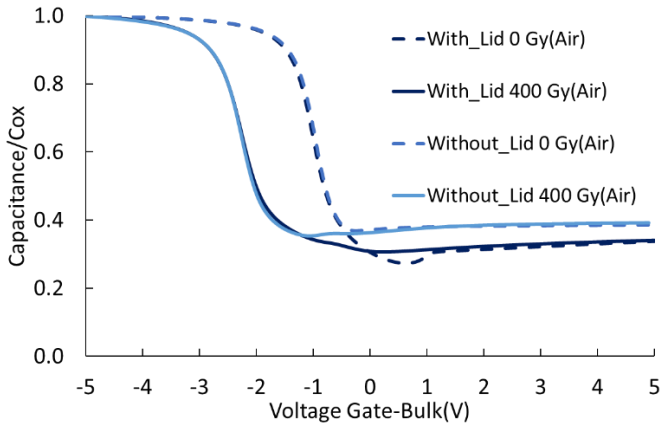

Fig. 9. Comparaison of normalized C/V of 100 nm 1 x 1 mm² at 0(dashed) and 400(solid) Gy(Air) with irradiation condition 2 (Co-60) . lid (dark blue) and without lid (light blue).

E. Comparaison between all Irradiation conditions

It is difficult to compare the C/V curves for different conditions due to the scattering of the results before irradiation. Therefore, we will use the normalized capacitance C/Cox to compare the results for different conditions.

In Fig. 10, the comparison of irradiation conditions 1 (Co-60) , 4 and 5 (X-rays) is shown for a 100 nm capacitor with an area of 1x1 mm² and for a 0-200-600 Gy(SiO_2) total dose. The curves obtained after irradiations are very close, which means that Co-60 irradiation, X-ray irradiation with Al filter, and X-ray irradiation with Al + Pb filter lead to the same observable degradation for high frequency C/V unbiased.

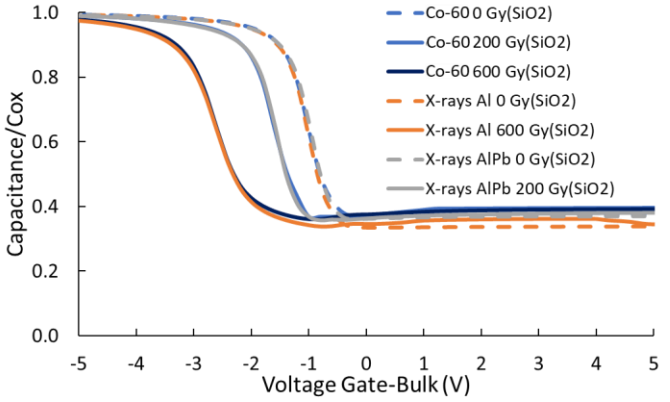

Fig. 10. Comparison of normalized C/V of 100 nm MOS capacitors with an area of 1x1 mm² irradiated in condition 1 (Co-60) at 0 – 200 – 600 Gy(SiO_2), 4 at 0 – 600 Gy(SiO_2) and 5 0 – 200 Gy(SiO_2) (X-rays).

In order to generalize this result, that is to say to carry out the comparison of all the irradiation conditions for several MOS capacitors which we studied, we chose to represent on the Fig. 11 and 12 the shift of the flatband voltage as a function of the dose. For the following curves, the data displayed corresponds to the average of measurements taken on pairs of capacitors with identical physical parameters. In Fig. 11, the flatband shift as a function of the dose is plotted for a 100 nm MOS capacitor with an area of 1x1 mm². It is important to note that on Fig. 11 no particular difference between the several irradiation conditions is observed. We can also note that the variation of the flatband voltage is important, which corresponds to a strong charge trapping in the oxide.

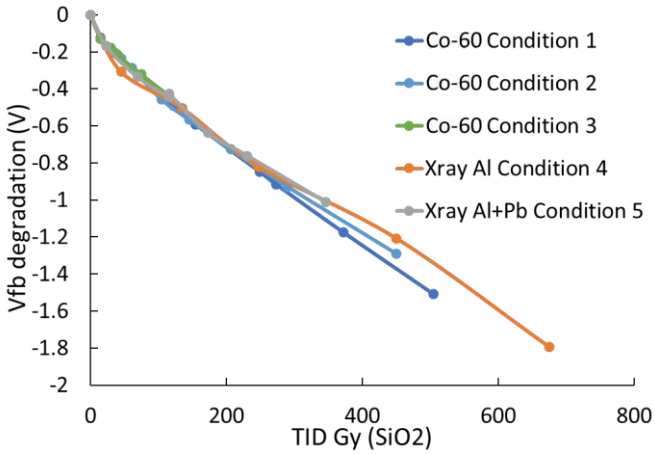

Fig. 11. Comparison of the 5 irradiation conditions on 100 nm MOS capacitors with an area of 1x1 mm².

The same results can be observed in Fig. 12, where the flatband shift as a function of the dose is plotted for a 100 nm MOS capacitor with an area of 0.5x0.5 mm².

The same comparison of all the irradiation conditions has been done for the reduction of the slope of the C/V curve. All the curves exhibit the same trend, no particular difference can be made between the several irradiation conditions and the reduction is weak, i.e. the interface trapped charge is weak.

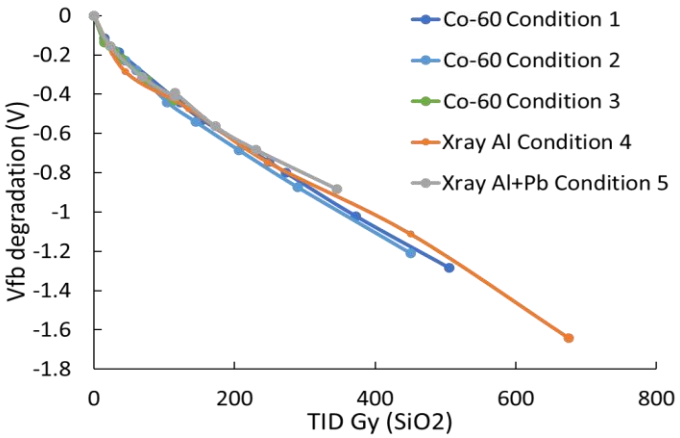

Fig. 12. Comparison of the 5 irradiation conditions on 100 nm MOS capacitors with an area of 0.5x0.5 mm².

As expected, since both the large area and the small area capacitors share the same oxide parameters, large and small capacitors show identical flatband voltage degradation. The differences in results between the 100 nm 1x1 mm² and 0.5x0.5 mm² capacitors are completely contained within the error bars of 3 standard deviations.

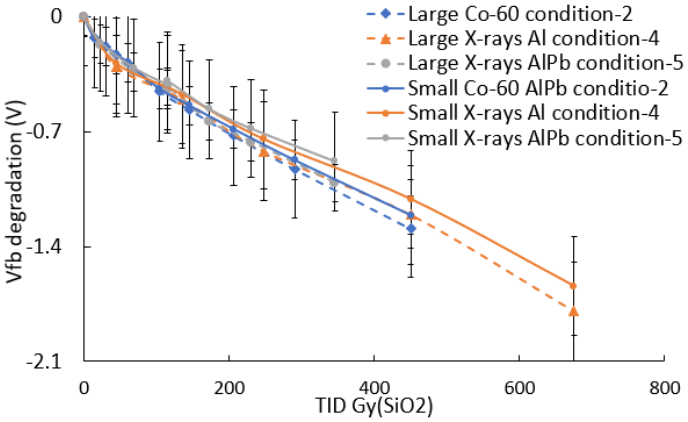

Fig. 13. Comparison of the 3 irradiation conditions (2(Co-60) and 4-5(X-Rays)) on 100 nm MOS capacitors with area of 0.5x0.5 mm² (Small) and 1x1 mm² (Large). Error bars corresponds to 3 standard deviations.

The same comparison of all the irradiation conditions has been done for the reduction of the slope of the C/V curve. All the curves exhibit the same trend, no particular difference can be made between the several irradiation conditions and the reduction is weak, i.e. the interface trapped charge is weak.

IV. BIASED IRRADIATION RESULTS

We are now going to study the different irradiation conditions effects while applying a voltage of 1 MV/cm on the capacitor gates. This means applying Vgb = +10 V for 100 nm and Vgb = +40 V for 400 nm. This bias should limit the differences in charge yields between the different conditions and a more rapid degradation of V_{fb} is expected. This will further limit the use of 400 nm capacitors, which are already very difficult to operate without bias. Moreover, knowing that the degradation was going to be more important, the C/Vs were extended to +/-10 V and slowed down to allow more precision. This allowed us to obtain a standard deviation of 0.2 V for the measurements in this section.

A. Flatband Voltage

For each irradiation condition an additional unbiased 100 nm CMOS die was added. Results have been extracted for this unbiased component and are similar to the results in Part III. This confirms the previous results and allows an unbiased reference to be made in relation to the biased components. A curve corresponding to the trend found in part III-E is therefore displayed in green.

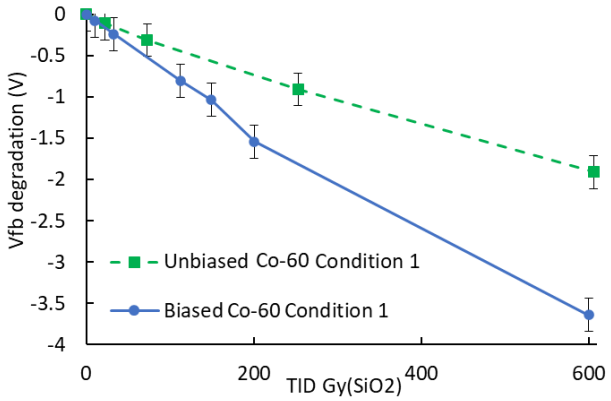

Fig. 14. V_{fb} degradation vs TID Gy(SiO_2) with condition 1 (Co-60) for 100 nm 1x1 mm² MOS capacitor biased (+10V) and unbiased . Error bars corresponds to 3 standard deviations.

In Fig. 14 are shown results of V_{fb} drift vs TID for biased component. As expected, we end up with an increase in V_{fb} shift compared to the unbiased component (green). Biasing electronic components limits initial recombination and therefore increases the number of trapped charges in the oxide during irradiation. With a bias of 1 MV/cm, the V_{fb} voltage shift is multiplied by ~2.

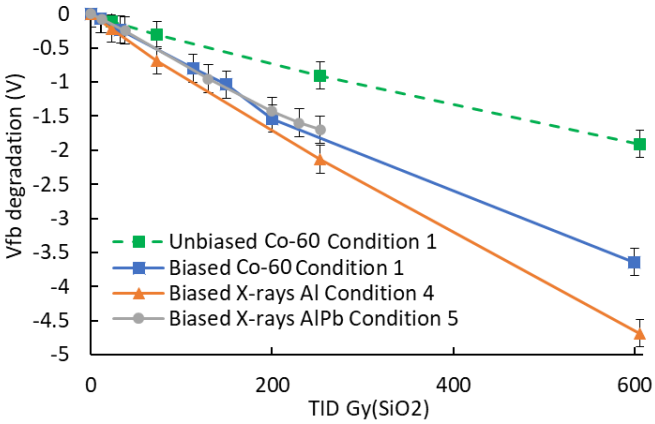

Fig. 15. Comparison for 3 irradiation conditions (1(Co-60)-4-5(X-Rays)) of 100 nm MOS capacitors with area of 1x1 mm² biased and unbiased. Error bars corresponds to 3 standard deviations.

The objective of the study is to investigate the differences between all the proposed irradiation conditions. Fig. 15 details the degradation of V_{fb} as a function of dose for different conditions. It can be seen that the biased components were all more degraded than the unbiased results. But unlike the unbiased test, this time the results are not homogeneous. The aluminium-only X-ray generator (conditions 4) does not seem to match the results for conditions 1 and 5.

The use of a lead filters allows to limit the photoelectric effect by cutting the low energies photons and to get closer to Compton scattering processes as Co-60.

B. *Biased Flatband Voltage Annealing*

As we noted earlier, a discrepancy appears with biased devices when irradiation conditions 4 (Al X-ray) is used. Fig. 16 shows the average annealing effect over 168 hours at room temperature for the different conditions studied previously. Contrary to the results of part III-C, a major difference appears.

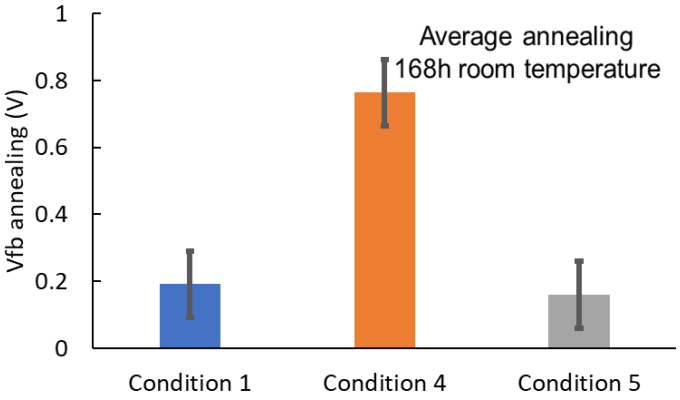

Fig. 16. Comparison of the V_{fb} annealing for 168h at room temperature for 3 irradiation conditions (1(Co-60)-4-5(X-Rays)) on 100 nm MOS capacitors with area of 1x1 mm^2 biased and unbiased. Error bars corresponds to 3 standard deviations.

For conditions 1 and 5 we find equivalent values to those found in part III-C. Condition 5 being slightly lower due to the lower total cumulative dose (253 Gy(SiO_2) in total compared with 600 Gy(SiO_2) for conditions 1 and 4). Nevertheless, a large difference appears when annealing the components irradiated with condition 4: an average annealing measured almost 3 times higher (~0.3 V unbiased against ~0.8 V with bias).

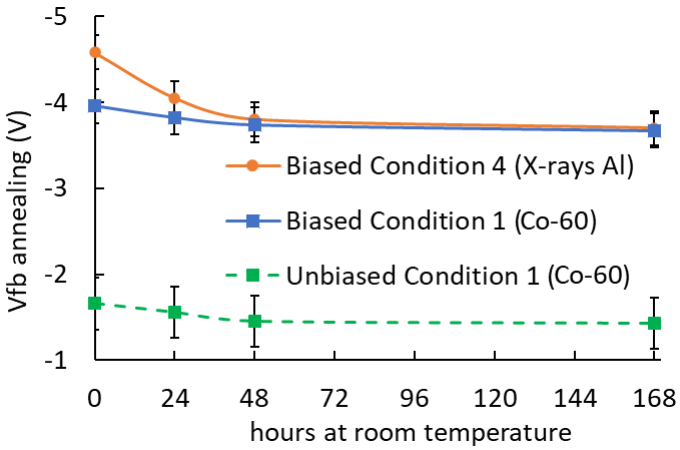

Fig. 17. Comparison of the V_{fb} annealing for 0, 24, 48, and 168 hours at room temperature for irradiation conditions 1(Co-60) and 4 (X-Ray Al) after 600 Gy (SiO2) on 100 nm MOS capacitors with area of 1x1 mm^2 biased and unbiased. Error bars corresponds to 3 standard deviations.

Fig. 17 shows the evolution of V_{fb} at room temperature from 0 to 168h after irradiation with 600 Gy(SiO_2). The biased and unbiased curves for condition 1 show an equivalent trend. Condition 4, which initially shows more degradation, has a much stronger annealing for the first 48 hours before returning to the annealing degradation level of condition 1.

C. *Interface charges*

Applying a bias voltage of 1 MV/cm on the gate of MOS capacitor has accentuated the appearance of interface charges. The evolution of the interface charges as a function of dose for the different irradiation conditions can be seen on Fig. 18. This is similar to the trends observed in the study of generic MOS [7]. Co-60 is the least degrading on the interface charges. There is a gap between Co-60 and high-energy X-ray, but this is reduced when a lead filter is used in addition to the Al. The same trend is observed for large surface area (1x1 mm²) and small surface area (0.5x0.5 mm²) capacitors.

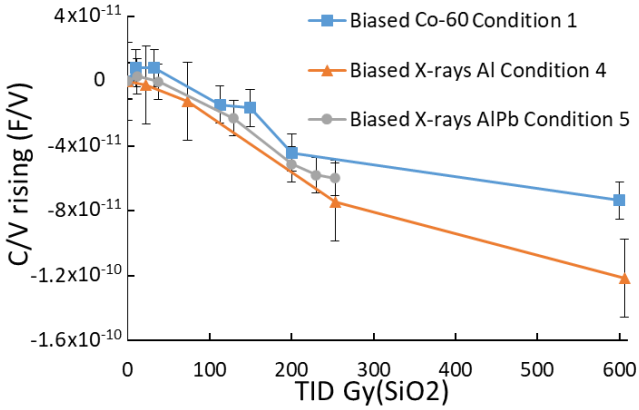

Fig. 18. Comparison of C/Vs hysteresis for 3 irradiation conditions (1(Co-60)-4-5(X-Rays)) on 100 nm MOS capacitors with area of 0.5x0.5 mm^2 biased. Error bars corresponds to 3 standard deviations.

D. *Interface charges Mobility*

If we perform two C/V runs, increasing then decreasing for the Vgb, we can extract a hysteresis revealing the mobility of the interface charges. Fig.19 shows the evolution of this hysteresis as a function of the dose in Gy(SiO_2) for the following 3 irradiation conditions: 1 (Co-60), 4 (X-ray Al), 5 (X-ray Al+Pb). These results are for MOS capacitors biased at 1MV/cm. From the point of view of mobility, the results are similar to the trend in part IV-A. Condition 1 (Co-60) and condition 5 (X-ray AlPb) follow the same trend, whereas this time condition 4 (X-ray Al), instead of being the most degrading, turns out to be less degrading. The same trend is observed for large surface area (1x1 mm²) and small surface area (0.5x0.5 mm²) capacitors.

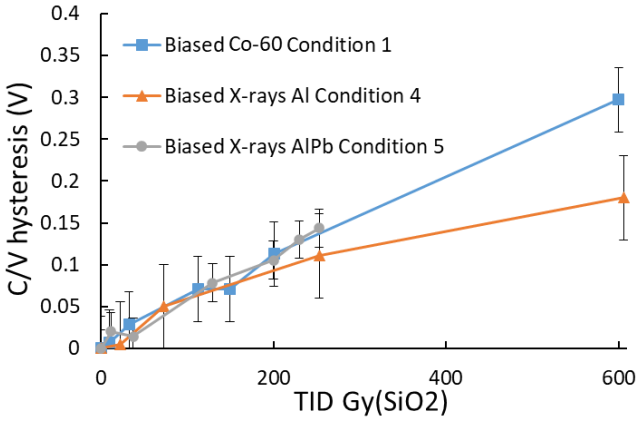

Fig. 19. Comparison of C/Vs hysteresis for 3 irradiation conditions (1(Co-60)-4-5(X-Rays)) on 100 nm MOS capacitors with area of 1x1 mm^2 biased. Error bars corresponds to 3 standard deviations.

V. Discussion and conclusion

In this paper, a comparison between high energy X-rays and Co-60 irradiations has been realized on MOS capacitors. Capacitance Voltage characterization has been used to study the dose response of MOS capacitors.

When exposed to ionizing dose, all the investigated devices exhibit a large shift of the flatband voltage and a weak reduction of the slope of the C/V curve, which means that the degradation is mainly due to oxide trapped charges than interface trapped charges. The effects of both the annealing after irradiation and the presence of a package lid have been also investigated. It is shown that they have no significant effect on the investigated MOS capacitors.

In order to compare high energy X-rays and Co-60 irradiations, five irradiation conditions were studied. For all the investigated devices, no particular difference between the several irradiation conditions was observed. This means that a high energy X-rays irradiation with a lead filter leads to the same degradation as Co-60 irradiation for the investigated MOS capacitors. This result corresponds to what has been proposed in [7] with the difference that we have no gap between the degradations obtained with Co-60 and high energy X-rays with a lead filter. This lack of gap is explained by the structure of the studied components. Indeed, the MOS capacitors were manufactured with only one thin aluminum layer on the top of the oxide.

The experiments were then reproduced with bias on the gate. This highlighted the benefits of the lead filter when using a high-energy X-ray generator. The Co-60 and Al+Pb filtered X-ray results were similar, while a gap appeared in the degradation of the V_{fb} with X-ray filtered only by aluminium. Finally, this also revealed the charge trapping at the interface and the charge mobility at the interface.

To take this work a step further , we'll need to run simulations with GEANT4 and irradiate a wide range of components.

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RADNEXT is an H2020 INFRAIA-02-2020 infrastructure project with the objective of creating a network of facilities and related irradiation methodology for responding to the emerging needs of electronics component and system irradiation; as well as combining different irradiation and simulation techniques for optimizing the radiation hardness assurance for systems, focusing on the related risk assessment.

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