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System on Chip based compact NQR Spectrometer

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► **To cite this version:**

Noreddine Kachkachi, Axel Gansmuller, Hassan Rabah. System on Chip based compact NQR Spectrometer. Colloque 2021 du GDR-SOC2 du CNRS, Jun 2021, Rennes, France. hal-04578093

HAL Id: hal-04578093

<https://hal.science/hal-04578093>

Submitted on 16 May 2024

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(1) NUCLEAR QUADRUPOLEAR RESONANCE

NQR(Nuclear Quadrupolar Resonance) is a spectroscopy technique that is used to study nuclei with spin superior to 1/2 like ^{127}I , ^{37}Cl , ^{27}Al and ^{14}N [1]. Though the NQR technique offers a wide range of applications, it suffers from various problems which are caused by its low sensitivity.

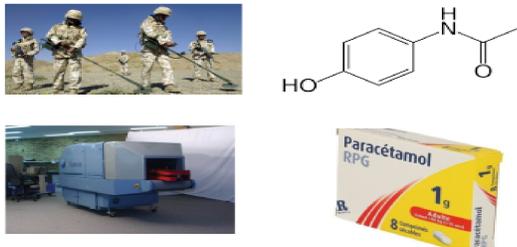


Fig. 1 NQR applications.

Several portable spectrometers were presented in the literature, but those applied to NQR had some crucial RF parts still in the analog domain, and performances (e.g. pulser time resolution and pulse width) were limited [2].

(2) PROPOSED SOLUTION

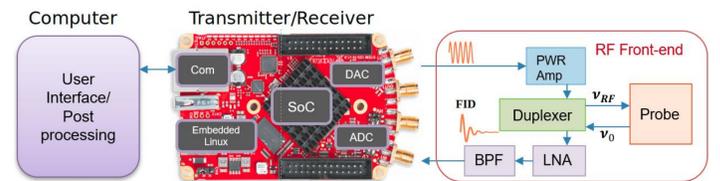


Fig. 2 New NQR spectrometer.

In this work we present a System on Chip solution integrating the major blocks of the spectrometer including, a high resolution pulser, a fully controllable pulse transmitter, an acquisition module, and a hardware debugger. The objective is to increase portability, sensitivity and immunity to various noise sources.

(3) SoC DESIGN AND VERIFICATION

The proposed spectrometer architecture is based on the Redpitaya board which embeds an AP-SoC (All Programmable SoC) Zynq 70x0 FPGA from Xilinx [3].

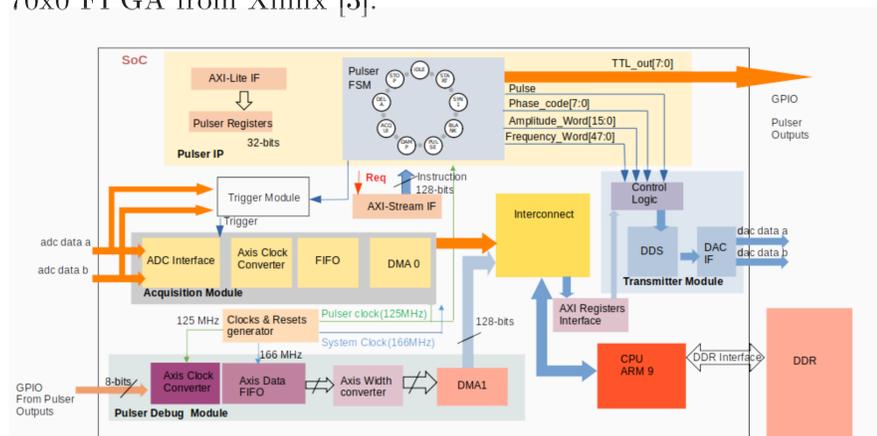


Fig. 3 SoC architecture.

In the proposed solution, all the traditional analog parts are replaced by digital blocks inside the FPGA.

SoC Architecture and Design:

The transmitter module produces the RF excitation signal that was generated by the DDS and modulated by the the pulser's outputs. The acquisition module acquires the digitized incoming signal FID(Free Induction Decay). The FID is then sent via Ethernet to the post-processing unit located in the computer. The pulser module orchestrates the functioning of the whole system.

The SoC is composed of:

- **An acquisition module** that handles the incoming signal FID and stores it inside the DDR via a DMA
- **A Pulser module** It generates the pulse sequence control signals (8 ns resolution).
- **A transmitter module** which is based on a Xilinx DDS that is controlled in phase, frequency and amplitude
- **A debug module** which is used to test functionality of the Pulser on the FPGA target
- **A backbone** : Composed of the processor sub-system, the AXI-Interconnect and the clocking wizard

SoC Verification and validation:

A complete verification platform was built. The verification environment is composed of a System Verilog Testbench, a pulser C Model, a tests database which contains for each experiment the pulser's instructions, and reference files for the experiment which are the pulser's expected outputs and the expected FID.

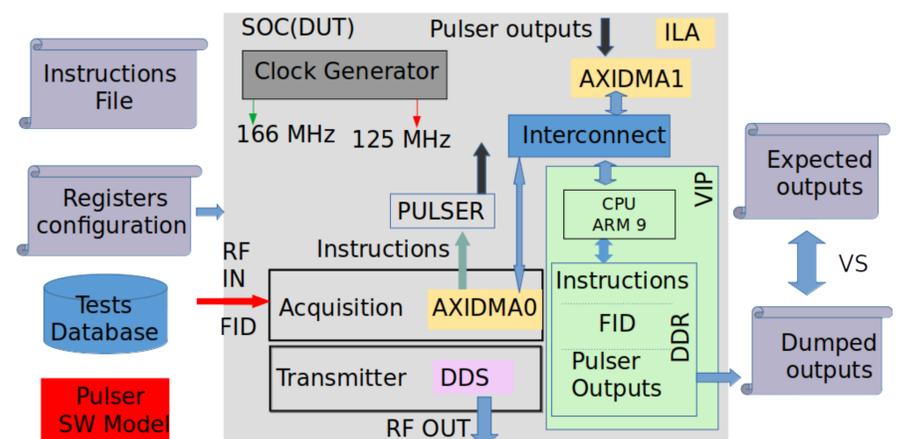


Fig. 4 SoC verification

The testbench is used to simulate different scenarii of an NQR experiment. A set of three output files is generated which are direct pulser outputs file, re-injected pulser outputs file, and a FID output file. A comparison is performed after simulation between the expected values and the actual ones.

After being implemented with Vivado, the design was validated on FPGA target. To validate the pulser on board, pulser's outputs are re-injected into the SoC, written in the DDR and then dumped in a file in order to be checked against the previously computed references. The acquisition functionality was tested by acquiring sinusoidal signals generated by an external waveform generator. The transmitter functionality was tested by the oscilloscope. Linux applications were written in order to drive the pulser, the acquisition and the spectrometer. The embedded system was then integrated with the spectrometer software to validate the system level behavior.

(4) CONCLUSION

Thanks to rigorous verification, design robustness and fast bug tracking, considerable instrument miniaturization was achieved. The current system results in a compact NQR spectrometer. In the developed system, a fully controllable RF pulse is generated and a signal generated by an RF generator was correctly acquired. Next steps are the acquisition of signal FIDs coming from real samples. Additional signal denoising algorithms will be further implemented on the FPGA module in order to enhance the spectrometer sensitivity.

(5) REFERENCES

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