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System on Chip based compact NQR Spectrometer

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Abstract

Nuclear Quadrupole Resonance (NQR) is a radio frequency spectroscopy technique providing high resolution molecular structure analysis of solid materials containing quadrupole atomic nuclei. Despite its relatively low sensitivity, the fact that no heavy equipment is needed to generate the spin polarization makes it potentially very useful for low cost and portable applications. The challenges of NQR instrumentation are therefore to increase its portability and sensitivity, and limit interference from various noises sources (e.g. radio frequency inference), in order to perform field applications outside the laboratory. To address this challenge, we present a System on Chip solution (SoC) integrating the major blocks of the spectrometer including: a high time resolution pulser, a fully controllable pulse transmitter, an acquisition module, and a hardware debugger. The design of the proposed solution is verified using behavioral simulation and validated on board. While most recent compact spectrometers still have crucial RF parts in the analog domain, our hardware and software modules are directly implemented on the Xilinx Zynq FPGA.

1. Introduction

Nuclear Quadrupolar Resonance is a spectroscopy technique that is used to study nuclei with spin superior to 1/2 like ^{127}I , ^{37}Cl , ^{27}Al and ^{14}N [1]. Though the NQR technique offers a wide range of applications, it suffers from various problems which are its low sensitivity, susceptibility to radio-frequency interference, and other background noises.

Several portable spectrometers were presented in the literature, but those applied to NQR had some crucial RF parts still in the analog domain, and performances (e.g. pulser time resolution and pulse width) were limited [2].

In this work we present a System on Chip solution integrating the major blocks of the spectrometer including, a high time resolution pulser, a fully controllable pulse transmitter, an acquisition module, and a hardware debugger. We first provide the details of the proposed architecture in section 2, and then explain the design and verification methodology in section 3. The results are summarized in section 4.

2. Proposed architecture

The instrumentation of NQR spectroscopy is principally composed of four main building blocks; the transmitter, the radio frequency front-end, the receiver and a computer. In a NQR experiment, an excitation RF signal is generated by the transmitter at a frequency ν_{RF} and sent after amplification to the probe that irradiates the sample. The nuclei generates then an NQR response signal called FID (Free Induction Decay) having a frequency ν_0 . After being pre-amplified by a LNA (Low Noise Amplifier), FID is acquired by the acquisition module and then post-processed by software.

The proposed spectrometer architecture is based on the Redpitaya board which embeds an AP-SoC (All Programmable SoC) Zynq 70x0 FPGA from Xilinx [3]. The developments of the current SoC were inspired by the available platforms (Ecosystem, Scripts, Linux applications, Makefiles, SoC projects on Xilinx AP-SoC,...) that were developed by the Redpitaya team and by P. Demin [4, 5]. The first intended applications of the new NQR spectrometer will be ^{14}N based materials analysis like Sodium Nitrate and paracetamol [6, 7].

In the proposed solution, (Figure 1), all the traditional analog parts are replaced by digital blocks inside the FPGA. The Pulser board is replaced by a home made IP coded in VHDL Language. Also an important part of software (Acquisition software) runs on the embedded system instead of the computer.

The SoC is composed of:

1. **An acquisition module** that handles the incoming signal FID (Free Induction Decay) and stores it inside the DDR via a DMA
2. **A Pulser module** It generates the pulse sequence control signals (8 ns time resolution).
3. **A transmitter module** which is based on a Xilinx DDS, that can be controlled by the pulser or by the SW, in phase, frequency and amplitude
4. **A debug module** which is used to test functionality of the Pulser on the FPGA target
5. **A backbone** Composed of the processor sub-system, the AXI-Interconnect and the clocking wizard

3. SoC Verification and validation

In order to fully verify and validate the SoC on simulation and on target, a complete verification platform (Fig-

