CMS iRPC FEB development and validation

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ABSTRACT

In view of the High Luminosity upgrade of the CERN LHC, the forward CMS Muon spectrometer will be extended with two new stations of improved Resistive Plate Chambers (iRPC) covering the pseudorapidity range from 1.8 to 2.4. Compared to the present RPC system, the gap thickness is reduced to lower the avalanche charge, and an innovative 2D strip readout geometry is proposed. These improvements will allow iRPC detector to cope with higher background rates. A new Front-End-Board (FEB) is designed to readout iRPC signals with a threshold as low as 30 fC and an integrated Time Digital Converter with a resolution of 30 ps. In addition, the communication bandwidth is significantly increased by using optical fibers. The history, final design, certification, and calibration of this FEB are presented.

1. Introduction

During the High Luminosity CERN LHC (HL-LHC) operation phase, the instantaneous luminosity will be increased to $5 - 7.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, i.e., a factor 5–7.5 above the LHC design value. The projected integrated luminosity of $300\,\mathrm{fb}^{-1}$ for Phase-1, the current LHC period, will be increased by an order of magnitude to $3000–4000\,\mathrm{fb}^{-1}$ in the coming two decades (Phase-2). The CMS experiment [1] at the LHC is implementing several upgrades to the present detector to improve the sensitivity to physics searches and to cope with: (i) the increased backgrounds; (ii) the larger pileup event rates; and (iii) the probable aging of the existing chambers. One upgrade includes the addition of new chambers in the muon endcaps [2].

Presently, CMS Resistive Plate Chambers (RPC) cover pseudorapidity up to $\eta = 1.8$, a region where two different muon systems always guarantee the coverage: Drift Tubes + RPCs in the barrel and Cathode Strip Chambers (CSC) + RPCs in the endcap. However, the forward region, $\eta > 1.8$, is covered only by the CSC system so it lacks redundancy where the background is highest and the magnetic field bending is lowest. Therefore, for the HL-LHC phase, the forward region of CMS will be complemented by three GEM (Gas Electron Multiplier) detector stations, and two improved RPC stations (iRPC) covering up to $|\eta| = 2.4$.

We modified the design of the iRPC chambers to cope with a higher background rate; an innovative 2D readout with narrow strip pitch (less than 1 cm) is used, taking advantage of the better timing to obtain the particle position with a centimeteric precision. The charge produced during the amplification process in the gas gaps is reduced to limit the electrode aging over time.

We designed a dedicated Front-End-Board (FEB) to read out the induced iRPC signal, discriminate it, and tag it in time with a precision of 100 ps. The design of the chamber and readout system is described in Section 2. Section 3 describes the FEB itself. The certification and calibration processes are described in Sections 4 and 5. Finally, Section 6 provides the state-of-the-art radiation tolerance details.

2. The iRPC readout design

The details of the iRPC chamber are described elsewhere [3], and an exploded view is provided in Fig. 1. In a nutshell, they are trapezoidal-shaped double gas gap chambers similar to the existing endcap RPCs with radially oriented readout strips between two gas gaps. These gaps are made of two High-Pressure Laminate (HPL) electrodes coated with a thin graphite resistive layer. The thickness of the electrodes, as well as the gas gaps, are reduced from 2 mm to 1.4 mm. The reduced thickness results in a lower charge produced in the gap as well as a lower screening effect from the thinner electrodes. The resulting pick-up charge by the strips is a factor of three lower than for a standard RPC chamber.

The strips are located inside a three-layer trapezoidal Printed Circuit Board (PCB) containing 48 readout strips with pitch width varying from 12.3 mm in the large base to 6 mm in the small base. Two PCBs are used per chamber: left and right. The signal propagates to both ends of the strip and is carried via narrow return-lines to three Enhanced Routing Network Interconnect (ERNI) connectors per PCB located in the wide edge of the trapezoid. This position is located furthest possible from the beam axis and benefits from the lowest irradiation level. The reference. [4] provides more details about the PCB.

For each PCB, one FEB is connected via the ERNI connectors. A copper plate is fixed on top of the FEB for temperature control. It plays the role of local ground reference and partial Faraday cage. On top, a stainless steel cover encapsulates the readout system nearly hermetically and complements the Faraday cage.

3. The iRPC front-end-board

The iRPC FEB version 2 (FEB v2) is a low-noise front-end electronics board capable of detecting signals with a charge as low as 30 fC. The FEB was designed in 2019–2020, produced in 2021, and certified in 2022. A photo of the board is provided in Fig. 2 and the schematic in Fig. 3. This version of the FEB is used for the iRPC demonstrator installed at the end of the Long Shutdown 2 in 2021. The previous version of the FEB is described in Ref. [5] and served as proof of principle of this innovative 2D readout system and certification of the iRPC engineering prototype.

The 48×2 signals are transferred to FEB v2. It hosts six Petiroc 2C ASIC controlled by three Cyclone-V FPGAs. The CERN GBTx chip (high radiation tolerance) is used for the data transfer through the VTRx transceiver to the back-end-board (BEB) [6]. This board communicates with the CMS Muon Level 1 trigger and stores hits for the data acquisition chain. The BEB performs slow control through the CERN SCA ASIC.

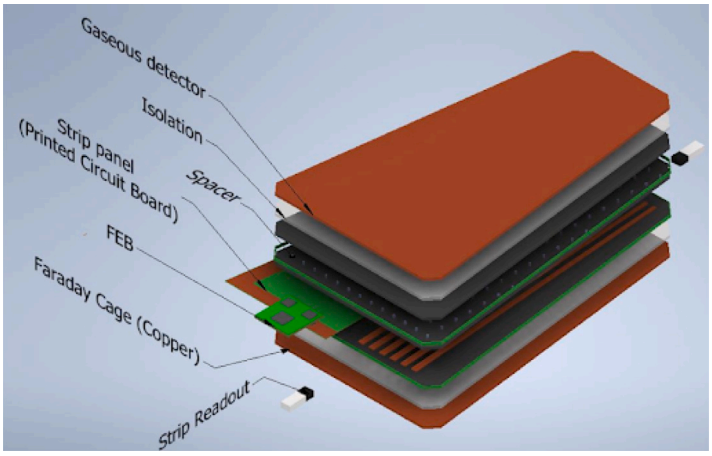

Fig. 1. Exploded view of the iRPC detector.

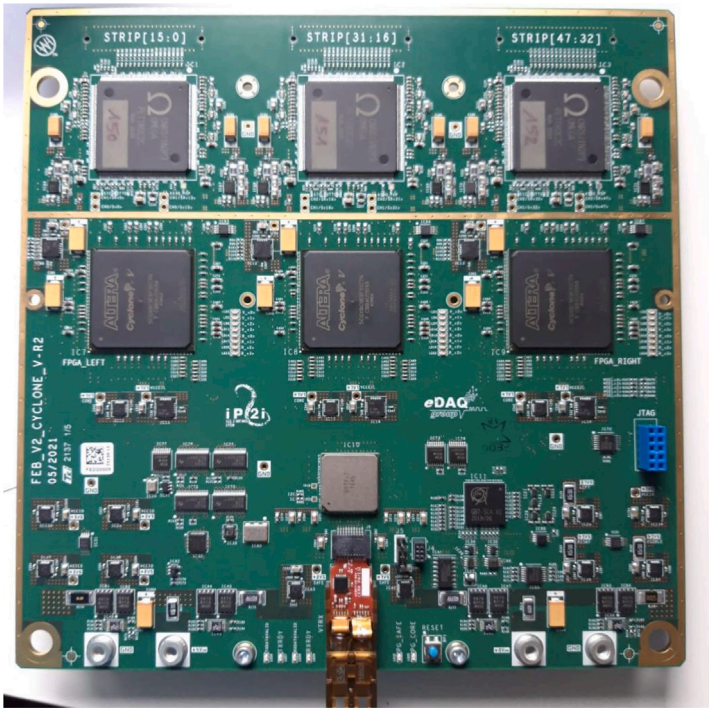

Fig. 2. Photo of a FEB v2 from top view.

The fast front-end ASIC, PETIROC2 [7], is a 32 channel version developed in AMS 0.35 µm SiGe technology. It hosts a preamplifier with a 1 GHz bandwidth and gain of 25 associated with a fast programmable comparator.

The first version of this ASIC was designed to read out silicon photomultipliers (SiPM) for particle time-of-flight measurement applications. It was successfully modified into version 2B, including features to reduce the cross talk among Petiroc channels, and finally, 2C, which can be considered a real *iRPCROC*. In this version, many analogical components that are useful for SiPM, but not for RPC, are removed. In addition, a channel-by-channel auto-reset feature is added to shut down each Petiroc channel for a period of few dozens of ns after the trigger signal is issued. This feature reduces retriggering effects in the chip significantly. Using Petiroc2C and an auto-reset time of ≈ 25 ns, it is possible to reach thresholds for the pickup signal of the order of 30 fC, while Petiroc2A is limited to O(100 fC). The resulting deadtime can be considered as negligible (well below 1%).

The signal received through the ERNI connector is pre-amplified and discriminated inside the Petiroc2C chip. It is then transferred to Altera Cyclone V FPGA, which provides the time-to-digital conversion module. The FEB hosts 3 FPGAs, each controlling 2 Petiroc2C chips. Each FGPA contains a Time Digital Converter (TDC) module using a tapped-delay-line architecture [8].

The central master FPGA also serves as a concentrator of the signals collected by all 3 FPGAs. The signal is packaged into frames and transferred to the GBTx chip.

The FEB is supplied by 2 low voltage (LV) lines: 2 V and 4 V. The former provides power mainly to the FPGA and consumes $\approx$ 6.5 A, whereas the latter $\approx$ 2.3 A. The total power consumption amounts to 22 W, which is efficiently evacuated using a fan in the laboratory or cold water in CMS.

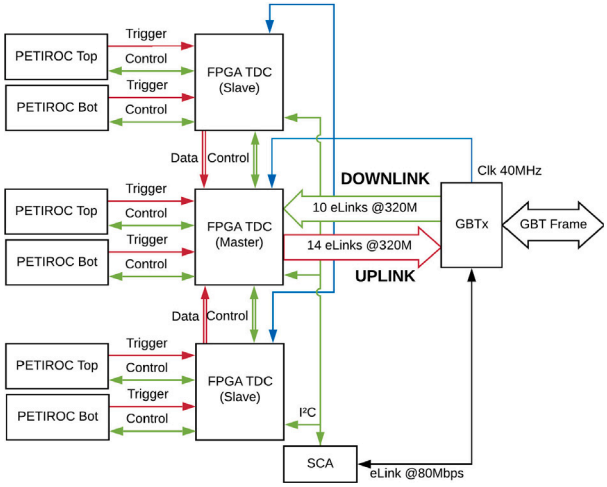

Fig. 3. FEB v2 schematic.

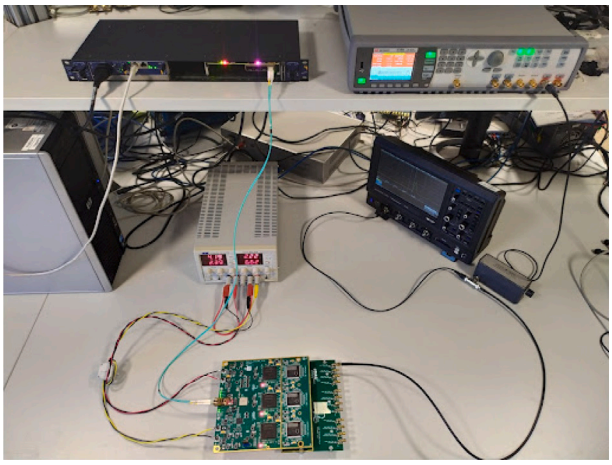

Fig. 4. A photo of the certification chain in IP2I Laboratory in Lyon, France.

4. FEB v2 certification

The certification of the FEB v2 is performed by a simplified standalone data acquisition system based on the CERN FC7 mezzanine card[1] inserted into a μTCA mini-crate. This system is portable and flexible. It is designed to read out one FEB at a time.

So far 18 FEBs have been produced: the PCB is manufactured by French company TECHCI and assembled by another French company FEDD.[2] Among them, 8 FEBs are installed on the iRPC demonstrator in 2021, and 10 others are used for project certification.[3] The certification setup is shown in Fig. 4, and the initial test steps at IP2I laboratory (Lyon, France) are the following:

1. Test independently each FEB electronic block: SCA, GBTx, Power Supplies, and tests points.
2. The data integrity of the system is verified.
3. The firmware for the FPGA is flashed into the FEB and validated.
4. The Petiroc2C and FPGA are operated.
5. Simulation and system operation checks are performed using an injection chain, including a generator, resistance, and capacitor. This approach allows us to emulate as close as possible the typical iRPC signal.
6. A common signal is injected into all channels to measure their relative delays with respect to each other, which are later stored in a look-up table. These delays are observed to be stable in time. A typical delay of ≤ 10 ns can be observed due to various connection lengths within the FEB and firmware implementation inside the FPGA.

5. FEB v2 calibration

In the second step, the Petiroc2C pedestals have to be individually aligned. A unique discriminator threshold THR is set for all the ASIC using a 10-bit Digital Analog Converter (DAC). For a given channel, if THR is too low, the channel would continuously trigger on noise, if it is too high the triggers count will be 0. The transition between the two regimes is called a pedestal: PD. For each channel i the PD_i is individually measured. To align all PD_i to a unique PD per ASIC, each channel is supplied with a 6-bit DAC tuner: it can shift PD_i up and down. A dedicated multi-step procedure was designed to perform a fine alignment of PD_i to a median PD on the test bench or a chamber. This procedure requires 30 mn. The obtained 6-bit DAC constants are tabulated in a database. After one year of operation of the iRPC demonstrator chambers, we verified that they do not change significantly over time.

The real signal threshold THR is defined by the relation THR = PD + eTHR, where eTHR is called effective threshold. The value of eTHR=7 DAC [9] that we use is the minimal value possible that guarantees a negligible noise level in the chamber (less than 1 Hz/cm^2).

The third step consists in converting the value of eTHR into an avalanche signal charge. The same injection setup shown in Fig. 4 is used to perform this operation. The response of the Petiroc2C in fC depends on the sharpness of the leading edge. A dedicated study performed with a high-frequency oscilloscope has shown that the typical rising time (since the induced signal is negative, it appears as *falling time*) of an iRPC signal is around 2 ns. The conversion factor for the iRPC signal is

$$\text{eTHR} = 4.6 \pm 0.05\ \text{fC/DAC} \quad (1)$$

A perfect linearity is observed between 50 and 500 fC. Below this value, a linear extrapolation is assumed since the injection circuit did not allow injecting a lower signal. Therefore 7 DAC converts into 32 fC.

The resolution and linearity of the TDC module were measured using the injection circuit with two channels: one trigger channel considered as a time reference and one test channel using the BEB setup. The results are shown in Fig. 5. A resolution of $\approx$ 20 ps for a TDC channel is obtained. The difference in time ΔT between the two channels is varied adding a *delay line*. A perfect linearity is observed.

The TDC resolution is negligible compared to the relative time resolution between 2 strips ends of the iRPC chamber of 160 ps [6]. This quantity is fundamental since it is used to reconstruct the position along the strip.

Furthermore the operations of the iRPC demonstrator have demonstrated that the FEB can operate without any problems in a magnetic field of $\approx$ 0.5 T. Finally, we verified that the total noise level of the system FEB and iRPC chamber stays below 1 Hz/cm^2, that is well within the requirements.

6. FEB v2 radiation tolerance

The iRPC chamber is designed to shield the FEB from the radiation flux as much as possible. Therefore, the FEB is located 3 m from the

[1] More information can be found there.

[2] We thank the TECHCI and FEDD companies for their continuous and proactive support in this project.

[3] Two out of four iRPC demo chambers are equipped with an earlier FEB version v2.1 with Petiroc2B and have a less performing design.

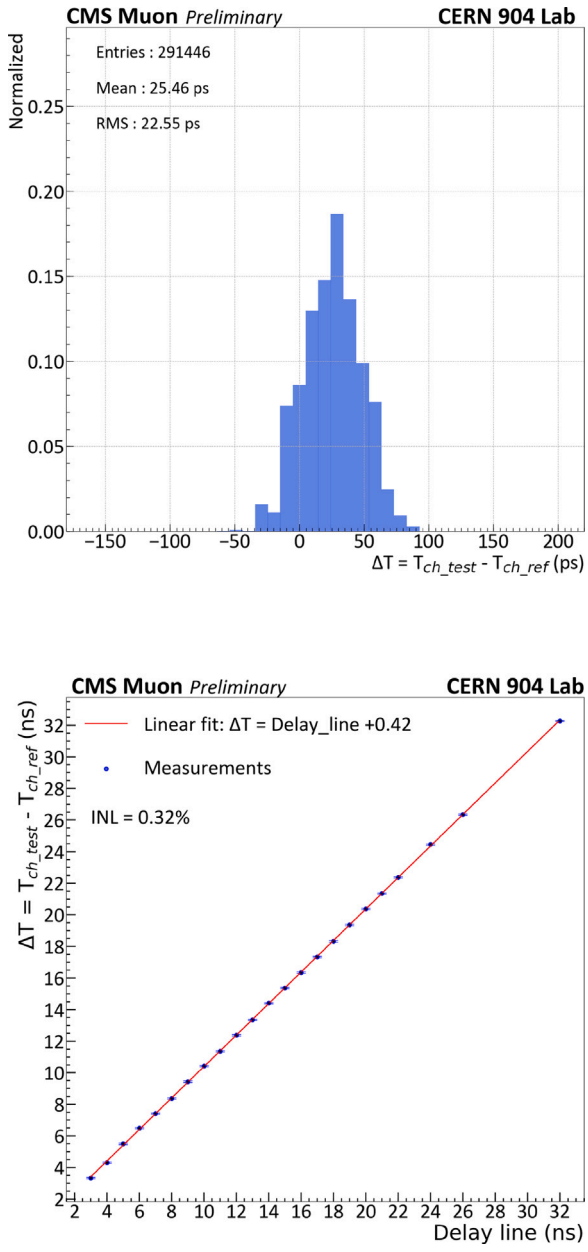

Fig. 5. Top: resolution of the iRPC TDC module; Bottom: linearity of the TDC module.

beam axis, which is the furthest possible distance. In this region the radiation dose is considered "moderate" for the LHC. This means that it is lower than inside the CMS tracker system where specific high radiation tolerant components are required. However, it is still not negligible for a standard commercial component such as Cyclone V. A dedicated campaign is, therefore, necessary to know if FEB v2 can withstand 10 years of HL-LHC operations.

The typical fluences and fluxes estimated by FLUKA simulation for the iRPC FEB [10] are provided in Table 1. The certification followed three steps with increasing severity of the irradiation.

As a first step, the FEB was operated under irradiation of an intensive ^{60}Co source at the Calliope facility located at ENEA Casaccia, Italy. The flux was set to 6.7 Gy/h on the Petirocs, while Cyclone V was protected by lead and received only 2.2 Gy/h. During 23 h of the test, the HL-LHC dose with safety factor (SF) > 2.5 was collected. No aging was observed: pedestals and gain of the Petirocs were unchanged, and currents and temperature were stable. No Single Events Upset (SEU) or Single Events Latchup (SEL) was identified during the test.

Table 1
Summary of the irradiation tests of FEB v2: 1st column is the type of particles used in the facility; 2nd column gives the Total integrated dose (TID), fluence, or the flux of these particles expected at HL-LHC depending on the quantity under scrutiny (high energy neutron flux and fluence is expressed in 1 MeV neutrons equivalent); 3rd column indicates the facility; 4th column shows the safety factor achieved during the test.

Particles type	HL-LHC conditions	Valid. facility	SF
^{60}Co γ	20 Gy	Calliope	2.5–8
Neq 1 MeV	6e11 cm^{-2}	FNG	3
	10e3 cm^{-2}s^{-1}	FNG	30
ThN/HEH		CHARM	Ongoing

After the success of the γ test, the FEB was installed into the 14 MeV neutron source in FNG, Enea Frascati, Italy[4] [11]. At the beginning of the test, the FEB was operated at fluxes going from a safety factor 1 up to 300 during periods of 20 min. No issues were observed below SF = 30, whereas above, errors in the TDC output were identified, indicating a possibility of SEU in the FPGA.

After this first phase, the FEB was set to standby mode and irradiated to a total neutron fluence of HL-LHC with a safety factor of 3 for 8 h. After this period, the FEB is being operated again, and no aging issues were observed.

The most demanding test with a mixed field of High Energy Hadrons (HEH) and thermal neutrons (ThN) is ongoing in the CHARM CERN facility at CERN. Additional tests using the FEB on the iRPC demonstrator at CMS are ongoing at 20%–30% of the HL-LHC instantaneous luminosity.

7. Conclusions

The RPC system coverage will be extended to $|\eta|$= 2.4 by installing iRPC chambers in the forward region on the 3rd endcap disk of the CMS experiment to cope with the HL-LHC conditions where they have to withstand much higher background and irradiation rates. A dedicated readout system and an innovative FEB are designed, built, and certified. The FEB fulfills the requirements to operate safely in the HL-LHC environment. The irradiation tests carried out now are promising, and final tests are still ongoing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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