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Ahmed Sabry Eltahir Ahmed, Rémi Perrin, Guillaume Lefevre, Cyril Buttay, Jacques Jay. Graphite Heat Spreader Embedded in a PCB Package for Improved SiC Die RthJC. 2023 IEEE Energy Conversion Congress and Exposition (ECCE), Oct 2023, Nashville, United States. pp.5543-5550, 10.1109/ECCE53617.2023.10362229 . hal-04567191

HAL Id: hal-04567191

<https://hal.science/hal-04567191v1>

Submitted on 3 May 2024

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Graphite Heat Spreader Embedded in a PCB Package for Improved SiC Die RthJC

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Abstract—This paper presents a printed circuit board (PCB)-based packaging with a heat spreading feature suitable for wide band gap devices and high-power loss density requirements. Embedding of power semiconductor devices inside a printed circuit board stack is a promising solution to reduce circuit parasitics, simplify device packaging, and reduce cost. However, the reduction in chip size enabled by wide-bandgap (WBG) semiconductors, together with the poor thermal conductivity of the insulating layers of PCBs present some challenges compared with direct die solder on thick conductive substrate. In this paper, a graphite heat spreader technique designed to be compatible with PCB embedding technology is demonstrated. A specific graphite spreading stack is fabricated and compared with a reference sample. At last, through simulation and experimental analysis, the electrical and thermal behavior of the different samples are evaluated.

Keywords—PCB, packaging, thermal management, graphite, heat spreading, MOSFET, SiC, PCB embedding, FEM.

I. INTRODUCTION

In the coming years, e-mobility will act as a boost for new technologies in power electronics. Among the emerging solutions, embedding a die in the PCB is one of the most promising to supplant the standard power module technology with DBC substrate and wire bonding [1].

The embedded die packaging (Fig. 1) with its low parasitic interconnection and low cost is perfectly suited for wide band gap devices such as SiC MOSFET [2]. However, performances have to come along with low cost, high reliability and good thermal management to ensure a new technology is competitive against established ones. Despite the intrinsic low cost of PCB manufacturing, SiC devices remains more expensive than their Si counterpart. Indeed, the SiC substrate fabrication is time and energy consuming with a lower yield compared to silicon, resulting in smaller wafer size and higher cost power module. Regarding this blocking point, trench type SiC MOSFETs offer the advantage of reducing the total die footprint by using a vertical channel in the semiconductor compared to the more classical planar structure, resulting in smaller dies at each new

device generation. However, this footprint reduction comes with higher power loss density and a smaller area for heat extraction when considering the pitch limitation of laser-drilled vias in the case of the PCB packaging. Thermal management of WBG devices is thus becoming challenging with regard to the PCB embedding environment.

In PCBs, the dielectric is often an epoxy-based material with a poor thermal conductivity ($< 1 \text{ W}/(\text{m}\cdot\text{K})$) compared to the copper of the conductive layer, limiting heat spreading around the die. To overcome this limiting point of the package, we propose to insert a material with high-thermal conductivity in the PCB stack: layered pyrolytic graphite material, with its anisotropic thermal conductivity that can go up to $1500 \text{ W}/(\text{m}\cdot\text{K})$ in-plane, offers the advantage of an alternative lateral path for the heat. This lateral path adds to the natural vertical one offered by the copper vias, connecting the top and bottom of the die, resulting in an

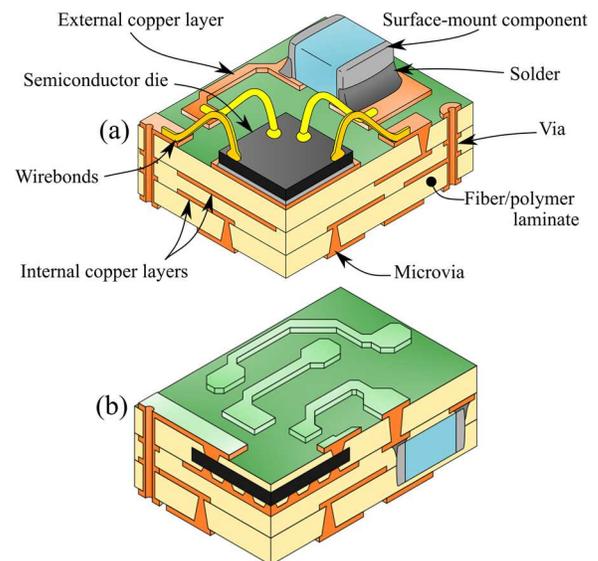


Fig. 1. (a) Classical PCB package. (b) Embedded PCB package.

improved thermal performance. Moreover, several manufacturers propose raw materials [3] as well as metalized ones [4] showing compatibility of the graphite with manufacturing process.

PCB package samples with embedded SiC dies and graphite were designed, fabricated, and experimentally validated. The PCB manufacturing process is presented as well as the thermal performance of PCB samples with graphite compared to a reference PCB samples without graphite.

II. PCB EMBEDDING PROCESS WITH GRAPHITE

Pyrolytic graphite is commercially available (Panasonic EYGS091205) in the form of sheets which makes it a suitable heat spreader to be embedded in a PCB package. Pyrolytic graphite sheet (PGS) is offered at a price of ~ 0.08 $\$/\text{cm}^2$. PGS of $50 \mu\text{m}$ thickness with $1300 \text{ W}/(\text{m K})$ in-plane thermal conductivity are selected. The cross-plane thermal conductivity is only $15 \text{ W}/(\text{m K})$.

The objective here is to integrate graphite heat spreader in a PCB stack without altering the PCB manufacturing process and embedding technology. This is described in this section.

A. PCB Manufacturing process.

As illustrated in Fig. 2, the PCB manufacturing process starts by stacking up conductive layers (copper) and dielectric layers (epoxy). The SiC chip is placed in a cavity of an epoxy layer.

After that, the stack-up is laminated resulting in a die embedded in a solid PCB. In order to interconnect the embedded chip to outer copper layers, vias are drilled by laser on both sides of the PCB package (Fig. 2). In addition, through-hole vias are drilled mechanically to interconnect top and bottom external copper layers. Drilled vias are then plated with copper by electrodeposition process. Finally, copper layers are chemically etched to form electrical connection copper tracks.

B. Fabrication of PCB samples with embedded graphite

In this proposed PCB package, the concept is to spread the heat laterally in addition to the vertical heat path provided by copper vias in the classical stack. Low thermal resistance path is provided for the heat; vertically through copper vias, and laterally through graphite. The combination of a vertical thermal path, offered by the vias, and a lateral one with graphite layers results in an efficient spreading effect to extract the heat as close to the chip as possible and to spread the heat within the PCB before reaching the isolation barrier of a cooling system.

Two graphite layers are stacked in a cavity of an epoxy layer (the same way the chip was placed) as shown in Fig. 2, together with thin adhesive layers (DuPont Pyralux LF0100) with $25 \mu\text{m}$ thickness and $0.22 \text{ W}/(\text{m.K})$ isotropic thermal conductivity. After that, the same steps of PCB manufacturing are applied. The stack-up is laminated, micro vias are UV laser drilled through graphite, then plated with copper using electrodeposition, and finally copper is etched to form copper tracks for electrical connection (Fig. 2). Fig. 3 presents some of the samples which are produced. The total thickness of the PCB is about 0.8 mm . Two heat spreading areas are considered around the chips: $20 \times 20 \text{ mm}^2$ or $10 \times 10 \text{ mm}^2$. Fig. 4 shows the good contact between copper vias (vertical thermal path) and graphite sheets (lateral thermal path) which is a key point to spread the heat.

C. PCB variants

Several PCB samples with different sizes and vias patterns are fabricated. One series of sample embeds SiC diode chips, while the other embeds SiC MOSFET chips, to evaluate the manufacturing difficulty associated with the gate contact. Embedded diodes and MOSFET chips have comparable sizes (Diode chip size is $3.1 \times 2.86 \times 0.24 \text{ mm}^3$ and MOSFET chip size is $3.36 \times 3.1 \times 0.21 \text{ mm}^3$). Fig. 5 shows the different PCB variants while Table I shows the characteristics of fabricated PCB samples.

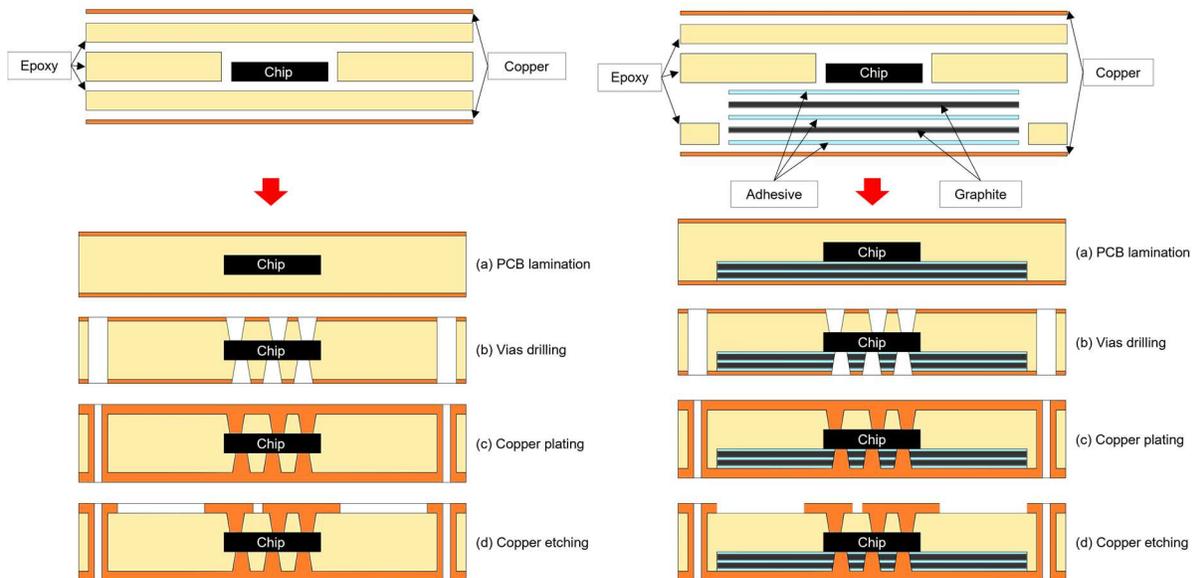


Fig. 2. PCB manufacturing process of a classical stack (left) compared to PCB stack with embedded graphite heat spreaders (right).

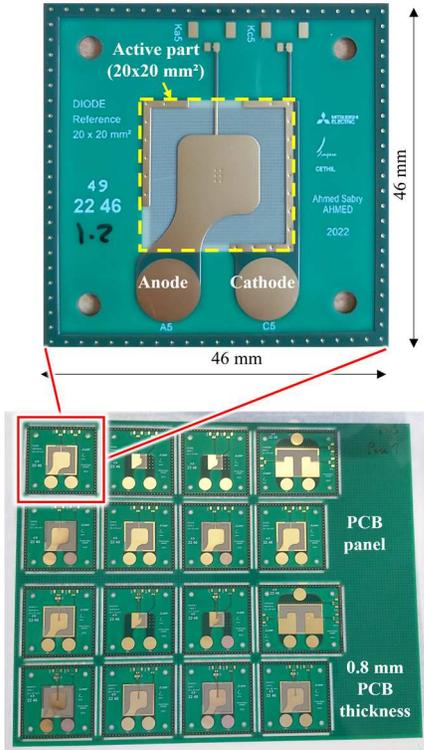


Fig. 3. Fabricated PCB samples.

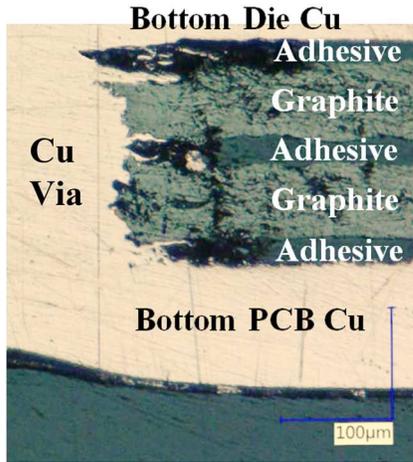


Fig. 4. Cross-section of a PCB sample with graphite showing copper via through graphite/adhesive stack.

TABLE I. FABRICATED PCB VARIANTS

Diode samples	Active part area	Vias patten	Graphite	MOSFET samples
D22R	20x20 mm ²	No distributed vias	No	M22R
D22Ga	20x20 mm ²	distributed vias all over the active part	Yes	M22Ga
D22Gb	20x20 mm ²	distributed vias on the periphery	Yes	M22Gb
D22Gc	20x20 mm ²	No distributed vias	Yes	M22Gc
D11R	10x10 mm ²	No distributed vias	No	M11R
D11Ga	10x10 mm ²	distributed vias all over the active part	Yes	M11Ga

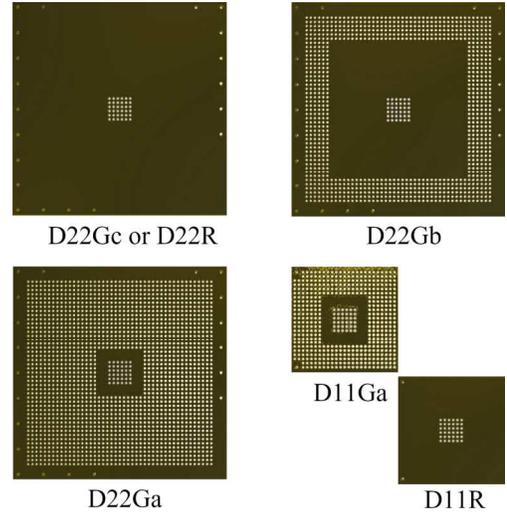


Fig. 5. Different Vias Patterns and Sizes of PCB samples.

III. ELECTRICAL CHARACTERIZATION TESTS

Electrical characterization tests of the 55 diodes and 42 MOSFETs samples are performed using a curve tracer (Keysight B1505A). Comparison is made with devices specification to detect any drift which may have been caused by embedding process. In this paper, only the parameters for which some chips show deviation with the specifications are presented. Regarding MOSFETs, gate threshold voltage (V_{ThGS}) as well as drain-source break-down voltage (V_{BV}) values are shown in Fig. 6. For diodes, break-down voltage (V_{BV}) values at high voltage are presented in Fig. 6. The tests conditions are:

- MOSFETs V_{thGS} measured at $V_{DS}=5$ V, $I_D = 10$ mA.
- MOSFETs V_{BV} measured at 10 μ A drain current.
- Diodes V_{BV} measured at 100 μ A anode current.

MOSFETs dies are CPM2-1200-0080B (1200 V, 36 A) with a minimum V_{BV} of 1200 V and minimum V_{ThGS} of 2 V [5]. In Fig. 6, results show that 36 MOSFETs have a V_{BV} higher than 1500 V while 38 MOSFETs have V_{ThGS} higher than 2 V. The diodes are SiC schottky devices and 47 of them have a V_{BV} higher than 700 V. In consequence, 86 % of the dies are found to be functional which is considered a good yield for the first batch. Some of non-functional samples show after cross-sectioning that the SiC diode was broken during fabrication (probably during the lamination process). This can result from miss-placing the die during stack-up process.

IV. THERMAL STRESS REFLOW TESTS

A thermal stress convection reflow test is performed on the PCB samples following the IPC-TM-650 standard [6]. This test simulates thermal cycles experienced by the PCB in soldering ovens. The maximum temperature of the temperature profile is 260 °C (corresponding to lead-free reflow cycle). The reflow test should be performed with a temperature profile between upper and lower specification limits (USL & LSL) as indicated in Fig. 7.

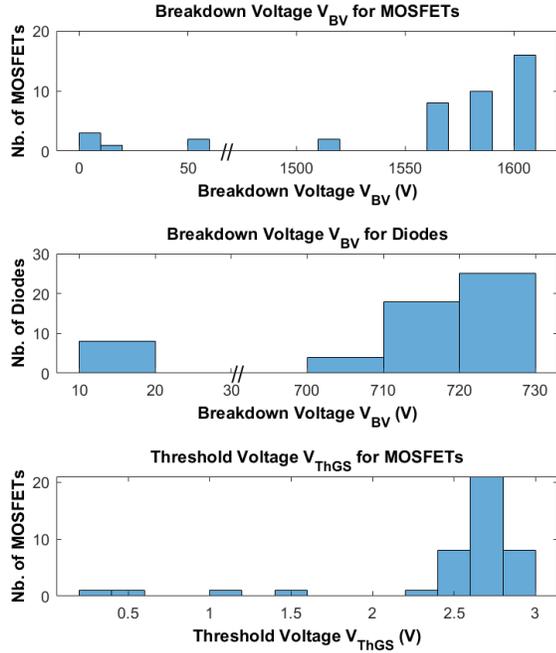


Fig. 6. Electrical characterization tests results.

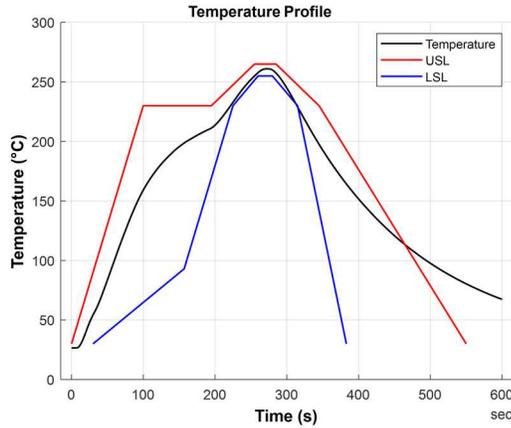


Fig. 7. Thermal reflow cycle showing temperature profile between USL and LSL profiles.

Fig. 8 shows profilometer measurements (Nano-Point-Scanner NPS-NP3) before and after reflow test to capture the deformation which may have been caused by the thermal stress. D22R and D22Ga are not affected by thermal stress cycles except for a little warping that can be observed. On the other hand, D22Gb show a swelling in the middle region where there are no micro vias. D22Gc exhibits swelling at the bottom edge as indicated in Fig. 8.

Graphite has low inter-layer shear strength and will exfoliate easily. This is consistent with the observation that PCB samples with graphite will exhibit swelling if not otherwise contained. Copper vias through the copper/adhesive/graphite stack form mechanical clamps which prevent delamination from propagating through the graphite layers.

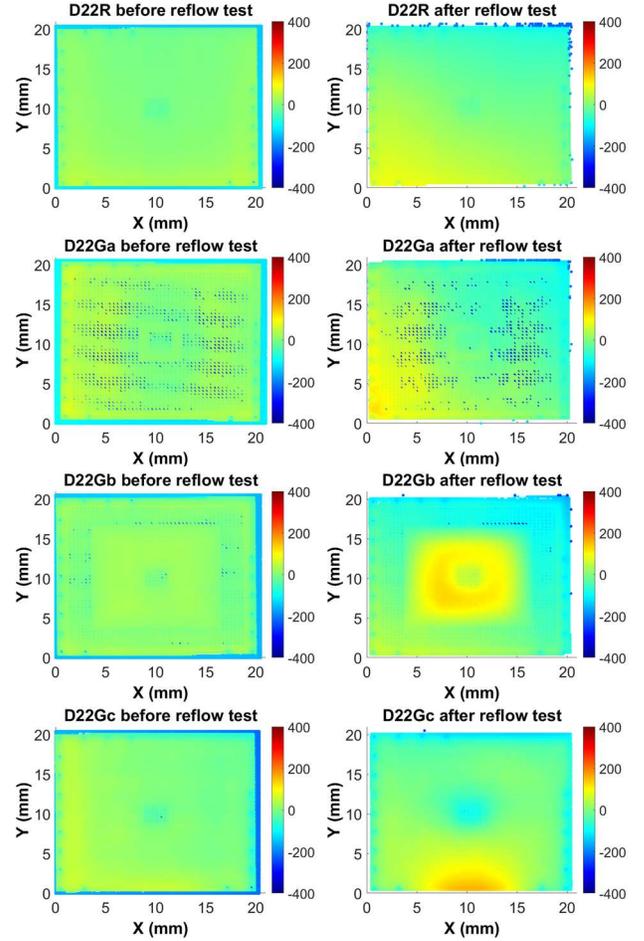


Fig. 8. Profile-meter pictures before and after thermal reflow tests.

Therefore, vias are important not only for providing vertical thermal path for the heat, but also for mechanical stability during thermal stress cycles.

V. TEST SETUP FOR THERMAL MEASUREMENT

Thermal impedance (Z_{th}) is the difference between chip junction temperature (T_j) at certain time during heating and a reference temperature (T_r) divided by input power (1):

$$Z_{thj-r}(t) = (T_j(t) - T_r) / Power \quad (1)$$

When the thermal impedance reaches a steady state, its value becomes equal to the junction to ambient thermal resistance (R_{thJA}) of the measured sample. The junction temperature T_j is obtained by measuring a Temperature-Sensitive Electrical Parameter (TSEP) of the semiconductor chip: the forward voltage drop of the diode (and of the body diode with a $V_{GS} = -5$ V bias in the MOSFET case) under a biasing current of 5 mA. The relationship between the TSEP value and the temperature is first calibrated in a calibration oven (with no power dissipated, assuming $T_j = T_r$). Fig. 9 shows the experimental test fixture for thermal impedance and thermal resistance tests.

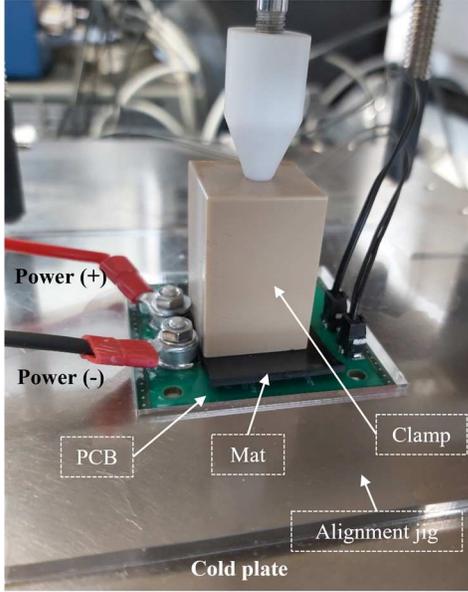


Fig. 9. Thermal impedance experimental setup.

The sample is clamped on a cold plate with a Thermal Interface Material (TIM: Sil-Pad®1500ST) and a pressure of 1.8 bar. An elastomeric mat (Viton) and a rigid PEEK block are used for homogenous distribution of the pressure on the 0.8 mm thick PCB sample. The cold plate is cooled by water with an inlet temperature of 23 °C, taken as the T_r for thermal impedance and thermal resistance calculation. An alignment jig is fixed on the cold plate so as to maintain PCB sample position in order to ensure the repeatability of the tests. Connectors are soldered on the PCB sample terminals to facilitate the electrical connection to power supply. The Z_{th} measurement is performed using a thermal analyzer (AnalysisTech Phase 12). This system automatically injects a given power level in the sample under test to force it to heat-up, and then monitors the TSEP value during the cooling down phase.

Since the thermal conductivity of SiC changes with temperature [7], the applied power is manually adjusted during measurements in order to keep T_j at a level of 65-70 °C regardless of PCB variant and TIM. This also allows to work at the same level of accuracy for the measured Z_{th} . For reference samples without graphite, the applied power is 11 W using the Sil-Pad TIM and 20 W using deionized water as a TIM. For samples with graphite, 16 W are applied using the Sil-Pad and 24-32 W using deionized water.

A. Thermal impedance measurements

Thermal impedance (Z_{th}) measurements are performed on all PCB variants with graphite and compared to the reference sample (which does not contain graphite). Accuracy estimation shows $\pm 0.5^\circ\text{C}$ for T_j measurements as well as $\pm 0.5^\circ\text{C}$ for the “T-type” thermocouple that measures the water inlet temperature of the cold plate [8]. In addition, the calibration curve of the die introduces some more uncertainties: calibrating the same SiC chip several times results in an estimated variation of $\pm 1.7^\circ\text{C}$ in T_j due to calibration. As a result, a total $\pm 2.7^\circ\text{C}$ accuracy is considered for temperature difference ($T_j - T_r$). This in turn yields an accuracy estimation for the thermal

resistance R_{thJA} of around $\pm 6\%$ for a T_j of 70 °C. A lower T_j , i.e. a lower temperature difference ($T_j - T_r$) would lead to an even lower accuracy of R_{thJA} measurement. Other sources of error (estimation of the dissipated power, etc.) are considered negligible here.

B. R_{thJC} estimation using TDIM

The dual thermal interface method (TDIM, described in JEDEC51-14 standard [9]) is used to obtain the junction to case thermal resistance (R_{thJC}) of the samples. TDIM is a differential technique that is based on measuring thermal impedance with two different TIMs having significant difference in thermal resistance. The difference in TIM creates a change in the heat path which results in a separation between the two thermal impedance curves (Fig. 10). The separation point is assumed to take place at the interface between the PCB package and the TIM. Therefore, the thermal impedance value at which the separation takes place indicates the R_{thJC} . A custom MATLAB code is used to calculate R_{thJC} following TDIM according to JEDEC51-14 standard.

Table II shows the thermal conductivity (k) and the thickness of the two TIMs used in the measurements to estimate R_{thJC} : a commercial thermal pad, and 3 droplets of deionized water.

The accuracy of TDIM is reported to be within $\pm 20\%$ [10]. Adding to the accuracy of R_{thJA} , the estimation of R_{thJC} can have $\pm 26\%$ accuracy. This low accuracy makes it difficult to distinguish between the R_{thJC} values of different samples specially at low thermal resistance packages.

Table III shows an example of R_{thJC} estimation where 5 tests are performed with each TIM to obtain a 5x5 matrix of R_{thJC} values (i.e. finding the separation point between each Z_{th} curves obtained with one of the TIMs with each Z_{th} curve obtained with the other TIM) using the same approach as presented in [11]. The average value is then taken as the R_{thJC} of the PCB sample. Standard deviation is also calculated to ensure the reproducibility of R_{thJC} calculations. All R_{thJC} results presented in the rest of the article are calculated the same way and correspond to the average of a similar 5x5 matrix of R_{thJC} values.

TABLE II. THERMAL INTERFACE MATERIALS

TIM	k (W/m K)	Thickness
Sil-Pad®1500ST	1.8	0.2 mm
Deionized water	0.58	$\ll 0.2$ mm

TABLE III. R_{THJC} ESTIMATION

R_{thJC} (K/W)	Reference sample	Sil-Pad®1500ST				
		1	2	3	4	5
Deionized Water	1	0.6015	0.6504	0.6504	0.6504	0.6504
	2	0.6495	0.6495	0.7119	0.7119	0.6495
	3	0.6572	0.6572	0.7199	0.7199	0.7199
	4	0.5989	0.5989	0.6477	0.6477	0.6477
	5	0.6014	0.6503	0.6503	0.6503	0.6503
Average R_{thJC}	0.66					
STD	0.036					

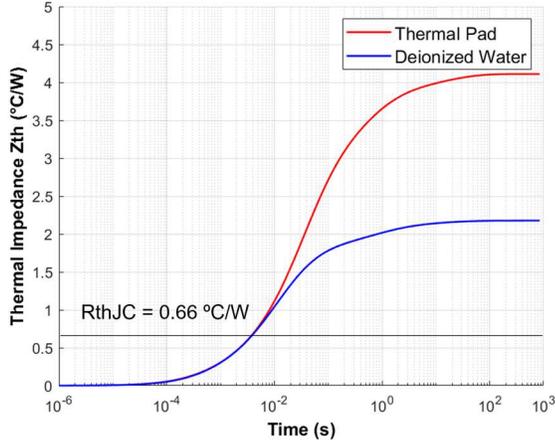


Fig. 10. Thermal impedance curves for the reference sample with different TIMs and the calculated R_{thJC} at the separation point.

VI. MODELLING

Thermal numerical simulations are performed using the finite element method (FEM) on ANSYS Mechanical. Only one quarter of the active part of the PCB samples was considered to limit computations and time (Fig. 11) without affecting simulation results. The thermal conductivities of the materials used for the simulations are specified in Table IV ([12], [13], [7]). Fig. 12 shows the impact of embedding graphite on temperature distribution for the same applied power and boundary conditions.

TABLE IV. MATERIAL PROPERTIES

Material	Thermal Conductivity (W/(m K))	Specific heat (J/(Kg.K))	Density (Kg/m ³)
Copper	385	385	8933
FR4	0.3	1150	1850
Graphite	1300 XY – 15 Z	850	1500
Adhesive	0.22	1926	1100
SiC	300	690	3210

The boundary conditions are set according to the experimental measurements. Because the TDIM method does not assume a constant temperature at the backside of the samples, we used a heat transfer coefficient (h) to represent the behavior of the TIM and the cold plate. Since this heat transfer coefficient is unknown, h is adjusted in the simulations so as to achieve the same R_{thJA} value (~ 4.27 K/W) with the simulation and the experiment of the reference sample without graphite (D22R) for 11 W power dissipation.

The value of h for which the simulations are found to correspond to the experimental results is 6000 W/(m² K) and is used for the calculations of R_{thJA} with the Sil-Pad TIM. Table V shows the boundary conditions applied in simulations in order to obtain R_{thJA} .

TABLE V. SIMULATIONS BONDARY CONDITIONS TO OBTAIN RTHJA

Location	Type	Value
SiC chip	Internal heat generation	Variable
PCB top	Heat transfer coefficient	10 W/(m ² K)
PCB bottom	Heat transfer coefficient	6000 W/(m ² K)

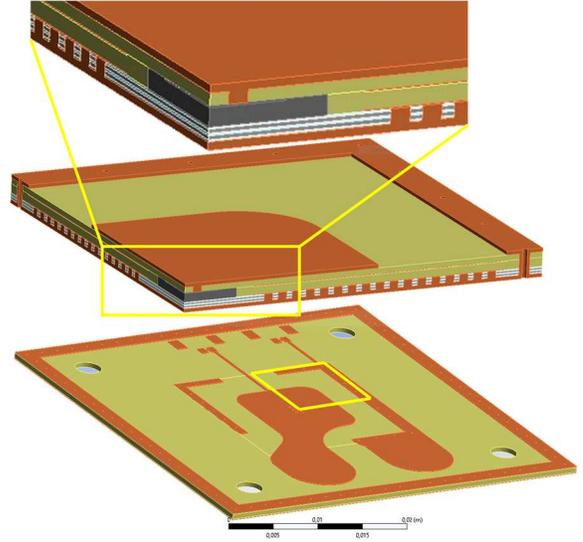


Fig. 11. CAD model of the fabricated PCB showing the quarter model considered for simulations.

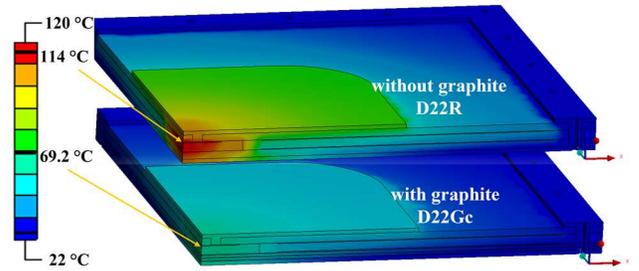


Fig. 12. Temperature contours of a PCB model showing the impact of embedding graphite on junction temperature. Power applied is 20 W and heat transfer coefficient at the bottom of the model is 5000 W/(m² K).

R_{thJC} is calculated in a way which mimics the TDIM method: two transient thermal simulations are performed for each sample, with two different values for h : 6000 W/(m² K) and 36000 W/(m² K), representing the Sil-Pad and water TIMs respectively. The processing method described in JEDEC51-14 (calculation of the derivative of the difference between both Z_{th} curves, threshold detection) is then applied. This allows us not to make any assumption on the temperature distribution on the backside of the samples, and yields a R_{thJC} value which is fully consistent with the measurement method.

VII. RESULTS AND DISCUSSION

Two parameters are compared here: R_{thJA} (steady-state value of the Z_{th} with Sil-Pad TIM) and R_{thJC} (obtained using TDIM method). Samples with graphite are compared to reference samples (without graphite) of the same size. Moreover, measurements are compared to FEM simulations. In addition, a commercial MOSFET sample packaged in a TO-247-3 case is used to provide a comparison point to a conventional packaging technology.

A. R_{thJA}

Table VI shows experimental and simulated (FEM) R_{thJA} values, as well as the difference with the reference samples. The experimental values are the average of 5 measurements (the sample was removed and replaced, with a fresh TIM each time), and the error value corresponds to the standard deviation of the 5 measurements.

TABLE VI. JUNCTION TO AMBIENT THERMAL RESISTANCE R_{thJA}

PCB Sample	$R_{thJA}(K/W)$			Reduction in R_{thJA} %	
	Experiment	FEM	Difference %	Experiment	FEM
D22R	4.11 ± 0.04	4.27	3.7 %	REF	REF
D22Ga	2.63 ± 0.04	2.09	26.1 %	- 36 %	- 51 %
D22Gb	2.54 ± 0.02	2.12	20 %	- 38.2 %	- 50.4 %
D22Gc	2.72 ± 0.02	2.2	23.8 %	- 33.8 %	- 48.5 %
D11R	4.41 ± 0.04	4.28	3.1 %	REF	REF
D11Ga	3.32 ± 0.07	2.48	33.8 %	- 24.7 %	- 42.1 %

Since h boundary condition was adjusted in simulations for the reference PCB sample, the difference with the measurements is only 3.7 % (not 0 % given the accuracy of the measurements). For PCB variants with graphite the difference can reach 20-35 %. This difference means that not all effects are properly modelled (the characteristics of the graphite may differ from their specified values, interfaces are not ideal in reality...).

Despite the difference between experimental and simulated values, the impact of embedding graphite is obvious. 34-38 % reduction in R_{thJA} is achieved (up to 51 % predicted by FEM simulations).

Increasing micro vias density (layout Ga or Gb) reduces R_{thJA} by about 2.5 % according to simulations, but this difference is too small to be validated experimentally. The effect of heat spreading due to graphite can be seen when comparing D22Ga with D11Ga (graphite sheet sizes of 20x20 mm², 10x10 mm², respectively) with an increase in R_{thJA} of about 18.7 % in simulations (2.09 K/W, 2.48 K/W, respectively) and around 26.2 % in measurements (2.63 K/W, 3.32 K/W, respectively). However, even the relatively modest area offered by the 10x10 mm² samples (a quarter of the area of the 20x20 mm² samples) already has a dramatic spreading effect compared with the reference sample, at 24.7% (experiment) and 42.1% (simulation) reduction in R_{thJA} . That means that even a 10x10 mm² graphite heat spreader can be sufficient for some applications, and that increasing the graphite area further may only yield moderate gains (20.8 % gain when increasing graphite size to 20x20 mm²).

B. R_{thJC}

Table VII presents the experimental and simulated R_{thJC} values for the various PCB variants. According to the simulations, the PCB variants with graphite achieve around 25 % reduction in R_{thJC} compared to the reference sample. Experiments are consistent and show a reduction of 10-30 %. For the 10x10 mm² samples, the reduction is more modest (19 % experimentally and 11 % in simulation for D11Ga with respect to the reference sample D11R). Because of the accuracy

limitations of the TDIM discussed above, it is not possible to draw a conclusion from the experimental data regarding the different vias layouts.

It is worth noting that the effect of the graphite heat spreader cannot be captured by the R_{thJC} value alone: the reduction in R_{thJC} between D22Ga and D22R is 0.2 K/W only (experimental values). However, when considering R_{thJA} (i.e the complete heat path, from junction to case to ambient), the reduction is much larger (from 4.11 K/W down to 2.63 K/W in Table VI, or a 1.47 K/W difference). This highlights that the spreading effect offered by the graphite also allows to use the cold plate and TIM layer much more efficiently.

TABLE VII. JUNCTION TO CASE THERMAL RESISTANCE R_{thJC}

PCB Sample	$R_{thJC}(K/W)$			Reduction in R_{thJC} %	
	Experiment	FEM	Difference %	Experiment	FEM
D22R	0.66 ± 0.04	0.6	10	REF	REF
D22Ga	0.46 ± 0.02	0.465	1.1	- 30.3 %	- 22.5 %
D22Gb	0.51 ± 0.02	0.45	13.3	- 22.7 %	- 25 %
D22Gc	0.59 ± 0.02	0.45	31.1	- 10.6 %	- 25 %
D11R	0.73 ± 0.03	0.6	21.7	REF	REF
D11Ga	0.59 ± 0.00	0.53	11.3	- 19.2 %	- 11.7 %

C. Comparison with a TO-247-3 package

The objective of this section is to provide a comparison point between the samples presented so far with a more common packaging technology. The same MOSFET chips, packaged by their manufacturer in a TO-247-3 package are characterized thermally using the same protocol as previously described. In this package, the SiC die is soldered directly on a thick (1-3 mm) copper lead frame. The amount of copper and the direct soldering of the die in TO-247-3 package improve its heat spreading function compared to a PCB package, at the expense of a bulkier package. Fig. 13 shows the difference between MOSFET TO-247-3 package and a classical PCB package. Table VIII shows R_{thJA} and R_{thJC} results for SiC MOSFETs in TO-247-3, M22R and M22Ga packages (note that results in tables VI and VII correspond to diode samples, not MOSFETs).

As for the diode PCB samples, the MOSFET M22Ga graphite sample offers a 36% reduction in R_{thJA} compared to the M22R reference sample, and a 29% reduction in R_{thJC} . When comparing with tables VI and VII. One can also observe that the R_{thJA} of M22R and M22Ga is about 5% lower than that of D22R and D22Ga. This is consistent with the difference in die size between the MOSFET and the diode.

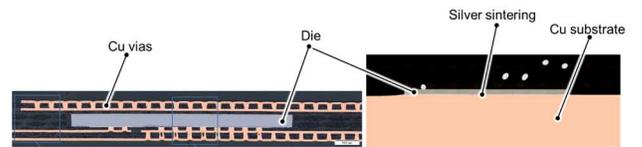


Fig. 13. Typical PCB stack with embedded die and 4 layers of via interconnections (left) in comparison with direct silver sintering die in a TO-247-3 package (right [14]).

TABLE VIII. COMPARISON BETWEEN TO-247-3 AND FABRICATED PCB PACKAGES

PCB Sample	<i>RthJA</i> (K/W)	<i>RthJC</i> (K/W)	Difference % in <i>RthJA</i> w.r.t. TO-247-3
	Measurements	Measurements	
M22R	3.88 ± 0.026	0.59 ± 0.05	+162 %
M22Ga	2.50 ± 0.014	0.42 ± 0.03	+ 69 %
TO-247-3	1.48 ± 0.014	0.45 ± 0.04	REF

Compared with the TO-247-3 package, the *RthJA* of M22Ga and M22R is 69 % and 162 % higher, respectively. This large difference is much smaller when considering *RthJC*, for which TO-247-3 and M22Ga show no significant difference (0.45 ± 0.04 K/W and 0.42 ± 0.03 K/W, respectively). This, together with the modest increase in *RthJC* when reducing the spreading area from 20x20 mm² to 10x10 mm² (D22Ga and D11Ga in table VII) seems to indicate that the graphite heat spreader is not efficient enough to fully utilize the 20x20 mm² area. For such large surface, the thick copper layers of the TO-247-3 package offers better heat spreading performance, at the expense of a much thicker package (5 mm for the TO-247-3, 0.8 mm for the PCB samples).

VIII. CONCLUSION

This paper presents a solution for heat spreading which is compatible with PCB manufacturing processes. It relies on a sandwiched structure of adhesive and graphite

Diode and MOSFET PCB packages with embedded graphite were successfully fabricated and compared to reference samples without graphite. An 86 % manufacturing yield for the embedded semiconductor devices has been measured, a reasonable value for a prototype run. Reflow tests show that a high density of micro-vias is necessary to provide mechanical clamping of the graphite layers, and prevent their exfoliation.

Thermal impedance measurements and simulations were performed to obtain *RthJA* and *RthJC* values of the samples. For *RthJA*, the JEDEC51-14 method was implemented experimentally and in simulation. The impact of embedding a graphite heat spreader in the PCB is obvious: up to 38 % reduction in *RthJA* and 30% reduction in *RthJC* are observed experimentally.

The *RthJA* of traditionally-packaged chips (TO-247-3) remains lower than that of PCB-embedded devices with a graphite heat spreader, indicating a more efficient spreading effect for a thick copper lead frame than for thin graphite layers. However, the graphite heat spreader constitutes an interesting trade-off, offering a clear improvement over standard PCBs without any increase in board thickness.

REFERENCES

- [1] C. Buttay, C. Martin, F. Morel, R. Caillaud and J. Le Lesle, "Application of the PCB-Embedding Technology in Power Electronics-State of the Art and Proposed Development," *3D-PEIM 2018 - 2nd International Symposium on 3D Power Electronics Integration and Manufacturing*, 2018.
- [2] R. Mrad, J. Morand, R. Perrin and S. Mollov, "A PCB based package and 3D assembly for high power density converters," *IEEE International Workshop on Integrated Power Packaging*, p. 73–77, 2019.
- [3] C. Hérold, N. Emery, J.-F. Mareché and P. Lagrange, "Synthesis and superconducting properties of bulk CaC₆ GIC," *Science and Technology of Advanced Materials*, 2008.
- [4] B. Ozpineci, E. Gurpinar, J. P. Spires and W. Fan, "Analysis and Evaluation of Thermally Annealed Pyrolytic Graphite Heat Spreader for Power Modules," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020.
- [5] "CPM2-1200-0080B, Silicon Carbide Power MOSFET, C2M TM MOSFET Technology," CREE, 2016.
- [6] "IPC-TM-650, Test Method Manual, Thermal Stress, Convection Reflow Assembly," IPC, 2020.
- [7] J. Lutz, *Semiconductors Power Devices, Physics, Characteristics, Reliability*, Springer, 2011.
- [8] J. W. Sofia, "Junction Temperature Accuracy Analysis," *ANALYSIS TECH*, 2011.
- [9] "JEDEC51-14, Transient Dual Interface Test Method for the Measurement of the Thermal Resistance Junction-to-Case of Semiconductor Devices with Heat Flow Through a Single Path," JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, 2010.
- [10] D. Schweitzer, H. Pape, L. Chen, R. Kuts and M. W. Walder, "Transient Dual Interface Measurement – A New JEDEC Standard for the Measurement of the Junction-to-Case Thermal Resistance," *27th IEEE SEMI-THERM Symposium*, 2011.
- [11] J. Knoll, C. DiMarino and C. Buttay, "A Guide for Accurate and Repeatable Measurement of the *RthJC* of SiC Packages," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022.
- [12] P. Industry, "PGS Graphite Sheets," Panasonic, 2021. [Online]. Available: www.industrial.panasonic.com.
- [13] DuPont, "Pyralux LF," DuPont, [Online]. Available: <https://www.dupont.com/electronics-industrial/pyralux-lf.html>.
- [14] E. Barbarini, "Wolfspeed C2M0025120D, 1200V SiC MOSFET, POWER report," SYSTEMplus Consulting, 2018.