# Study of Supercapacitor Ageing for Next Generation Avionics

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***Abstract*—This work studies the lifetime of super-capacitors in micro power cut ride-through applications within avionics power supplies. Analysis shows that the ride-through function's footprint in the application can be significantly reduced in relation to the current solution thanks to supercapacitors. Supercapacitor ageing is a well known phenomenon that can be described by Eyring's Law based equations. However, they do not encompass voltage cycling-induced accelerated ageing. Moreover, they do not properly predict lifetime when supercapacitor voltage is much lower than rated value. These two last phenomena occur during avionics operation. Therefore, a test-bench and protocol were developed allowing to evaluate the technology's suitability for the application. Results show that the components are compatible with the mission duration of 30 years. Additionally, tests and an impedance spectrometry characterisation validate their performance under fast, pulsed current operation such as the one under analysis.**

***Index Terms*—Super Capacitor, EDLC, lifetime model, ageing, Eyrings Law, avionics**

## I. Introduction

In order to ride-through input grid transient power cuts, avionics power supplies contain an energy reserve function. In present-day designs, this function must support nominal flight computer consumption (up to $\sim 150\,\mathrm{W}$ in next generation avionics) during the duration of micro power interruptions (up to $200\,\mathrm{ms}$), while fitting in a constrained footprint of less than $140\,\mathrm{cm}^2$ with a height lower than $2.5\,\mathrm{cm}$. On the other hand, operating temperature range ($-40\,^\circ\mathrm{C}$ to $85\,^\circ\mathrm{C}$ ) and mission service time (30 years) makes the implementation of this function challenging. Aluminium electrolytic and super-capacitors are the only potentially compliant alternatives. The Airbus standard here applicable, $ABD0100g2-1.8C$ [1], defines (requirement #009, Table 5.3) their required tolerance to grid transients, see Fig. 1. In reality, $115\,\mathrm{V}$ RMS AC grid supplied equipment encounter up to $30\,\mathrm{ms}$ interruptions while $28\,\mathrm{V}$ DC grid ones actually do support the maximum $200\,\mathrm{ms}$ duration.

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| Steady-state characteristics | | | Normal | Abnormal | Emergency |
|---|---|---|---|---|---|
| Voltage (VDC) (see note below) | Min | SA, A330, A340 | 27 - ΔVdc | 25 - ΔVdc | 18.5 - ΔVdc |
| | | A380 | 27 - ΔVdc | 25 - ΔVdc | 20 - ΔVdc |
| | | A350 | 27 - ΔVdc | 24.5 - ΔVdc | 21.5 - ΔVdc |
| | Max | SA, A330, A340, A380 | 30.3 | 32.5 | 32.5 |
| | | A350 | 31.7 | 32.5 | 32.5 |
| Voltage ripple | | | Figure 5-7 | Figure 5-7 | Figure 5-7 |
| | | | | | |
| **Transient characteristics** | | | **Normal** | **Abnormal** | **Emergency** |
| Voltage | | | | | |
| Voltage transients | SA, A330, A340 | | Figure 5-8-A | Figure 5-8-A | Figure 5-8-A |
| | A380 | | Figure 5-8-B | Figure 5-8-B | Figure 5-8-B |
| | A350 | | Figure 5-8-C | Figure 5-8-C | Figure 5-8-C |
| Voltage variation due to APU starting | SA, A330, A340, A380 | | Figure 5-9-A and Figure 5-9-B | N/A | N/A |
| | A350 | | Figure 5-9-C | N/A | N/A |
| Voltage spikes | | | Figure 5-10 | Figure 5-10 | Figure 5-10 |
| **Power interruption** : maximum duration | | | 200 ms (SA, A330, A340) or 3 ms (A380, A350) | 5 s | 200 ms (SA, A330, A340) or 3 ms (A380, A350) |

Fig. 1: Required susceptibility of 28V DC equipment [1].

The current function implementation counts on components resembling the $MAL213659681E3$, $100\,\mathrm{V}$, $680\,\mu\mathrm{F}$ electrolytic capacitors from Vishay. Each one provides $7\,\mathrm{W}$ during $200\,\mathrm{ms}$, even after ageing and considering operating condition's impact on capacitance and tolerance. Mounting is horizontal due to component maximum height ($37.5\,\mathrm{mm}$ surpassing the maximum allowable value of $25\,\mathrm{cm}$. Thus, with their $18\,\mathrm{mm}$ diameter, they occupy roughly $7.20\,\mathrm{cm}^2$. This means that to achieve function size reduction, the chosen component should be able to provide both: more energy per unit surface, and more power per unit surface than the current solution. The selected component must then have an energy density higher than $166\,\frac{\mathrm{mJ}}{\mathrm{cm}^2}$ and a power density higher than $833\,\frac{\mathrm{mW}}{\mathrm{cm}^2}$.

Though avionic systems do tolerate extreme temperatures ($-40\,^\circ\mathrm{C}$ *to* $85\,^\circ\mathrm{C}$), design lifetime considers actual mission profile temperatures. Fig. 2 shows a temperature probability density function resembling that of avionics equipment. The distribution's low deviation value (about $7.5\,^\circ\mathrm{C}$), means one can consider the $35\,^\circ\mathrm{C}$ average temperature for lifetime calculations.

Fig. 3 shows a Ragone Plot of commercial energy storage devices that either maintain or improve function integration. Depicted performance is worst case value at the end of the mission duration (with increased equivalent series resistance, ESR, and reduced capacitance). The characteristics of the current component currently implemented on avionics equipment is marked with a red dot. Electrolytic capacitor devices are represented with filled circles. Circle color represents component nominal voltage as indicated in the color bar to the right of the diagram (units are in volts). A component improves energy reserve function integration if its energy density is higher. Dividing its energy density by the one

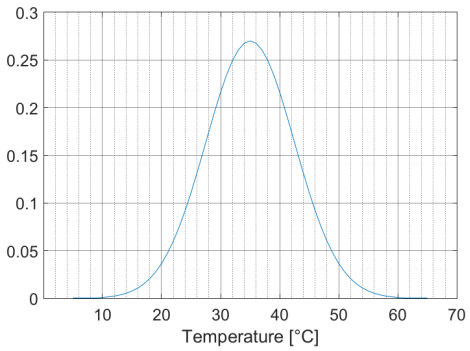



Fig. 2: Approximation of avionic equipment temperature time share distribution.

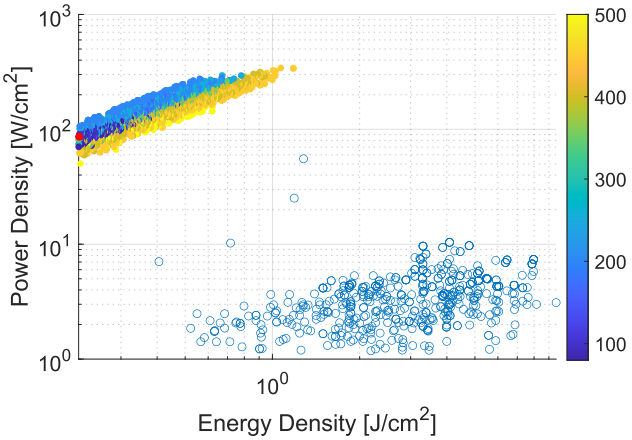



Fig. 3: Ragone plot for COTS super-capacitors and aluminum electrolytic capacitors.

of the current implementation (for electrolytic capacitors) allows to estimate integration improvement. Hollow blue circles represent super capacitors in Fig. 3. Since super-capacitors are power density limited, relative improvement is estimated dividing a component's power density by the minimum ordinate of the chart ($833\,\frac{\mathrm{mW}}{\mathrm{cm}^2}$).

Considering Fig. 3, one can conclude that footprint could be reduced by more than 75% using high voltage (HV) category components (the ones rated $450\,\mathrm{V}$). This is due to the technology's energy density -"$\propto \frac{C \cdot V_{app}^2}{2 \cdot A}$" - increasing with voltage, which is linked to the usage of higher end dielectric films. However, function implementation with a resulting voltage of $\sim$ $360\,\mathrm{V}$ in avionic safety critical Design Assurance Level (DAL) "A" (equipment failure can be hazardous or catastrophic) environments would impose additional safety-related constraints that would make the solution less attractive. In Fig. 3, super-capacitors performance shows they could allow a similar footprint reduction, without the need for HV circuitry. Their main limitation however is power density - "$\propto \frac{V_{app}^2}{4 \cdot ESR \cdot A}$"-, which is linked to low electrolyte conductivity, and component lifetime. Note that, here, $V_{app}$ is component nominal voltage in the application.

### A. *Super-capacitor Lifetime*

Super-capacitor lifetime can be modelled using Eyring's law, see Eq. 1, where the $200\,\mathrm{mV}$ and $10\,^\circ\mathrm{C}$ constant are typical [2]. In Eq. 1, "$L$" is expected application lifetime, "$L_O$" is lifetime for rated maximum temperature, $T_r$ and voltage $V_r$. Furthermore, $V_{app.}$ and $T_{app}$ are respectively application nominal voltage and temperature.

$$L = L_O \; 2^{\frac{V_r - V_{app.}}{K_v}} \; 2^{\frac{T_r - T_{app.}}{K_t}} \tag{1}$$

Typically the values of Eq. 1's constant parameters are $K_v = 200\,\mathrm{mV}$ and $K_t = 10\,^\circ\mathrm{C}$ [2] [3]. However, studies have shown that Eq. 1 has limitations which are significant to the application at hand.

Firstly, lifetime prediction as a function of $V_{app}$ is not precise when $V_{app}$ is far below $V_r$. Below a certain threshold, lifetime no longer increases as expected when decreasing $V_{app}$. This was noted in [4], where an ad-hoc lifetime curve differing from Eq. 1 was proposed to fit experimental lifetime evaluation at $0\,\mathrm{V}$. It is reproduced in Fig. 4. Now, for a component that suits the application like the MAL2235x1003: $L_O = 2\,\mathrm{kh}$, $V_r = 2.6\,\mathrm{V}$ and $T_r = 85\,^\circ\mathrm{C}$. Then, to attain mission duration at $40\,^\circ\mathrm{C}$: $V_{app} \leq 2.35\,\mathrm{V}$, which is close to the region in which Eq. 1 is no longer valid in [4]. For some manufacturers Eq. 1 is valid far below $V_r$ [5], but for others this is not the case [3]. Do note that in Fig. 4 lifetime dependency on temperature is still considered independently of floating voltage.

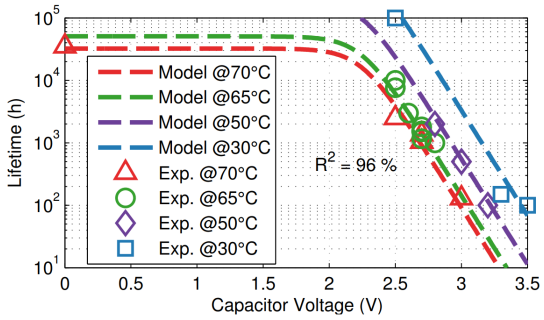



Fig. 4: Proposed curve for a supercapacitor's lifetime with voltage and temperature when considering lifetime increase limit at $0\,\mathrm{V}$ from [4]

Secondly, [6] shows that periodical power and voltage cycling can also reduce lifetime. Super-capacitor ageing is mainly driven by solid electrolyte interface (SEI) formation. This is caused by chemical reactions between gas present in the electrolyte and the electrodes. It effectively reduces the components activated carbon electrode active area and with that capacitance. The phenomenon can also increase ESR due to cracking related to internal pressure increase. The hypothesis is that power cycling induced electrolyte ion movement periodically removes the passivized SEI from electrode surface, renewing an ageing cycle and accumulating it in the electrolyte. The phenomenon is depicted in

Fig. 5 a) [6], and can be important when electrode pore diameter is comparable to solvated ion diameter. Fig. 5. In [6], this effect was shown to be capable of shortening lifetime by as much as $50\%$. For the super-capacitors of interest, which could require further component voltage derating for lifetime, curtailing power density even more and making them operate within the voltage range in which the standard ageing model from Eq. 1 is no longer valid. Voltage cycling can however also increase lifetime as in [7], since capacitance can recover after resetting component voltage.

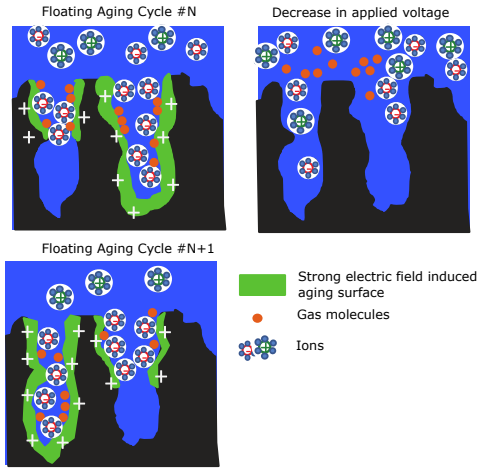



Fig. 5: Acceleration of ageing due to power cycling repeatedly separating the solid electrolyte interface (SEI) passivated layer and restarting an ageing cycle from [6].

Avionics reliability engineering specialists translate a 30 year mission duration into a component lifetime requirement of $110\,\mathrm{kh}$. To comply, for the $MAL223591003E3$, a $20\,\mathrm{F}$, rated $2\,\mathrm{kh}$ at $2.6\,\mathrm{V}$, $85\,^{\circ}\mathrm{C}$ supercapacitor, using Eq. 1, maximum steady state component voltage should be $V_c \leq 2.24\,\mathrm{V}$. If one considers the component operates with only $5\%$ discharge during power interrupts, the components power density at end of life would be $\sim 6\,\frac{\mathrm{W}^2}{\mathrm{cm}}$ and its energy density $\sim 8\,\frac{\mathrm{J}^2}{\mathrm{cm}}$. This means that if one only considers the surface of the energy storage components, function footprint could reduce by $\sim 70\%$.
Additionally, an energy reserve within avionics can be solicited up to 2 times per flight by grid micro power-cut events in the most demanding of A/C families. These can occur, for example, when aircraft power switches from the stand-by power system to the auxiliary power unit (APU) generator upon engine start-up. These A/C typically have between 3 and 7 flights per day on average, so power cycling events through component lifetime can be high, between 54000 and 128000. Thus, given the above described phenomena, it is apparent that component lifetime compatibility with the application is not guaranteed and that experimental testing is necessary.

## II. Ageing Platform

Due to the aforementioned limitations of Eq. 1, a test-bench was developed to evaluate the chosen supercapacitors' compliance with application mission duration. The goal of the tests was to perform accelerated ageing on the components to:

1) Precisely determine the coefficient in Eyring's that relates lifetime to operating temperature. In Eq. 1, the typical value of $10\,^{\circ}\mathrm{C}$ is used. Eq. 1 validity in relation to this parameter is generally accepted, independently of the level of voltage derating.
2) Determine whether, at typical steady state application voltages, lifetime deviation from that predicted by Eq. 1 is significant.
3) Determine whether the power cycling the components as in the application significantly reduces their lifetime.

Note that the goal is not to validate the lifetime model from Fig. 4 at low voltage, but rather to validate compliance to app. lifetime when operating with high voltage derating. Thus, in the test-bench, ageing acceleration is only supported by increased temperatures. Two separate thermal chambers were used, one at $80\,^{\circ}\mathrm{C}$ and another one at $70\,^{\circ}\mathrm{C}$. For components aged at $80\,^{\circ}\mathrm{C}$, the acceleration factor with regard to mean $35\,^{\circ}\mathrm{C}$ is 22.6, meaning total test duration to achieve the $110\,\mathrm{kh}$ needed lifetime would require $\sim 6.7$ months of ageing.

Fig. 6 presents a high level schematic of the test bench. It is based on a Compact RIO rapid prototyping control module with analog/digital I/O extensions. Its digital outputs command optical floating drivers to minimize HF EMI coupling. The drivers, in turn, control 8 power stage channels by pairs. Each channels' topology is a synchronous buck converter. Each contains input bypass MLCCs, a MOSFET half-bridge, an output choke, a Hall Effect current sensor, an output relay and output bypass MLCCs. Each output is connected to one supercapacitor all of which are, in turn, placed in separate boards within one of two thermal chambers. All power stages are fed by a common input $600\,\mathrm{mF}$ bus. The chosen supercapacitors where $MAL223591003E3$ $20\,\mathrm{F}, 3\,\mathrm{V}$ ruggedized supercapacitors from Vishay.

Fig. 7 on the other hand shows the resulting test-bench, where the controller is clearly visible on the left, next to the input capacitor bus, which has the power stage channels to its right. Power stage output cable connections going to one of the thermal chambers can also be seen at the right of the image.

Components were aged at a $1.9\,\mathrm{V}$ floating voltage in steady state. Additional $\sim 0.3\,\mathrm{V}$ derating was applied below the above calculated minimum $2.24\,\mathrm{V}$ required per Eq. 1 to compensate for potential acceleration in ageing due to power cycling. The power-cycle event frequency was set to $5\,\mathrm{min}$ to condensate the same number of cycles throughout ageing at $80\,^{\circ}\mathrm{C}$ as would occur throughout the lifetime of the component in an A/C with 3 flights per day.

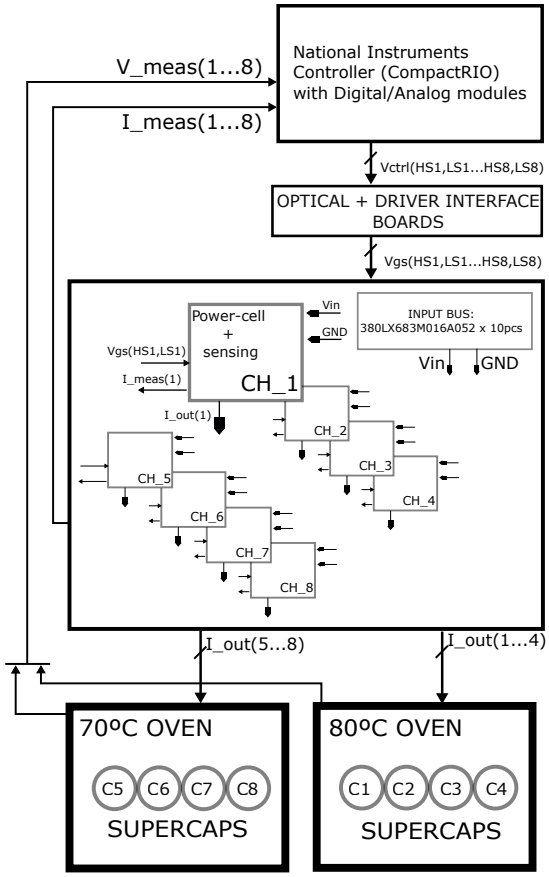



Fig. 6: High level diagram of the test bench used to age the components.

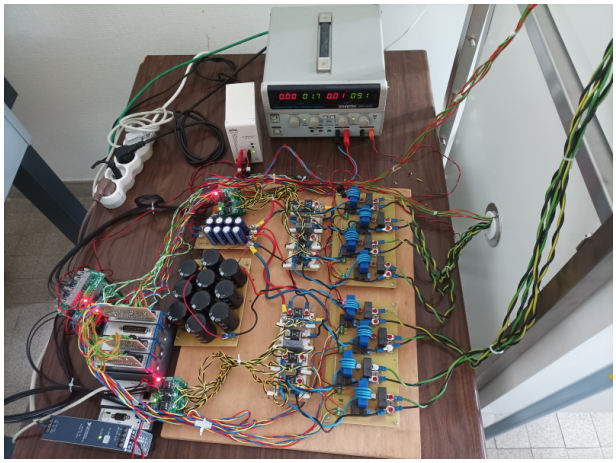


Fig. 7: Experimental setup for the component ageing test-bench.

In the application, component current charge and discharge pulses slightly deviate from a constant pulse to compensate for capacitor discharge. Since simulation showed discharge is below $10\%$ of initial voltage for components of interest, cycling at constant current was considered representative. The amplitude of current used was $8\,\mathrm{A}$. This is half the maximum current level the components could encounter at end-of-life, when asked to provide full power with a degraded ESR. Though components must be able to operate under this situation, it is not representative of normal operation and so it was considered reasonable to apply a $50\%$ margin. Fig. 8 shows voltage and current waveforms representative of the power cycle on any of the channels. Power cut duration was set to the ABD maximum of $200\,\mathrm{ms}$. The reason why there is a $1\,\mathrm{s}$ delay between the discharge and charge pulses is because it was desirable to also be able to estimate ESR with the standard procedure from [3].

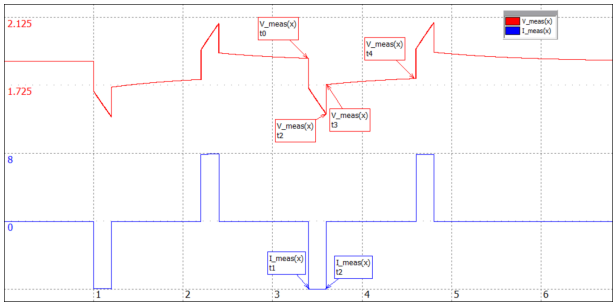



Fig. 8: Spice model power cycle wave-forms for a single component. The actual applied time between power cuts is not properly represented. Components modelling is per [9].

Fig. 9 describes the state machine of the control system managing each power channel. The state machine determines whether the power state is in standby ("control_standby()"), whether it operates in average current mode control ("control_current()") or in voltage mode control ("control_voltage()"). It also determines the applicable control reference in each case and defines transitions between states ("TIMEOUT" being the timeout event of the timer that is armed upon state entry). To minimize the impact of supercapacitor charge on the power bus, initiation of each channel's state machine was delayed by $3\,\mathrm{s}$ with regard to the previous one (i.e.: channel $\#2$ was delayed by $3\,\mathrm{s}$ with regard to $\#1$, $\#3$ was delayed by $3\,\mathrm{s}$ with regard to $\#2$ and so on). As can be deduced from Fig. 8 ESR is estimated by measuring component current and voltage right before the end of discharge, $t_2$, and measuring voltage right after ($10\,\mathrm{ms}$ delay as in [11]), $t_3$. It is then estimated after each cycle as in Eq. 2. In Fig. 9, measures at $t_2$ correspond to those triggered upon "DISCHARGE" state exit, while those at $t_3$ are triggered after entry into the "WAIT" state. An additional system-level state machine was tasked with recovering the measured values from the one in Fig. 9. It then calculated ESR as in Eq. 2 and communicated the estimations with a timestamp to a separate desktop PC for storage in an autonomous way.

$$\overline{ESR} = \frac{V(t_3) - V(t_2)}{I(t_2)} \tag{2}$$

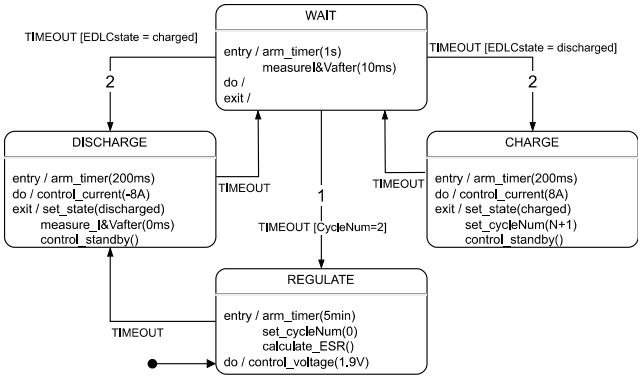



Fig. 9: State-machine of the control system managing the test-bench

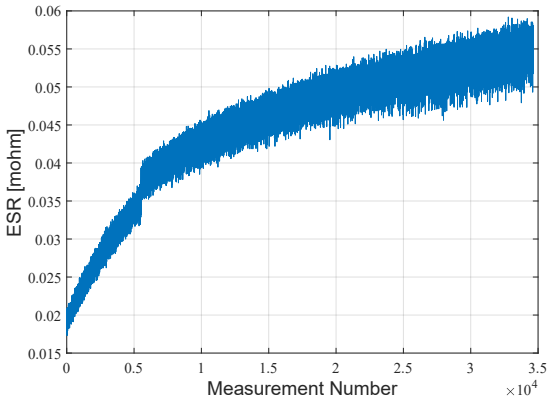



Fig. 11: Estimated Values of ESR for one component during the test.

## III. Experimental Results and Analysis

Since component data-sheets report ESR for power cycles of longer duration (e.g.: lasting $1\,\mathrm{s}$ in [11]) and at rated voltage, it was important to validate that its value would not significantly degrade when using the component under the intended conditions. Fig. 10 shows ESR dependency on applied voltage resulting in a $+50\%$ increase from the datasheet value in low frequency. However, when using Eq. 2 to estimate ESR in the test-bench, the value was close to the datasheet one ($\pm 10\%$) for all components. In Fig. 10, the color bar shows evolution with frequency, its values being $log10(f/1[Hz])$, with "f" being frequency in Hertz.

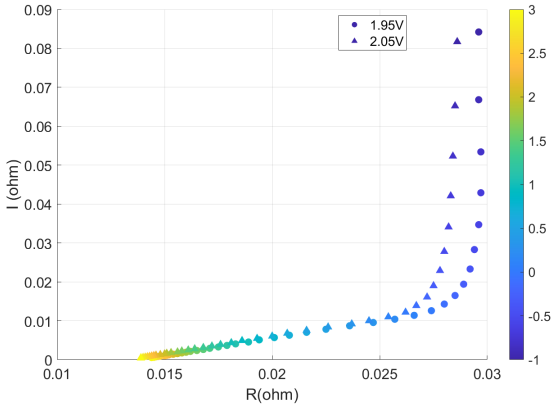



Fig. 10: Electrochemical Impedance Spectroscopy of a healthy component.

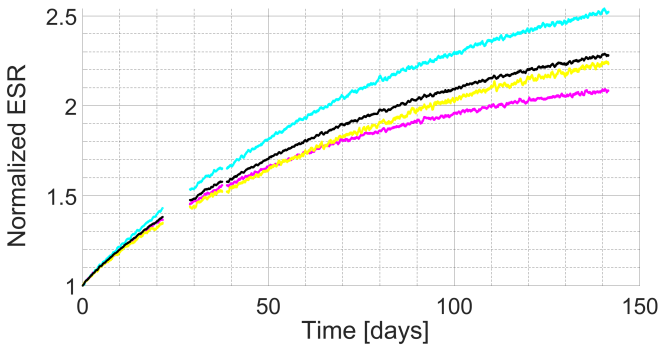
Fig. 11 shows raw ESR estimations for one of the components aged at $85\,^{\circ}\mathrm{C}$. While $\pm 3\,\mathrm{m}\Omega$ random variation could indicate a low precision, the large amount of measurements performed (one every $5\,\mathrm{min}$) at a very high rate in relation to the speed of ageing allowed to perform averaging to eliminate the influence of noise and bring out an accurate average measurement for analysis.

Fig. 12 on the other hand, shows processed experimental results from the ageing tests (each value shown is the average of all those acquired in an $8\,\mathrm{h}$ window). X axis represents days of testing deduced from the time stamp information associated to each measurement. Data is missing for a 7 day period after the first 23 days of operation because the desktop PC shut down during a summer break power interruption and so was re-started after one week. In Fig. 12, each color corresponds to an individual component. Significant dispersion exists between individual components. However, it was verified that average temperature, voltage and current applied was the same for all of them. Thus, black traces are added in Fig. 12 to represent the average behavior of all components aged at a given temperature.

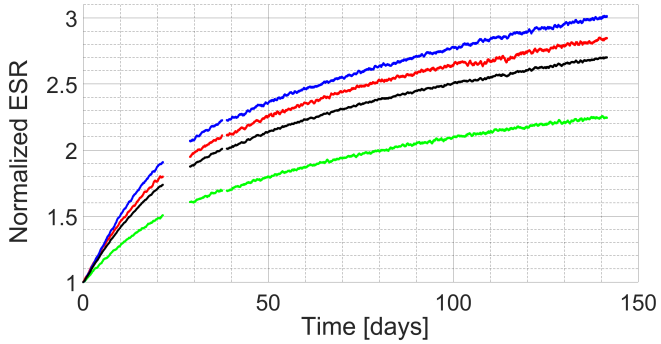
Both average ESR curves from Fig. 12 double datasheet ESR during ageing tests at 40 and 140 days respectively. This is typically considered end of life (e.o.l) for electrolytic aluminium capacitors and even for many supercapacitors (e.g.: [11], [12]). Therefore, the test was stopped after $142$ days of testing when this was observed upon test-bench supervision. However, datasheet information later showed that e.o.l is reached after a 4x increase in ESR for these specific ruggedized EDLC series to which the MAL2235x1003 belongs [13].

Towards the end of the test, ageing rate is clearly constant for the average curve of Fig. 12a at $\sim 0.5\frac{\%}{day}$. Thus, extrapolating, test results indicate that $402$ days of testing are necessary to reach e.o.l at $80\,^{\circ}\mathrm{C}$. Eq. 1 would have predicted that 976 days were needed under the tests conditions. Extrapolating 12b is challenging since the components do not seem to be ageing at a constant rate and thus only a rough notion of the value of $K_t$ can be obtained. The ageing rate for the last 20 days of the test of 12b was fitted with Matlab's linear model fitting tool to be $0.42\frac{\%}{day}$, with $R^2 = 0.8896$. On the other hand, for 12a, in the 20 day window centered around the time when average ESR was $\sim 224\%$ ($62^{nd}$ day), the ageing rate was estimated as $0.83\frac{\%}{day}$ with $R^2 = 0.995$. This seems to indicate that for the $MAL223591003E3$, $K_t$ will also be close to $10\,^{\circ}\mathrm{C}$.

With these results target $110\,\mathrm{kh}$ at $35\,^{\circ}\mathrm{C}$ translates into




(a) ESR of components submitted to 70 °C




(b) ESR of components submitted to 80 °C

Fig. 12: Ageing test bench results for ESR.

4.86 kh at 80 °C, i.e.: 202 days. Considering the extrapolation of Fig. 12a, at the end of mission duration, component ESR would be 300% of its initial value. This is the end of life value actually used to depict Fig. 3.

## IV. Conclusion

This article provided experimental evidence of the compatibility of supercapacitor lifetime with an avionics application. As a result, the energy storage function within a flight computer could reduce footprint by as much as 70%, which is critical for next generation avionics targeting A/C programs were 200 ms power interruptions can occur. Future research should use the developed test bench to launch an additional ageing campaign in order to precisely calculate coefficient $K_t$ from Eq. 1. Finally, the difference between experimental component lifetime and the value that would be predicted by Eq. 1 also verifies the need and the importance of performing ageing tests on components to qualify them for the application.

## References

[1] Electrical Characteristics of AC and DC Equipment, ABD0100 g2-1.8:C, Airbus SAS, 2019.

[2] Illinois Capacitors Inc, "Life expectancy of Supercapacitors", Technical Note, Illinois Capacitors Inc (2019).

[3] Eaton, "Application Guidelines", Technical Note PS-5006 (visited 20/01/2021)

[4] T. Kovaltchouk, "Contributions à la co-optimisation contrôle-dimensionnement sur cycle de vie sous contrainte réseau des houlogénérateurs directs", PhD Thesis, Université de Lyon 15/10/2015.

[5] Maxwell, "Boostcap Ultracapacitor Product Guide ", Doc. No. 1014627.1, Maxwell Tech. (2009).

[6] R. German, "Étude du vieillissement calendaire des supercondensateurs et impact des ondulations decourant haute fréquence ", PhD Thesis, Université de Lyon 10/12/2013.

[7] R. Chaari, "Capacitance recovery analysis and modelling of supercapacitors during cycling ageing tests", Energy Conversion and Management, Volume 82, June 2014.

[8] R. German, "Impact of Voltage Resets on Supercapacitors Aging," in IEEE Transactions on Industrial Electronics, vol. 63, no. 12, Dec. 2016.

[9] R. German, "Improved Supercapacitor Floating Ageing Interpretation Through Multipore Impedance Model Parameters Evolution," in IEEE Transactions on Power Electronics, vol. 29, no. 7, July 2014.

[10] P. Kreczanik, "Study of Supercapacitor Aging and Lifetime Estimation According to Voltage, Temperature, and RMS Current," in IEEE Transactions on Industrial Electronics, vol. 61, no. 9, Sept. 2014.

[11] Maxwell, "3.0V 5F ULTRACAPACITOR CELL, Advanced Small Cell with XP Technology, BCAP0005 P300 X11", 3002553-EN.3.

[12] Eaton, "HV Supercapacitors Cillindrical Cells, Technical Data ", Doc No 4376, May 2016.

[13] Vishay, "Ruggedized Electrical Double Layer Energy Storage CapacitorsUp to 3 V Operating Voltage", Doc No 28455, July 17th 2019.