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Published in IET Power Electronics
Received on 5th June 2013
Revised on 12th January 2014
Accepted on 30th January 2014
doi: 10.1049/iet-pel.2013.0414

ISSN 1755-4535

Equivalent matrix structure modelling and control of a three-phase flying capacitor multilevel inverter

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Abstract: In this study, an equivalent matrix structure of three-phase flying capacitor multilevel inverters (FCMIs) is developed. This structure is obtained by using a switching function for each voltage level. For one switching function, there is more than one combination of gate signal to produce each output voltages. Hence ($3n$) switching functions are defined for all switch combinations of the output voltage and their corresponding switch states. Therefore the modulation strategy of a three-phase FCMI is obtained in two steps. Firstly, the direct space-vector modulation of the matrix converter is used to compute the switching functions. The gates signals of the three-phase FCMI can be calculated by inversing the modelling part. In this work, the direct space-vector multilevel modulation based on the use of $2n$ different three level functions called modulation functions is presented. Using this approach, the modulation strategy of a three-phase FCMI is designed without using a Park transform. To validate the effectiveness of the equivalent matrix structure modelling and control, simulation results are given for nine-level FCMI. Moreover, experimental results are given for a three-level neutral point clamped (NPC) converter prototype laboratory.

1 Introduction

Multilevel converters are more and more used in industry and research for high-power applications [1–4]. There are several advantages of multilevel inverters such as; improved waveform quality, no transformer needed, better output waveforms, which reduce the size of output filters and high efficiency (low switching frequency). The output voltage waveform of a multilevel inverter is composed of intermediary voltage levels, which are obtained from DC capacitor–voltage sources. DC capacitors create a high dc bus and enable supplying higher power [1, 2]. The various dc capacitor connections of the dc bus allow the use of many low power sources. The most popular multilevel inverter topologies are diode clamped inverter (DCI), flying capacitors multilevel inverters (FCMIs), cascaded multi cell with separate DC sources and module multilevel converter [1, 3–7]. Among the various multilevel converter topologies that have been proposed, the flying capacitor topology is emerging as a particular attractive solution because of the natural [3] or active (using a modified pulse-width modulation, PWM [7]) balancing of the dc bus [8, 9]. This is not the case of the DCI and NPC which need the balancing of dc voltages (across capacitors). To implement the balancing, the control strategie must take into account the charging and discharging phenomena of the capacitors [10–12].

Classical algorithms developed for two-level converters have been extended to multilevel inverters such as hysteresis current control, triangulo sinusoidal, harmonic elimination and space-vector modulation (SVM) [10–17].

In this paper, we develop an equivalent matrix structure of the three-phase $(n+1)$-level FCMI. Firstly, a switching function is defined to each voltage level. There is more than one combination to produce each output voltages. Therefore ($3n$) switching functions are defined for all switch combinations of the output voltage and their corresponding switch states. Then the relation between the switching functions and their corresponding switch states are developed. Hence any PWM control of the equivalent matrix structure can be used. In this case, the direct modulation system without using a Park transform (in d, q frame) can be used. Finally an inversion modelling is used to generate the gate signals of the FCMI.

Section 1 presents the equivalent matrix structure of the three-phase $(n+1)$-level FCMI. The design of the control system is presented in Section 3. Simulation results are given in Section 4 to show the very good performances, which have been obtained with the modelling of the three-phase nine-level FCMI. The developed line-to-line SVM for FCMI $(n+1)$-level-based on equivalent matrix converter is the same as for NPC $(n+1)$-level converter when we controlling the matrix converter by switching function. The difference is made in inversion of modelling parts, that is, in the relation between switching function and gate signal of the used converter. For this reason, we have inserted in Section 5 the experimental results for the three-phase NPC three-level converter prototype laboratory

using the developed line-to-line SVM to highlight the feasibility and performance of this new modulation, and conclusion is done in Section 6.

2 Equivalent matrix structure of the three-phase ($n+1$)-level FCMI

In this section, the equivalent matrix representation of the three-phase ($n+1$)-level FCMI is obtained using n switching functions of each phase-leg and corresponding relations of these switching functions with the gate signals are determined. Then, the multilevel operating by using two phase-to-phase voltages is expressed by the switching functions and the conversion modelling is obtained by using $2\times n$ elementary modulated voltages (or $2\times n$ modulated functions with the three states -1, 0 and 1). Finally the average modelling is presented which are used for the control system design.

2.1 Structure and operating principle

The FCMI requires a larger number of capacitors to clamp the device (switch) voltage to one capacitor–voltage level. Provided all capacitors have equal capacitance values, an ($n+1$)-level inverter will require a total $n(n-1)/2$ clamping capacitors per phase leg in addition to n main dc bus capacitors. The size of the voltage increment between two consecutive legs of the clamping capacitors defines the number of voltage steps in the output waveform. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor, then for an ($n+1$)-level inverter, if the voltage of the main dc-link capacitor is us, the voltage across a single capacitor is us/n. Each next clamping capacitor will have a us/n voltage increment from its immediate inner one. The voltage levels and the arrangements of the flying capacitor in the FCMI structure implies the same voltage stress across each main device: us/n for an ($n+1$)-level inverter [3].

The topology of the ($n+1$)-level FCMI consists of three commutation circuits (Fig. 1). The required switches are made of $2n$ transistors (T_{1c}, …, T_{2nc}) with anti-parallel diodes. The two switches $T_{(n+i)c}$ and $T_{n-(i-1)c}$ with $i=1, \ldots, n$ of a phase leg c ($c=1$, 2 or 3) (Fig. 1) are driven with complementary states

$$T_{(n+i)c} + T_{n-(i-1)c} = 1 \quad \text{i.e.} \quad T_{(n+i)c} = \bar{T}_{n-(i-1)c} \tag{1}$$

2.2 Fundamental principles of FCMI

In comparison with DCI, more flexibilities exist in a FCMI to generate output voltages. Using Fig. 2, the output voltage of a phase leg c ($c=1$, 2 or 3) with respect to the point 0 (u_{c0}) can be synthesised by various switch combinations (see Table 1). For each voltage level, a switching function f_{rc} is defined where r is the voltage level that is, r is used to define the rows in the ideal matrix ($r \in \{0, \ldots, n\}$) and c is the phase leg that is, c is used to define the columns in the ideal matrix ($c \in \{1, 2, 3\}$):

- For the voltage level $u_{c0}=0$ ($f_{0c}=1$), all upper switches $T_{1c}-T_{nc}$ are turned off, that is, all lower switches $T_{(n+1)c}-T_{2nc}$ are turned on. This is the unique combination to implement this voltage level and so the number of possibilities is defined as $n_p=1$.
- For the voltage level $u_{c0}=u_s/n$ ($f_{1c}=1$), n combinations of one switch in the on state exist and the remaining $(n-1)$ switches are off. So n possibilities exist and $n_p=n$, …
- For the voltage level $u_{c0}=ru_s/n$ ($f_{rc}=1$), $(n!/(r!(n-r)!))$ combinations of r switches in the on state exist and the remaining $(n-r)$ switches are in the 'off state' and then $n_p=(n!/(r!(n-r)!))$, …
- For the voltage level $u_{c0}=(n-2)u_s/n$ ($f_{(n-2)c}=1$), $(n(n-1)/2)$ combinations of $(n-2)$ switches in the 'on state' exist and two switches in the 'off state' exist ($n_p=(n(n-1)/2)$).

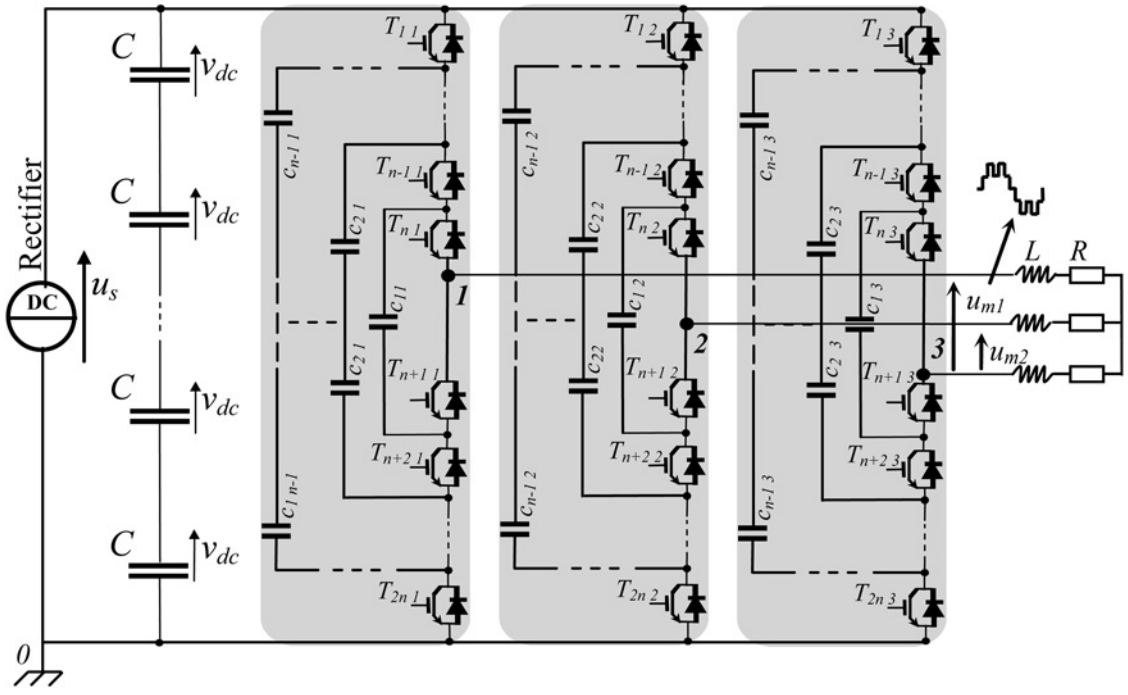


Fig. 1 *Schematic diagram of the three-phase (n + 1)-level FCMI*

doi: 10.1049/iet-pel.2013.0414

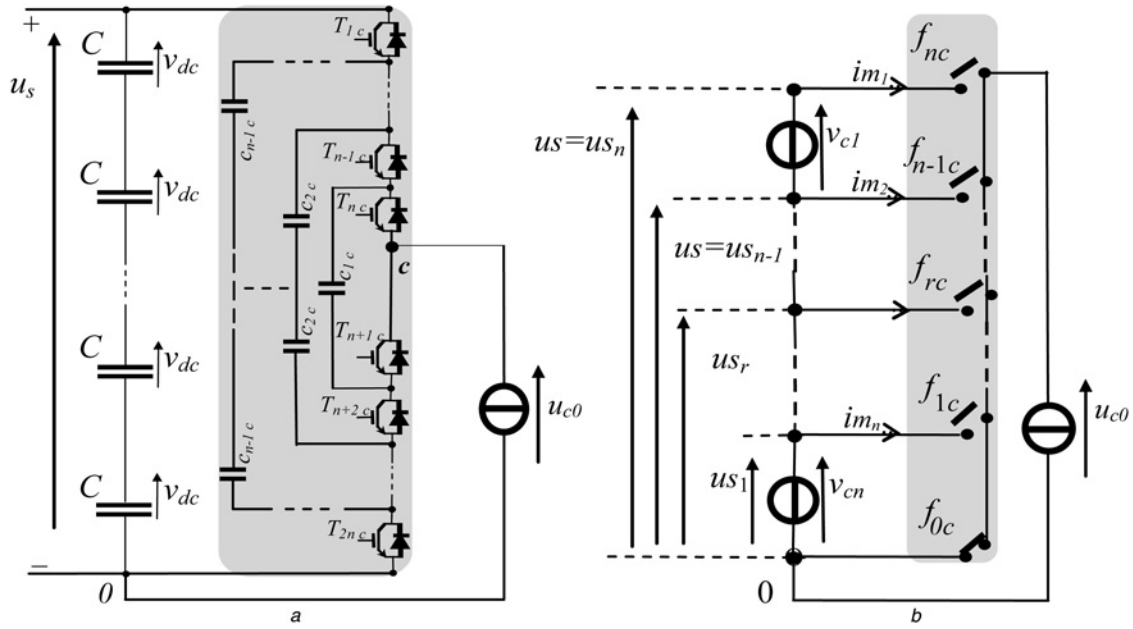


Fig. 2 *Output voltage of a phase leg c*

a Commutation circuit with semiconductors
b Equivalent circuit with ideal switches, $c \in \{1, 2, 3\}$

Table 1 Equivalent ideal switching

Gate signals					$\sum_{i=1}^{n} T_{ic}$	n_p	Switching functions					Output voltage
T_{1c}	T_{2c}	…	$T_{(n-1)c}$	T_{nc}			f_{0c}	f_{1c}	…	$f_{n-1\,c}$	$f_{n\,c}$	u_{c0}
0	0	…	0	0	0	$\binom{0}{n}$	1	0	…	0	0	$0 = u_{s_0}$
1	0	…	0	0	1	$\binom{1}{n}$	0	1	…	0	0	$\frac{1}{n} \cdot u_s = u_{s_1}$
0	1		0	0								
0	0		0	0								
			1	0								
0	0		0	1								
		:							:			:
		…			r	$\binom{r}{n}$	0	…	1	…	0	$\frac{r}{n} \cdot u_s = u_{s_r}$
		:							:			
0	1	…	1	1	$n-1$	$\binom{n-1}{n}$	0	0	…	1	0	$\frac{(n-1)}{n} \cdot u_s$
1	0		1	1								
1	1		1	1								
			0	1								
1	1		1	0								
1	1	…	1	1	n	$\binom{n}{n}$	0	0	…	0	1	$u_s = u_{s_n}$

• For the voltage level $u_{c0} = (n-1)u_s/n$ $(f_{(n-1)c} = 1)$, n combinations of $(n-1)$ switches in the on state exist and one switches in the off state exist $(n_p = n)$.
• For the voltage level $u_{c0} = u_s$ $(f_{nc} = 1)$, all upper switches T_{1c}, …, T_{nc} are turned on and it exists a single possibility $(n_p = 1)$.

We find that the number of upper switches in the on state is equal to the output voltage level u_{c0}

$$r = \sum_{i=1}^{n} T_{ic}, \text{ with } c \in \{1, 2, 3\} \tag{2}$$

Therefore this clamped commutation circuit is equivalent to a commutation circuit (Fig. 2*b*) where one ideal switch f_{rc} among $(n+1)$ switches is at anytime switched on. The switch states are called switching functions (f_{rc}). If $f_{rc} = 1$, the corresponding ideal switch (and so corresponding transistors diodes) is closed. Otherwise, if $f_{rc} = 0$, it is open. The last switch state is deduced from the other switch states as $f_{nc} = \bar{f}_{0c} \cdot \bar{f}_{1c} \cdots \bar{f}_{(n-1)c}$.

Hence, switching functions (f_{rc}) are defined as (Table 1)

$$f_{rc} = 1 \text{ if } \sum_{i=1}^{n} T_{ic} = r \text{ for } r \in \{0, \ldots, n\} \tag{3}$$

2^n switching states (T_{rc}) of each commutation circuit (c) exist and connect three phases from the capacitor–voltage divider to the load (Table 1).

Hence, by considering a continuous conduction mode, an equivalent converter with ideal switches may be considered

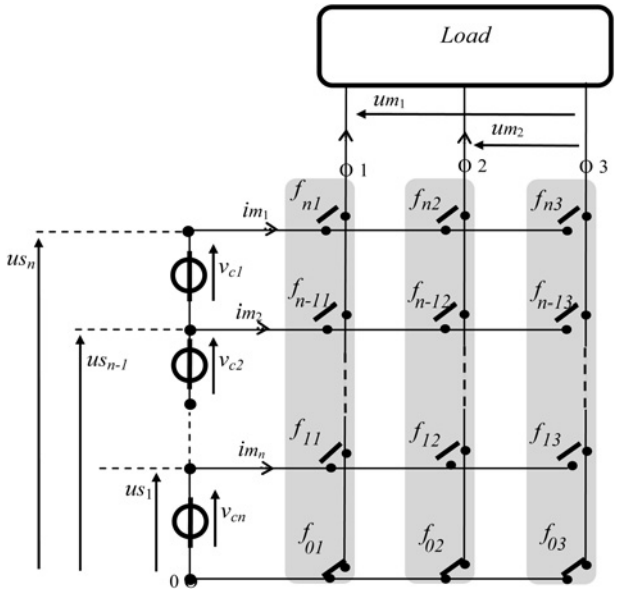


Fig. 3 *Equivalent matrix structure of a FCMI with three commutation cells of (n + 1) ideal switches*

for an easier study (Fig. 3). Table 1 shows possible switch combinations of the voltage levels and their corresponding switch states.

In order to implement wished switching functions ($f_{\text{ref\_}rc} = 1$), r gate signals of upper transistors are turned on and $(n - r)$ gate signals of upper transistors are turned off

$$\text{if } f_{\text{ref\_}rc} = 1 \text{ then } \sum_{i=1}^{n} T_{\text{ref\_}ic} = r \quad \text{for } r \in \{0, \ldots, n\}, \quad c \in \{1, 2, 3\} \tag{4}$$

For one commutation circuit, there is more than one combination to produce each output voltages among the set of voltages (u_s/n, $2u_s/n$, …, $(n-1)u_s/n$) (Table 1). Then the FCMI is more flexible than the DCI. By a proper selection of capacitor combinations, it is possible to balance the capacitor charge [1, 16]. As for the diode clamping, the capacitor clamping requires a large number of capacitors to clamp the voltage. Provided that the voltage rating of each used capacitor is the same as the main power switch, a $(n+1)$-level converter will require a total of $n(n-1)/2$ clamping capacitors per phase leg in addition to n main dc bus capacitors.

2.3 Equivalent matrix representation

To analyse the mathematical representation of the voltage conversion, an equivalent ideal matrix structure is used (Fig. 3) and is obtained from Fig. 1:

- by replacing chokes with current sources and capacitors by voltage sources,
- by using only two phase-to-phase modulated voltages (the third one can be deduced with others). This non-trivial consideration will simplify greatly the control algorithm, which can be designed without using Park transform and
- by bringing together all ideal switches in a matrix ($(n+1) \times 3$) containing vertical equivalent commutation circuits as explained in the previous section.

2.4 Analysis of multilevel operation

The phase to point 0 modulated voltages are mathematically given by the following equations (Fig. 2*b*)

$$u_{c0} = (u_c - u_0) = \sum_{r=0}^{n} f_{rc} us_r \tag{5}$$

and phase-to-phase modulated voltages are given by (Fig. 3)

$$\begin{aligned} um_1 &= u_{10} - u_{30} = \sum_{r=0}^{n} (f_{r1} - f_{r3}) us_r \\ um_2 &= u_{20} - u_{30} = \sum_{r=0}^{n} (f_{r2} - f_{r3}) us_r \end{aligned} \tag{6}$$

As input voltage sources are assumed to have a constant value, each phase-to-phase voltage is shaped through $(n+1)$ modulated voltages as

$$um_1 = \sum_{r=0}^{n} vm_{r1} \text{ and } um_2 = \sum_{r=0}^{n} vm_{r2} \tag{7}$$

In a general form, we obatin

$$um_p = \sum_{r=0}^{n} vm_{rp} \text{ with } p \in \{1, 2\} \tag{8}$$

The $2 \times (n+1)$ elementary modulated voltages are given by

$$vm_{rp} = m_{rp} \cdot us_r, \text{ with } r \in \{0, \ldots, n\} \text{ and } p \in \{1, 2\} \tag{9}$$

The modulation functions are defined as

$$m_{rp} = f_{rp} - f_{r3} \tag{10}$$

The multilevel voltage is obtained by the combination of dc capacitor voltages (us_r). A simultaneous magnitude and width modulation is possible. By using a 0 voltage level and a us/n voltage level, an $1/n$ level modulation is found. By using a us/n voltage level and $2us/n$ voltage level, a $2/n$ level modulation is obtained and so one. By using a $(n-1)us/n$ voltage levels and us/n voltage levels, a full level modulation is found.

2.5 Average modelling

The control system regulates the equivalent mean value of the modulated voltage in each modulation period [7]. The mean value of a modulated voltage in the modulation period (T_m) is given by

$$\langle um_p(t) \rangle = \left[\frac{1}{T_m} \cdot \int_{k.T_m}^{(k+1)\cdot T_m} um_p(t) \mathrm{d}t \right], \quad \text{with } k \in N \text{ and } t \in \left[k \cdot T_m, (k+1) \cdot T_m \right] \tag{11}$$

By assuming a constant dc bus voltage during a modulation period, the mean values of a modulation functions and

doi: 10.1049/iet-pel.2013.0414

voltage sources (8)–(10) are

$$\langle um_p(t)\rangle = \sum_{r=0}^{n} \langle vm_{rp}(t)\rangle \tag{12}$$

and

$$\langle vm_{rp}(t)\rangle = \langle m_{rp}(t)\rangle \cdot us_r \tag{13}$$

The mean value of a modulation function is therefore defined as

$$\langle m_{rp}(t)\rangle = \left[\frac{1}{T_m} \cdot \int_{k.T_m}^{(k+1)\cdot T_m} m_{rp}(t) \cdot \mathrm{d}t\right] \tag{14}$$

The mean value of a modulation function corresponds to a signed voltage ratio, which is defined according to one capacitor voltage.

3 Design of the control system

3.1 General control scheme

The block diagram representation describes the full causal process from gate signals to the equivalent average modulated multilevel voltage of the FCMI (Fig. 4). The proposed control system has been designed by a methodological inversion of this one. As a result, three main blocks enable a modulation method for the multilevel voltage source inverter.

Therefore, in order to ensure a correct multilevel operating of the FCMI, the control system is built with a connection controller and a direct SVM, which is based on the conversion controller and vector modulator.

3.2 Conversion controller for the matrix converter

The conversion controller for the matrix converter is obtained by the inversion of (13) and (12) and is designed as follows.

First per unit levels are defined as: $\underline{x} = (x/(us/n))$. The $(3\ n^2+3\ n+1)$ different configurations for the voltage space vector are represented in the frame $\left(0, \underline{\boldsymbol{um}}_1, \underline{\boldsymbol{um}}_2\right)$ (Fig. 5). Two different vectors can be joined by a line if it is possible to apply them by only one commutation. The frame is consequently divided into $(2{\cdot}3{\cdot}n^2)$ triangular areas. The average value of both modulated voltages may be set by switching, respectively, the three vectors, which define the sector where the desired voltage vector is located. The hexagon of the three level, five level and $(n+1)$ level are designed with bold lines. The presented vector approach has been used for a three-phase five-level NPC converter in [8] and then extended to a $(n+1)$-level DCI in [9].

The duration of each vector is determined by obtained projections onto the frame vectors $(0, \underline{\boldsymbol{um}}_1, \underline{\boldsymbol{um}}_2)$. For all square areas four triangular sectors have to be considered (Fig. 6). To find a general and simple algorithm, the sectors ① and ② are used. The two sectors ③ and ④ may be also used if one wants to make the DC link balancing using these redundant vectors or to minimise the number of commutations.

The function $(y = \mathrm{sign}(x))$ is defined as

$$y = \mathrm{sign}(x) = \begin{cases} 1 \text{ if } x > 0 \\ -1 \text{ if } x < 0 \end{cases} \tag{15}$$

Elementary duty cycles of modulated voltages according to the smallest voltage level (us/n) are defined as

$$d_1 = \langle \underline{um}_1 \rangle \text{ and } d_2 = \langle \underline{um}_2 \rangle \tag{16}$$

where $\langle \underline{um}_1 \rangle$ and $\langle \underline{um}_2 \rangle$ are the mean values of corresponding modulated voltages.

The sector where the vector is located may be detected by using a quantification function (*fix*), which is defined as

$$\begin{aligned} &y = fix(x) = a \text{ if } x \in [a, a + \mathrm{sign}(a)[, \\ &\text{with } a \in \{-(n-1), \ldots, -1, 0, 1, \ldots, (n-1)\} \end{aligned} \tag{17}$$

Therefore the *fix* functions return integer portions of numbers. In the case of a negative number argument, the function *fix* returns the first negative integer greater than or equal to number.

This sector is found thanks to parameters i and j defined as $i = fix(d_1)$ and $j = fix(d_2)$.

If the wished voltage vector is located as depicted in Fig. 6, two sectors, which are defined by three vectors, can be considered

Sector ①:

$$\begin{aligned} &\boldsymbol{u}_1 = u(i, j), \quad \boldsymbol{u}_2 = \boldsymbol{u}(i + \mathrm{sign}(d_1), j) \\ &\text{and } \boldsymbol{u}_3 = u(i, j + \mathrm{sign}(d_2)) \end{aligned} \tag{18}$$

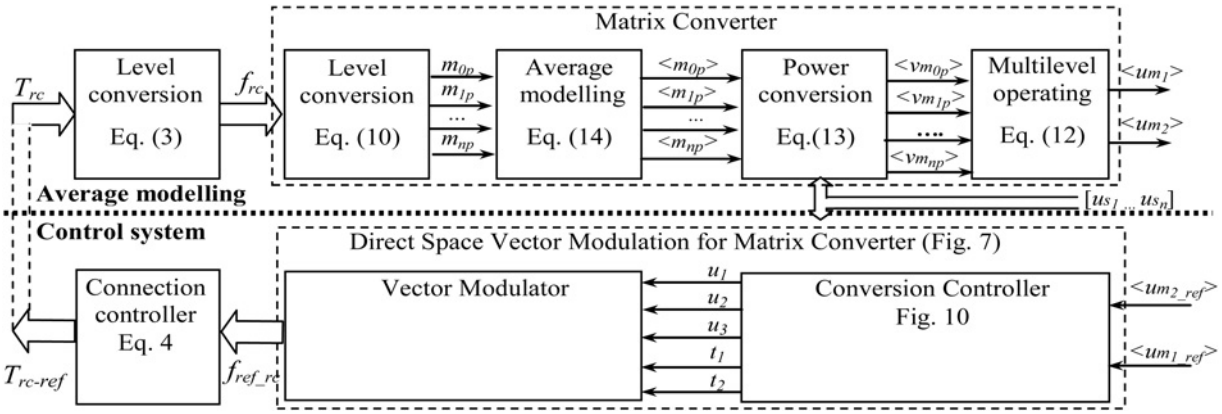


Fig. 4 *Modelling and control architecture of the FMCI*

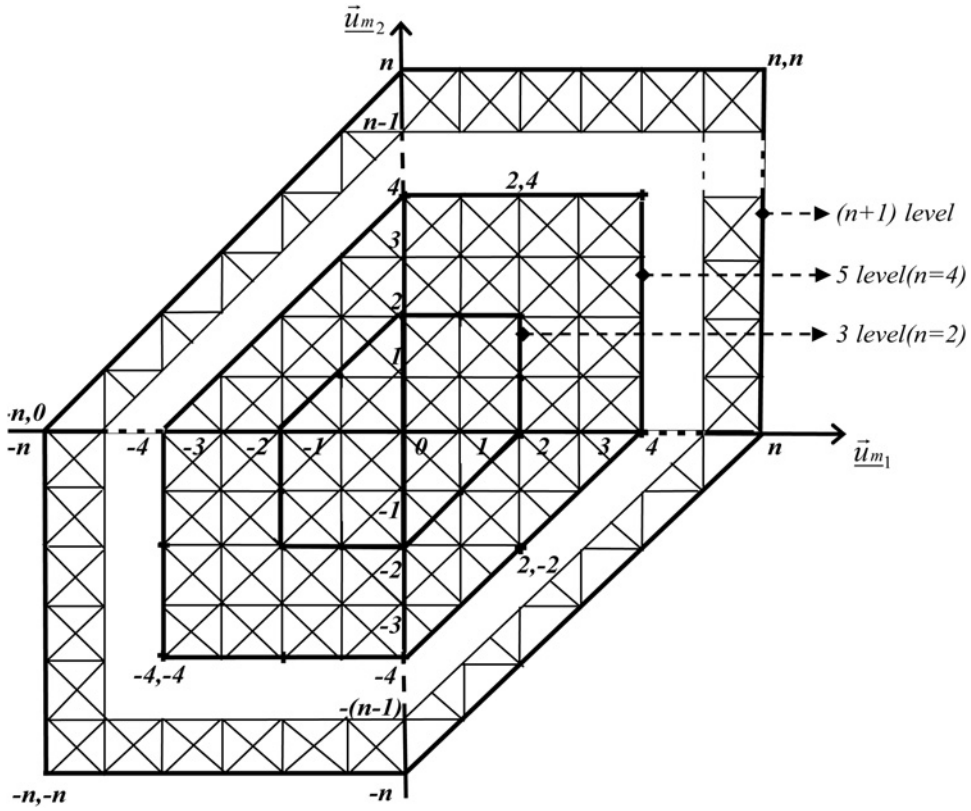


Fig. 5 *Space vector location into the frame (0, $\underline{um}_1$, $\underline{um}_2$)*

or sector ②

$$\begin{aligned} \boldsymbol{u}_1 &= u(i+\text{sign}(d_1), j+\text{sign}(d_2)), \\ \boldsymbol{u}_2 &= \boldsymbol{u}(i, j+\text{sign}(d_2)) \text{ and } \boldsymbol{u}_3 = u(i+\text{sign}(d_1), j) \end{aligned} \tag{19}$$

The modulated voltage vector can be timely generated by applying vectors $\boldsymbol{u}_1$, $\boldsymbol{u}_2$ and $\boldsymbol{u}_3$ during respective durations t_1, t_2 and t_3

$$\underline{\boldsymbol{um}} = \frac{t_1}{T_\text{m}} \cdot \boldsymbol{u}_1 + \frac{t_2}{T_\text{m}} \cdot \boldsymbol{u}_2 + \frac{t_3}{T_\text{m}} \cdot \boldsymbol{u}_3 \tag{20}$$

with the coordinated variation domains of $\underline{\boldsymbol{um}}$, $\boldsymbol{u}_1$, $\boldsymbol{u}_2$ and $\boldsymbol{u}_3$ is $\{(-n, -n), \ldots, (n, n)\}$ (Fig. 5).

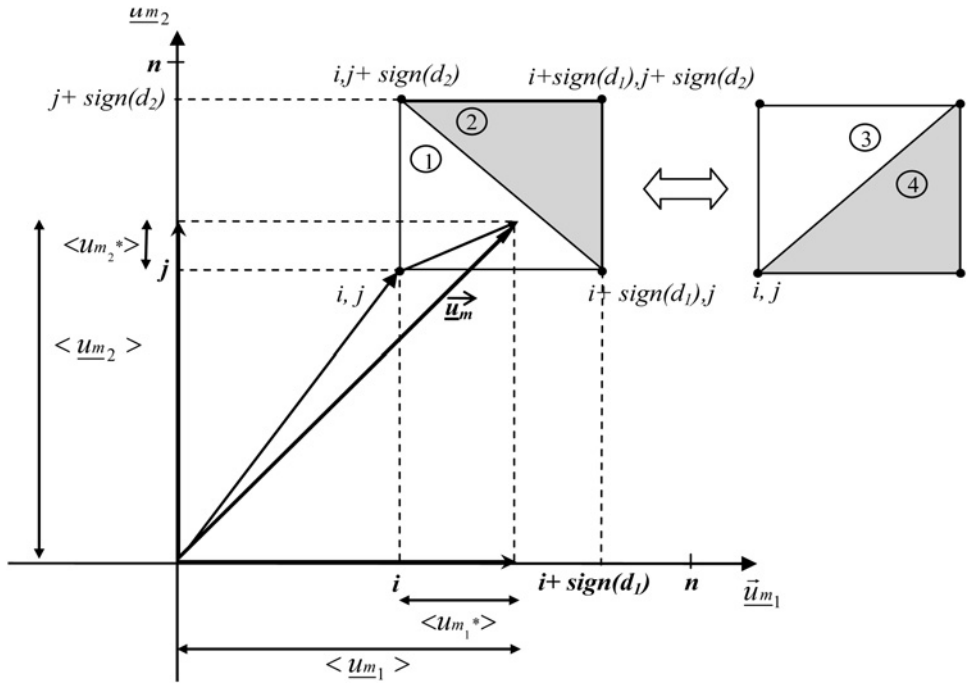


Fig. 6 *Expanded view of the studied sector*

doi: 10.1049/iet-pel.2013.0414

In fact only two durations must be determined because the sum of all durations should be equal to the modulation period T_m

$$t_1 + t_2 + t_3 = T_m \tag{21}$$

Let us consider that the duration of vector $\boldsymbol{u}_1(t_1)$ is fixed, then, by using (20) and (21), we obtain

$$\underline{\boldsymbol{um}} = \frac{1}{T_m} \cdot \left(t_2 \cdot \left(\boldsymbol{u}_2 - \boldsymbol{u}_1 \right) + t_3 \cdot \left(\boldsymbol{u}_3 - \boldsymbol{u}_1 \right) + T_m \cdot \boldsymbol{u}_1 \right) \tag{22}$$

If we use the projections of the reference voltage vector onto axis (0, $\underline{\boldsymbol{um}}_1$, $\underline{\boldsymbol{um}}_2$) the desired modulated voltage can be also expressed as (Fig. 6)

$$\underline{\boldsymbol{um}} = \langle \underline{um}_1 \rangle \cdot \underline{\boldsymbol{um}}_1 + \langle \underline{um}_2 \rangle \cdot \underline{\boldsymbol{um}}_2 \tag{23}$$

A simple expression is obtained by using the location of the operation domain (i, j) and per unit durations of modulated voltages $\left(\langle um_1^* \rangle, \langle um_2^* \rangle \right)$ which corresponds to this domain as (Fig. 6)

$$\underline{\boldsymbol{um}} = \left(i + \langle um_1^* \rangle \right) \cdot \underline{\boldsymbol{um}}_1 + \left(j + \langle um_2^* \rangle \right) \cdot \underline{\boldsymbol{um}}_2 \tag{24}$$

1. If the modulation voltage is located in triangle ①, that is, $\left| \langle um_1^* \rangle \right| + \left| \langle um_2^* \rangle \right| \leq 1$: the vector $\boldsymbol{u}_1 = \boldsymbol{u}(i, j)$ is chosen as the corner vector and it is expressed as follows

$$\boldsymbol{u}_1 = \boldsymbol{u}(i, j) = i \cdot \underline{\boldsymbol{um}}_1 + j \cdot \underline{\boldsymbol{um}}_2 \tag{25}$$

The choice of vectors $\boldsymbol{u}_1$, $\boldsymbol{u}_2$ and $\boldsymbol{u}_3$(18) gives

$$\begin{cases} \boldsymbol{u}_2 - \boldsymbol{u}_1 = \text{sign}(d_1) \underline{\boldsymbol{um}}_1 \\ \boldsymbol{u}_3 - \boldsymbol{u}_1 = \text{sign}(d_2) \underline{\boldsymbol{um}}_2 \end{cases} \tag{26}$$

Using (25) and (26), (22) becomes

$$\underline{\boldsymbol{um}} = \left(\left(\frac{t_2}{T_m} \text{sign}(d_1) + i \right) \underline{\boldsymbol{um}}_1 + \left(\frac{t_3}{T_m} \text{sign}(d_2) + j \right) \underline{\boldsymbol{um}}_2 \right) \tag{27}$$

As (24) is equal to (27), time durations of vectors are deduced

$$t_2 = T_m \cdot \left| \langle um_1^* \rangle \right|, \text{ and } t_3 = T_m \cdot \left| \langle um_2^* \rangle \right| \tag{28}$$

2. If the modulation voltage is located in triangle ②, that is, $\left| \langle um_1^* \rangle \right| + \left| \langle um_2^* \rangle \right| > 1$: the vector $\boldsymbol{u}_1 = \boldsymbol{u}(i + \text{sign}(d_1),$

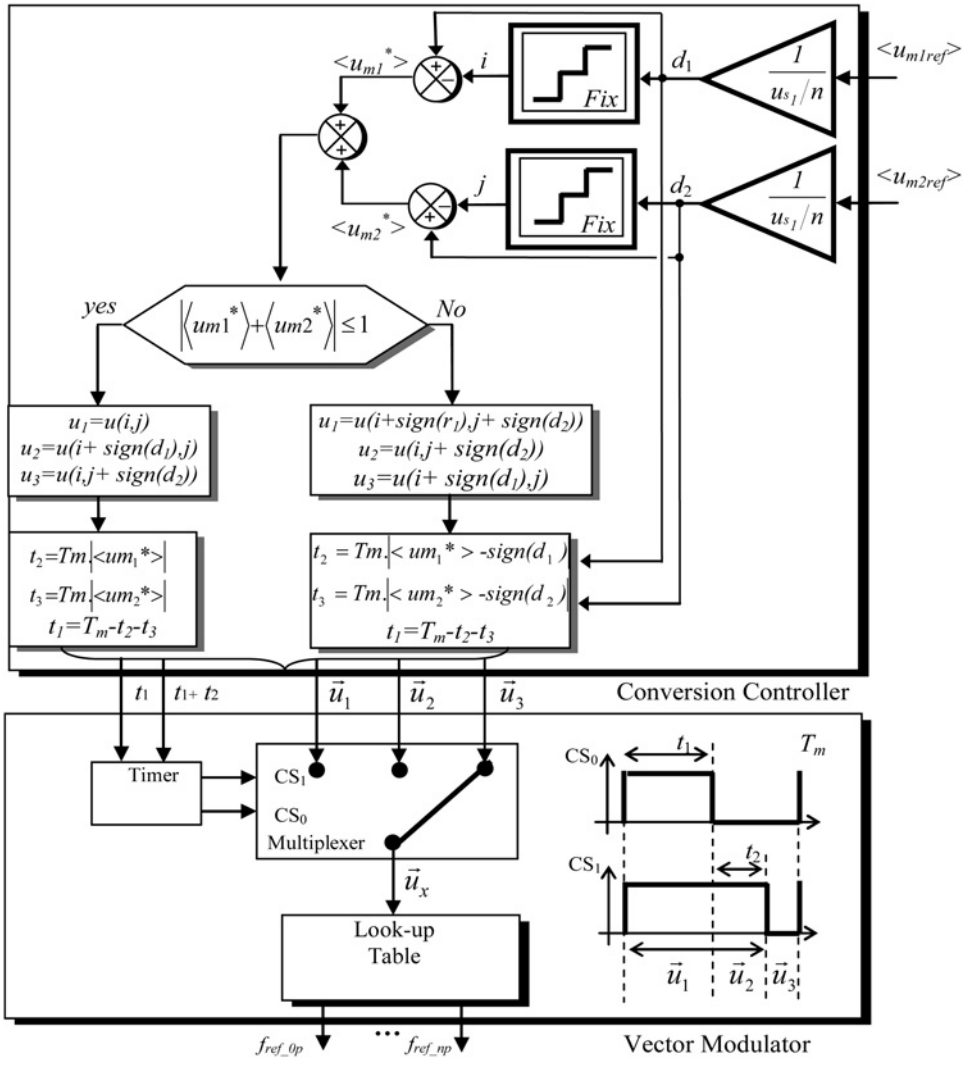


Fig. 7 *Direct SVM for the three-phase matrix converter*

$j + \text{sign}(d_2)$) is chosen as the corner vector and it is expressed as follows

$$\begin{aligned} \boldsymbol{u}_1 &= \boldsymbol{u}(i + \text{sign}(d_1), j + \text{sign}(d_2)) \\ &= \big(i + \text{sign}(d_1)\big)\underline{\boldsymbol{um}}_1 + \big(j + \text{sign}(d_2)\big)\underline{\boldsymbol{um}}_2 \end{aligned} \tag{29}$$

Now, considering the triple of vectors given by (19), we obtain following expressions

$$\begin{cases} \boldsymbol{u}_2 - \boldsymbol{u}_1 = -\text{sign}(d_1)\underline{\boldsymbol{um}}_1 \\ \boldsymbol{u}_3 - \boldsymbol{u}_1 = -\text{sign}(d_2)\underline{\boldsymbol{um}}_2 \end{cases} \tag{30}$$

Equation (22) is rewritten as

$$\begin{aligned} \underline{\boldsymbol{um}} = &\left(\left(-\frac{t_2}{T_{\text{m}}}\text{sign}(d_1) + i + \text{sign}(d_1)\right)\underline{\boldsymbol{um}}_1\right. \\ &\left.+\left(-\frac{t_3}{T_{\text{m}}}\text{sign}(d_2) + j + \text{sign}(d_2)\right)\underline{\boldsymbol{um}}_2\right) \end{aligned} \tag{31}$$

The identification of this vector (31) with coordinates of the wished modulation vector (24), durations are easily found

$$\begin{aligned} t_2 &= T_{\text{m}}\left|\langle um_1^* \rangle - \text{sign}(d_1)\right|, \\ \text{and } t_3 &= T_{\text{m}}\left|\langle um_2^* \rangle - \text{sign}(d_2)\right| \end{aligned} \tag{32}$$

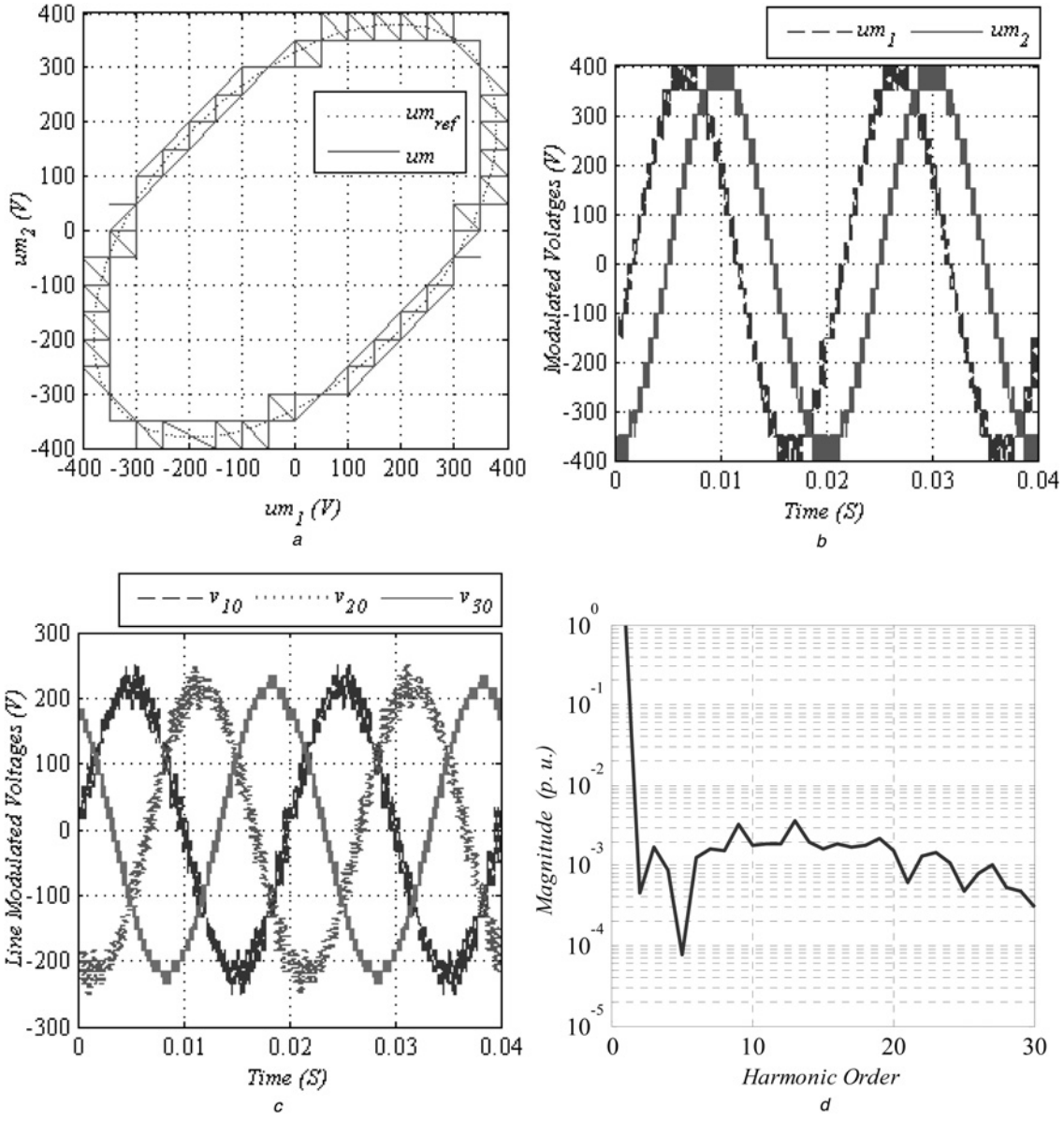


Fig. 8 *Simulation results with a nine-level FCMI*

a Reference modulated voltages and switching vectors
b Modulated voltages (u_{m1} and u_{m2})
c Line modulated voltages (v_{10}, v_{20} and v_{30})
d Harmonic spectrum of the modulated voltage v_{10}

doi: 10.1049/iet-pel.2013.0414

3.3 Vector modulator

The vector modulator has been designed with a multiplexer whose output selector is controlled by a timer (Fig. 7). According to the wished references ($\langle um_{1\_ref}\rangle$ and $\langle um_{2\_ref}\rangle$), the region is located, the three vectors are selected and corresponding values of x are applied to the multiplexer. Moreover the durations (t_1 and t_2) are sent to the timer. With such modulators, modulation voltage references are then made equal to mean value modulation voltage references, that is, $\langle um_{r\_ref}\rangle = um_{r\_ref}$.

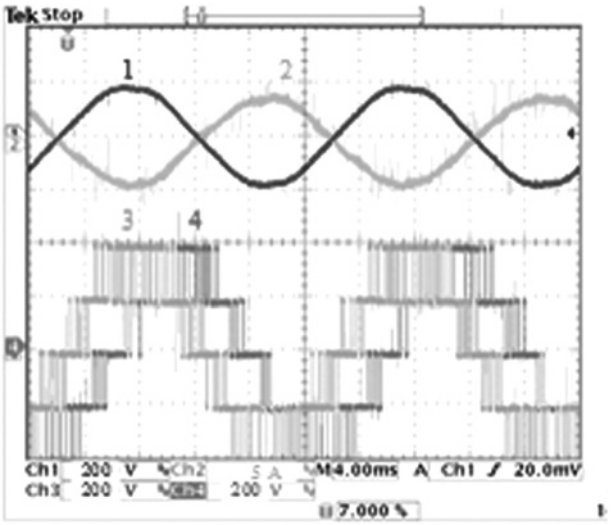
Fig. 7 shows the direct SVM for the matrix converter, which is composed of the conversion controller for the matrix converter and vector modulator.

3.4 Connection controller

The connection controller processes corresponding gate signals in order to set a wished modulation functions via the inverse of (10) and (4) or Table 1. Therefore the connection controller is the inverse modelling of the level conversion of the FCMI (Fig. 4).

4 Simulation results

Using the developed general modelling and control algorithm based on the use of the matrix converter (Fig. 4), the voltage waveforms of a nine-level FMCI are shown in Fig. 8. The fundamental frequency is 50 Hz and the modulation frequency is 5 kHz. The reference line-to-line voltage draws an ellipse in the frame $(0, \underline{\boldsymbol{um}}_1, \underline{\boldsymbol{um}}_2)$ and their corresponding used sectors are shown in Fig. 8*a*. The line-to-line modulated voltages and their references are depicted in Fig. 8*b*. The obtained three-phase output line voltages of the FCMI are shown in Fig. 8*c*. To highlight the good sinusoidal waveforms of the first line voltage v_{10} the FFT (harmonic spectrum) is calculated and depicted in Fig. 8*d*. In front of the fundamental component, higher harmonics are negligible and their maximum value is approximately 0.36%. The developed equivalent model uses the simple algebraic equations by taking into account the number of levels and the redundant vectors. Then, the space vector PWM for a direct matrix converter is used with inverse modelling to control the FCMI.



1: line voltage 2: line current 3: Modulated voltage (um_{13})
4: Modulated voltage (um_{23})

Fig. 9 *Scope hardcopy of the NPC three-level converter*

5 Experimental results

Experimental tests have been carried out to validate the direct SVM (Fig. 7) of the three-level NPC Converter. The fundamental frequency is 50 Hz and the modulation frequency is 3 kHz. The scope hardcopy (Fig. 9) shows the line voltage, line current and the modulated voltage. This figure shows the three-level voltages generated by the NPC converter. It is worth mentioning that this control strategy has been used successfully for the control of a three-phase three-level converter, used for the grid connection of a renewable energy-based generator.

6 Conclusion

In this paper, the fundamental work is the modelling of the FCMI [$(n+1)$ level] to obtain the matrix converter equivalent structure. The switch combinations of the output voltage and their corresponding switch states are defined by using ($3n$) switching functions. First, a SVM has been used to control the matrix converter. Then using mathematical inversion of the modelling equations the switch states of the FCMI are given. Therefore the modelling and control of the FCMI are simplified by using an equivalent matrix converter. This modelling and control system is validated through experimental test, using a three-level NPC converter and by simulations of nine-levels FCMI topology.

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doi: 10.1049/iet-pel.2013.0414