A Tool for Automatic Radiation-Hardened SRAM Layout Generation

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***Abstract*—A new era of space exploration is emerging, characterized by a rapid surge in satellites and significant cost reductions. Memory circuits play a vital role in space applications, and it is essential to develop techniques to address the radiation-induced upsets in these circuits. This work extends a previously presented method to detect Multiple-Cell Upsets (MCU) in SRAMs for space applications. The method involves spatially interleaving an SRAM array with a network of radiation detectors. Considering the relationship between the radiation-hardening level and the area penalty added by the detection cells, a tool for automatically generating the SRAM layout with different configurations was developed and is presented in this work. The developed tool facilitates using the new method in commercial applications, providing different levels of protection according to the environment in which the circuit will be exposed.**

***Index Terms*—automatic layout generation, detection cell, multiple-cell upsets, radiation hardening, SRAM**

I. Introduction

With the advancement of space exploration, the need to design radiation-tolerant circuits, particularly memory circuits, becomes increasingly critical [1]. The advent of new nanotechnologies has led to a considerable reduction in transistor dimensions and cell sizes. Consequently, a single radiation-induced particle impact can affect more than one memory cell in a memory plan, resulting in the transition from SEU to Multiple-Cell Upset (MCU) [2], [3].

Numerous techniques at different levels are presented in the literature to tackle radiation effects. Redundancy-based solutions, while extensively explored across various implementation strategies [4], increase system complexity. The basic Hamming code [5] is a widely used solution that can detect two errors and correct one within a single data word. However, Error Detection And Correction (EDAC) algorithms need redundant bits whose number increases with the number of errors to detect and correct [6]. The adoption of Radiation-Hardening-By-Design (RHBD) memory cells [7] does not allow the detection and thus the correction of radiation-induced corruptions of data. RHBD cells usually have more transistors than traditional designs, increasing the circuit area.

All the techniques presented have in common, mainly area and power consumption penalties. These penalties are already expected in the radiation-tolerant circuit design and are also present in the new method proposed in [8], which gave rise to the EDA tool developed and presented in this work. However, considering the significant increase in the MCU rate for new technological nodes, the existing techniques may not provide a satisfactory level of robustness depending on the application needs [2], [9]. The advantage of the method presented in [8] is the increase in fault detection capability (evaluated by laser testing in [10]) according to the increase in the number of events. Unlike the techniques already in the literature, the method benefits from increasing multiple events, achieving a high detection rate even in a high MCU rate environment.

Despite the significant advantage of the method for detecting MCUs, the main challenges for its use in commercial circuits are the modification of a conventional SRAM array, with the insertion of exclusive cells for detection between the traditional cells, and the significant reduction in SRAM storage capacity. In this context, this work extends the previously presented method by developing a radiation-hardened SRAM layout generation tool. The main goal and focus of the work is to provide an easy-to-use tool to minimize the challenges mentioned above, leaving it up to the designer to determine, based on the data generated by the tool, the best cost-benefit ratio concerning the level of protection and area penalty.

II. The Detection Method

Before presenting the developed tool, it is essential to understand the architecture and operation of the method proposed in [8]. The method, illustrated in Fig. 1, involves spatially interleaving a memory array with a network of radiation detectors. For optimal coverage of the memory array with minimal detection cells, it is preferable to percentage-driven place the detection cells in an interleaved manner with the data cells. At the bottom of the memory array, a logic circuit is integrated to generate an alarm signal whenever a radiation-induced

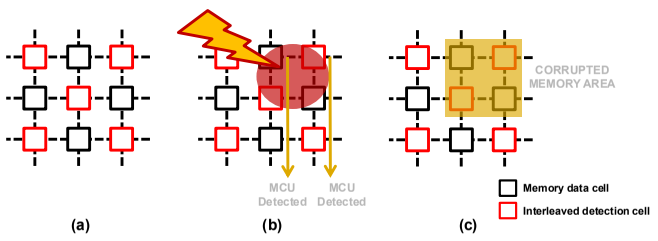


Fig. 1. The detection method idea: (a) Memory plan spatially interleaved; (b) Alarm signal; (c) Cluster of physically adjacent data cells [8].

particle alters the state of a detector. Following the impact, the detection cells are automatically refreshed to their initial state. The alarm signal is then transmitted to the processor, enabling it to initiate an interruption or carry out a total/partial memory refresh. The main advantage of this solution is that the technique does not present an event detection limitation, according to the increase of SEUs and MCUs. The method was already validated through electrically-induced SEU/MCU and laser testing, as presented in [10]. According to the number of n-bit MCUs that impact an SRAM array, mainly their shapes [3], and considering the ratio between detection and data cells as the maximum provided by the developed tool (50%), the MCU detection capability (considering only the SRAM core) can reach close to 100%. SEUs that exclusively impact data cells would not be detected.

A. Architecture

At the bottom of the SRAM array, the detection logic circuit responsible for creating the alarm signal is designed in a tree structure composed of NAND2/NOR2 logic gates and an SR Latch circuit. To provide a clear understanding of the detection method's architecture and operation, the electrical schematics displayed below will solely depict the detection cells. It is important to note that both data and detection plans will be interleaved and physically together in the SRAM. Fig. 2 presents the electric schematic of a small part of the SRAM core, highlighting the detection logic and the detection cell architecture. In every two columns of the SRAM core, the detection lines (DL) are connected to the NAND2 gates positioned on the first level of this circuit. The outputs of these same gates are used to send this signal back to the cell plan through the refresh line (RL) and propagate the signal to the other NOR2 and NAND2 gates in the circuit to get a single alarm signal through the SR Latch output. The method introduces some overheads in terms of area (around 150% considering the worst-case) and power consumption, which are better described in [10].

The detection cell architecture was defined based on the traditional 6T-SRAM bit cell. The goal is to design a detection cell that balances area and radiation sensitivity like the widely adopted memory cell. The 6T-SRAM core is maintained with two PMOS and NMOS transistors forming a cross-coupled pair of inverters. However, the NMOS access transistors are replaced by pairs of PMOS/NMOS transistors in charge of detecting and refreshing the detection cell after a state change.

B. Operation

The left-side PMOS/NMOS transistor pair in the detection cell is responsible for detecting any alteration in the stored value. Conversely, the transistors located on the right side are responsible for refreshing the cell back to its initial state after a state change has occurred. Fig. 3a and Fig. 3b present schematics composed with only detection cells to better illustrate the detection method operating modes. In regular operation (no cell impacted), all the detection cells store a '0' logic value. In this case, considering a single detection cell view (presented in Fig. 2), there is an ON-state PMOS (P0) and an OFF-state NMOS (N0) transistor on the detection side, allowing VDD to pass through the detection line and reach the detection logic circuit (DL_{0_OUT} = '1'). Through the first level NAND2 logic gate output (RL_0), this same signal arrives at the right side of the detection cell, where the ON-state NMOS (N3) and OFF-state PMOS (P3) transistors will keep the value stored by the cell. This signal is also propagated through the detection logic keeping the alarm signal off.

If one or more cells in the plan are affected, causing a change in the stored logic value, there is an inversion in the states of all the transistors abovementioned. Thanks to the ON-state NMOS transistor on the left side of the detection cell (N0), in this operation mode, VDD is no longer passing through the detection line but GND. This value also modifies the NAND2 output at the first level (RL_{0_OUT} = '0'), which is propagated throughout the detection logic, modifying the output of the last level NOR2 gate and therefore triggering the alarm signal ($SIGNAL_{NxN}$ = '1'). That same signal also arrives on the right side of the detection cell, causing the cell to retrieve the value previously stored. If an upset impacts the detection logic, a false alarm may be generated, which may cause non-impacted data cells to be reset unnecessarily.

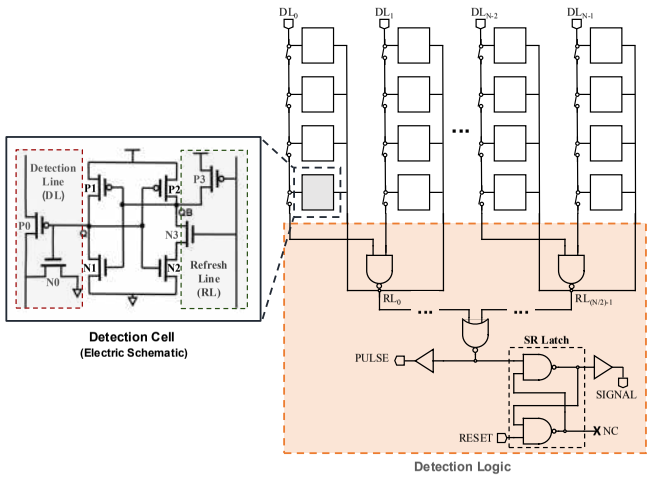


Fig. 2. The detection plan schematic, highlighting the detection logic and the detection cell architecture.

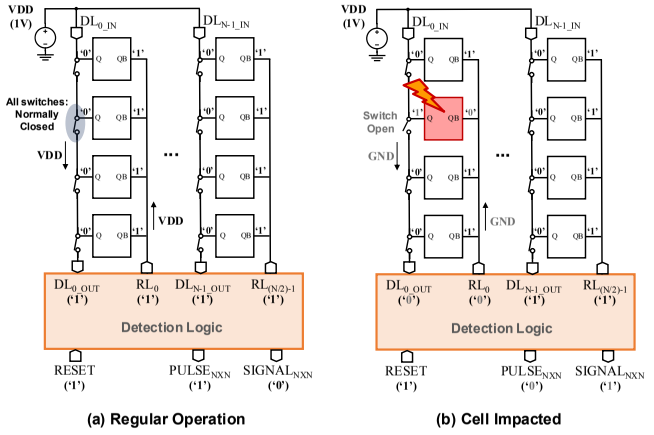


Fig. 3. Detection method operation modes: (a) Regular operation (no event); (b) Cell impacted by a radiation event.

III. Radiation-Hardened SRAM Layout Generation Tool

Because it is customizable, the presented method allows varying the number of added detection cells aiming at the relationship between robustness and overheads. The design of a conventional SRAM is not a trivial task; designing an SRAM that implements the proposed method with data and detection cells becomes more challenging. The main goal of the developed tool is to automatically generate the layout of the core of a radiation-hardened SRAM, facilitating the application of the new method and providing multiple sizes and protection configurations. The tool also provides the option of automatically generating the schematic of the generated layout, a function of utmost importance due to the difficulty in logically relating many data and detection cells. Two types of data inputs are available to determine the size of SRAM that will be generated: number of rows and columns or memory size. In the first option, the user is free to insert the desired number of rows and columns, the tool being responsible for validating the data according to the rules of an SRAM array. In the second option, six different predefined memory sizes (from 1 kb to 1 Mb) are available to the user.

The differential of the presented method is the insertion of exclusive cells to detect radiation-induced upsets. Thus, the developed tool offers five different levels of radiation robustness for generating the SRAM layout. Level 0 does not add any detection cells to the memory plan and creates a traditional unhardened SRAM array. From level 1 to level 4, different percentages of detection cells (ranging from 12.5% to 50%) are interleaved in the memory plan, always looking for the best array coverage. The detection logic circuit is not generated automatically by the tool; it is necessary to add it manually after generating the core layout. The tool was implemented in the SKILL language to ensure integration with a prominent tool in integrated circuit design. Algorithm 1 presents a summarized view of the code developed for the tool's implementation.

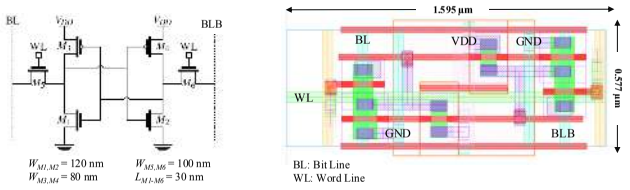
It is essential to highlight that the tool uses small pre-designed macros to replicate them to generate different SRAM core layout options. For the design of these macros, only the data and detection cell layouts that will be used in SRAM are needed. Fig. 4a and Fig. 4b show the electrical schematic and layout of the data and detection cells designed in the 28 nm FD-SOI technology from ST Microelectronics used in this first version of the tool. Among the different models available on this Process Design Kit (PDK), this work considers the regular threshold voltage (RVT). The architecture chosen for the data cell design was the traditional 6T-SRAM. The data and the detection cell layouts, shown in Fig. 4, were designed using the rectangular-diffusion topology [11]. This topology is commonly used for high-density SRAMs, reducing the bit cells area and process variability [12]. Using DRC clean macros, the tool will also generate the final SRAM layout without DRC errors, regardless of the technological node used.

Algorithm 1: Automatic SRAM layout generation tool

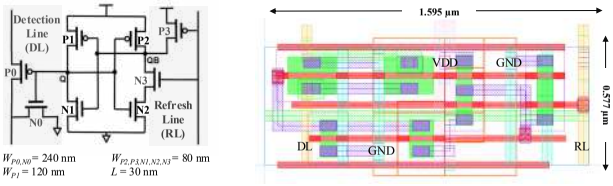
```
set_bindkey; ⇒ To start the tool.
display_form;
Input Data: ⇒ Receive data from user.
Bool ← bool; ⇒ To select the input data method.
Bool2 ← bool2; ⇒ Schematic generation option.
Row ← row; ⇒ Number of rows in the SRAM core.
Col ← col; ⇒Number of columns in the SRAM core.
Size ← size; ⇒ Memory size method.
Macro ← macro; ⇒ Radiation hardening level.

⇒ Check data input method.
if bool is 0 then
    if size is "1 kb or 4 kb or ... 1 Mb" then
        row ← 32 or 64 or ... 1024;
        col ← 32 or 64 or ... 1024;
    end
end
⇒ Input data validation.
if log2(row) & log2(col) are INTEGERS then
    cv ← open_cell_view();
    if macro is "0% or 12.5% or ... 50%" then
        create_layout(cv macro row col);
        ⇒ Create the schematic view.
        if bool2 is 1 then
            create_schematic(cv macro row col);
        end
    end
    ⇒ Prepare layout information.
    num_cells ← row × col;
    num_detection ← macro × num_cells;
    data_capacity ← (num_cells − num_detection) / 1024;
    display_succesfull_message;
    display_layout_information;
else
    display_error_message;
end
```

IV. Tool Execution and Results

After creating a cell view layout in Cadence® Virtuoso, the tool is started by pressing a defined shortcut key. Figure. 5 shows the new window that appears over the cell view window, with all the functions available for generating the SRAM layout: SRAM core dimensions, radiation hardening level, and generation of the schematic view. In Fig. 6, an example of the tool's execution is presented. In step 1, the data entry method is chosen, the desired number of rows and columns (16×16) is entered, and the radiation hardening level is set (1) via the slide button. In step 2, the layout is generated, and a success message appears on the screen. In the image, it is possible to observe the detection cells positioned between the SRAM data cells in a smaller amount (12.5%). Finally, step 3 presents the generated layout information: total number of cells, number of detection cells, and data storage capacity.



(a) 6T-SRAM bit cell: electric schematic and layout.



(b) Detection cell: electric schematic and layout.

Fig. 4. Electric schematic and layout of data and detection cells used in the SRAM array: (a) 6T-SRAM bit cell and (b) Detection Cell.

The generated layout information helps know the newly created layout's characteristics and compares the cost-benefit between circuit protection level, storage capacity, and area penalty. From protection levels 1 to 4, a reduction in storage capacity is observed following the increase in the percentage of detection cells (from 12.5% to 50%). From this data, it is possible to determine the area overhead in the SRAM core layout (without considering the two extra detection cell's transistors), which, considering levels 1 to 4, equals 14.3%, 33.33%, 60%, and 100%, respectively. Based on the results generated by the tool and defining the necessary protection level according to the environment in which the circuit will operate, it is possible to automatically generate the SRAM core layout with the lowest area penalty possible.

V. Conclusion

This work extended the previously presented method to detect multiple upsets in SRAMs by developing a radiation-hardened SRAM layout generation tool. Despite area and power consumption penalties, the advantage of the method

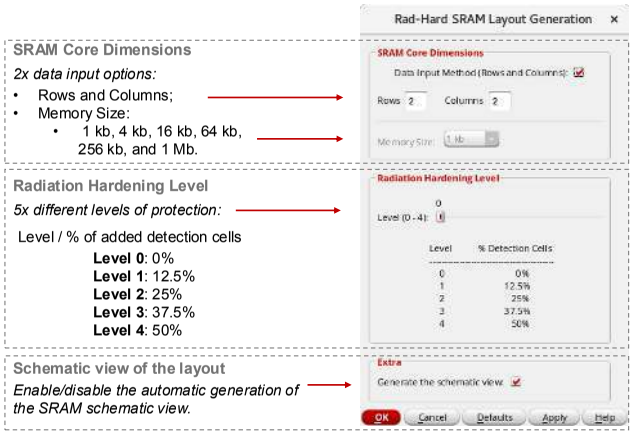


Fig. 5. Automatic SRAM layout generation tool main window, highlighting all the available features.

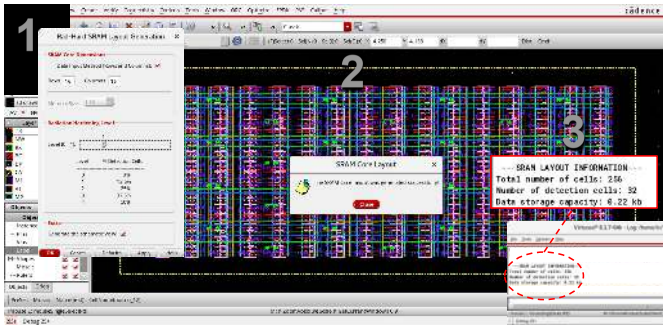


Fig. 6. An example of running the tool: (1) defining the input data, (2) generating the SRAM layout, (3) providing layout information.

is that it benefits from the increase of multiple events and achieves a high detection rate even in the harshest environments. One of the main challenges of applying the new detection method is the significant area penalty, reaching around 144% in the circuit presented in [10] and consequently reducing memory storage capacity. With the development of the tool presented in this work, this problem is minimized since it is up to the designer to determine, based on the information generated by the tool, the best cost-benefit ratio concerning the level of protection and area penalty. The tool also facilitates the task of generating the core layout of an SRAM, providing unlimited array sizes with different levels of protection to be chosen according to the project's needs.

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