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# Thermal coupling assessment for a PCB-based package with embedded chips and graphite heat spreader

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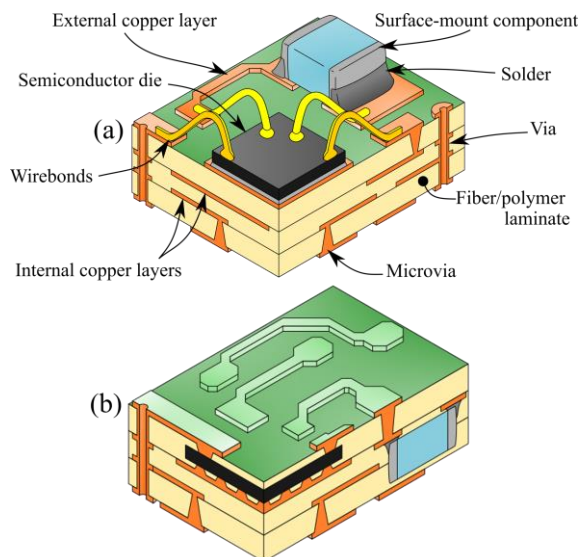
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## Abstract

A graphite heat spreader designed to be compatible with printed circuit board (PCB) embedding technology is demonstrated. It is suited to wide-bandgap devices and high-power loss density requirements ( $> 500 \text{ W/cm}^2$ ). PCB samples integrating a graphite heat spreader stack are designed and fabricated then compared to a reference sample, through both simulation and experimental analysis. It is found that the graphite spreader reduces thermal resistance by up to 38 %, while increasing thermal coupling between adjacent chips by 3-fold.

## 1 Introduction

Among the emerging packaging solutions for power electronic devices, PCB-embedding of semiconductor chips (**Figure 1**) is one of the most promising solutions to replace the standard power module technology which uses Direct Bonded Copper (DBC: ceramic) substrate and wire bonding [1]. The packaging of an embedded die has a low parasitic inductance which is well suited for fast switching wide-bandgap devices such as SiC MOSFET [2]. However, performances must be accompanied by low cost, high reliability and good thermal management for this new technology to be able to compete with existing ones. In



**Figure 1:** (a) Classical PCB package. (b) Embedded PCB package.

multichip packaging, the effect of thermal coupling between the two diodes can be desirable for some applications in order to have a balance in junction temperature between the two chips, for example in the case parallel connection as it helps having a coherent aging of all the chips in the package at the same speed [3].

In PCBs, the dielectric is usually an epoxy-based material with low thermal conductivity compared to the conductive copper layer ( $< 1 \text{ W/(m.K)}$  vs.  $400 \text{ W/(m.K)}$ , respectively), limiting heat spreading around the die. To overcome this limitation, we propose to insert a material with high-thermal conductivity in the PCB stack: sheets of layered pyrolytic graphite material, with an anisotropic thermal conductivity that can go up to  $1500 \text{ W/(m.K)}$  in-plane. This provides the advantage of a low-thermal resistance lateral path for the heat. This lateral path adds to the existing vertical one provided by the copper vias, resulting in an improved thermal performance.

In our previous work [4], single embedded die PCB packages with embedded graphite heat spreaders were designed and successfully fabricated, demonstrating the compatibility of graphite layers with the PCB manufacturing process in particular with the PCB embedding technology. Electrical characterization tests were performed and a manufacturing yield for the embedded semiconductor devices of 86 % was obtained which is a good yield for a first prototype run. Thermal impedance measurements showed that up to 38 % reduction in junction to ambient thermal resistance  $R_{thJA}$  and 30 % reduction in junction to case thermal resistance  $R_{thJC}$ .

In this paper, we investigate PCBs with two power devices (diodes) embedded, to analyze the effect of the heat

spreader on the thermal coupling between the devices. The manufacturing process of PCB with embedded graphite is presented as well as the resulted improvement in thermal performance and the associated effect on the thermal coupling between the two embedded diodes. Finally, a simplified Thermal Equivalent Circuit Model (TECM) is generated in order to describe the transient thermal behavior.

## 2 PCB embedding process with graphite

The PCB manufacturing process with embedded dies starts by stacking up conductive layers (copper) and un-cured dielectric layers (glass fiber/epoxy resin) called prepreg. The embedded SiC chip is placed in a cavity formed in prepregs. After that, the stack-up is laminated resulting in a die embedded in a solid PCB. In order to interconnect the embedded chip to outer copper layers, vias are drilled by laser on both sides of the PCB package (Figure 2). In addition, through-hole vias are drilled mechanically to interconnect the top and bottom external copper layers. The vias are then plated with copper using an electroplating process. Finally, the copper layers are chemically etched to form the electrical circuit. More layers of copper can be stacked with epoxy layers in the same way to produce a multi-layer PCB.

In this proposed package assembly shown in Figure 2, graphite layers are stacked together with adhesive layers and placed in a cavity of the prepreg (as for the SiC chips) during the stack-up process. Micro vias are UV laser-drilled through the graphite/adhesive stack and filled with copper to provide the chip with electrical connections as well as offering a low thermal resistance vertical path for the dissipated heat. Because the chips are not in direct contact with the graphite sheets (there is an adhesive layer in-

between), the density of micro vias should be sufficient to transfer the dissipated heat from the chip into graphite with low thermal resistance. In practice, vias with 240  $\mu\text{m}$  diameter and 390  $\mu\text{m}$  pitch are selected, as they according to the manufacturing capability.

The combination of a vertical thermal path, offered by the vias, and a horizontal one with graphite sheets results in a more efficient heat spreading to extract the heat as close to the chip as possible. Because of its spreading effect, it is expected that graphite has an effect of thermal coupling between chips in a multi-chips package.

Pyrolytic graphite sheets (PGS: Panasonic EYG-S091205 [5]) of 50  $\mu\text{m}$  thickness (1300 W/(m.K) XY & 15 W/(m.K) Z) are chosen to be embedded in the PCB. Two PGS are stacked with three adhesive layers (0.22 W/(m.K) with a thickness of 25  $\mu\text{m}$  (DuPont Pyralux LF0100) as shown in Figure 2. The two diodes are SiC chips with a size of 3.1 x 2.86 x 0.24  $\text{mm}^3$ . The heat spreading area (graphite area) is 20 x 30  $\text{mm}^2$ . The distance between the centers of the two diodes is 10 mm (Figure 3). The total thickness of the PCB is 0.8 mm.

PCB package samples with two embedded SiC dies and

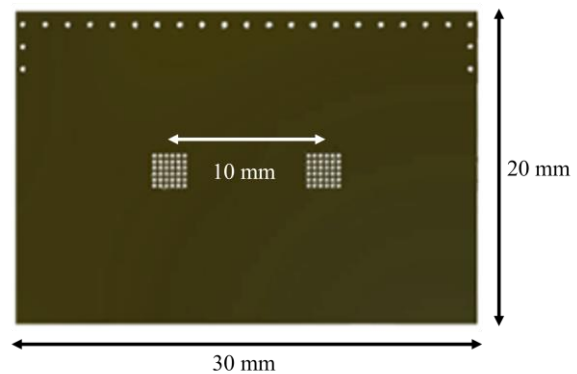


Figure 3: Spreading area at back side of the PCB.

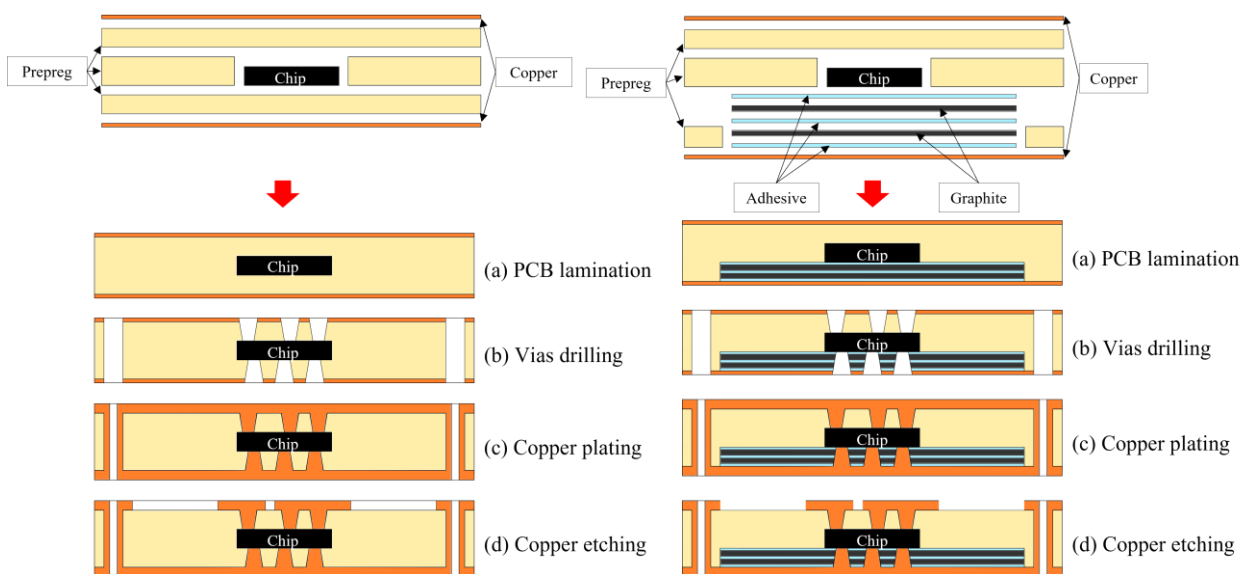
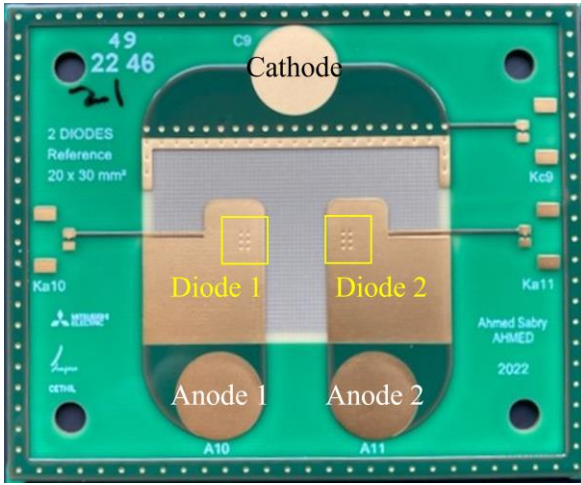
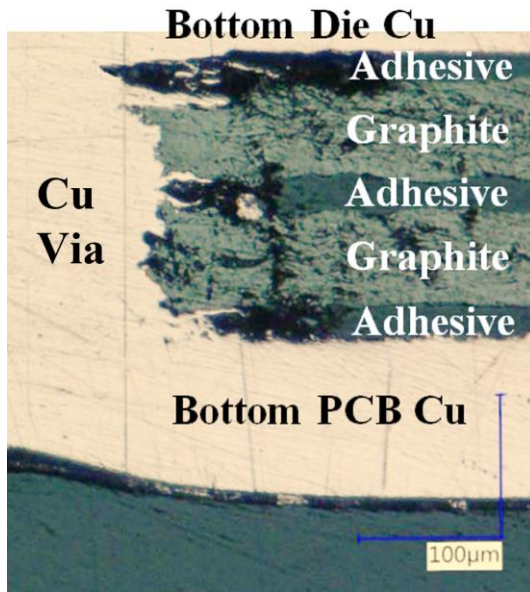


Figure 2: PCB manufacturing process of a classical stack (left) compared to PCB stack with embedded graphite heat spreaders (right).



**Figure 4:** Fabricated dual-diode PCB sample. The PCB size is 46 x 46 mm<sup>2</sup>; the graphite insert is 20 x 30 mm<sup>2</sup> and the distance between the center of both chips is 10 mm.



**Figure 5:** Cross-section of a PCB sample with graphite showing copper via through graphite/adhesive stack.

graphite are successfully fabricated (Figure 4).

Figure 5 shows a cross section through a micro via showing the good contact between copper vias (vertical thermal path) and graphite sheets (lateral thermal path) which is a key point to spread the heat.

### 3 Test setup for thermal measurements

The objective of these measurements is to quantify the thermal resistance of the PCB package from the junction temperature of the chips to the reference temperature (inlet temperature of a cold plate). Thermal impedance ( $Z_{th}$ ) is the difference between chip junction temperature ( $T_j$ ) at certain time during heating and a reference temperature

( $T_r$ ) divided by the dissipated power ( $P$ ) as shown in equation (1).

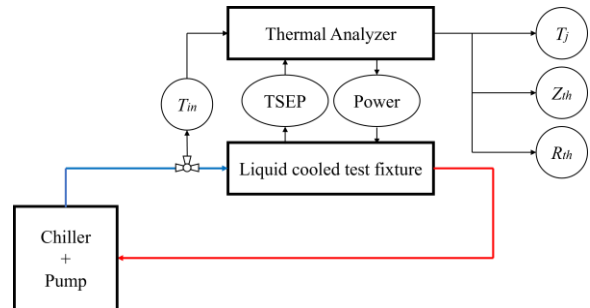
$$Z_{th}(t) = \frac{T_j(t) - T_r}{P} \quad (1)$$

In steady state, the  $Z_{th}$  value becomes equal to the thermal resistance between the junction and the reference which is called junction-to-ambient thermal resistance ( $R_{thJA}$ ). In this study, the reference or the ambient refers to the inlet cooling water.

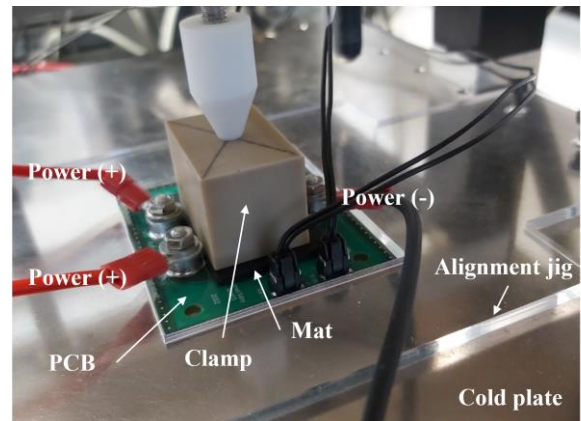
The thermal impedance measurement is performed using a thermal analyzer (AnalysisTech Phase 12 [6]). This system automatically injects a given power level in the tested device to force it to heat-up, and then monitors a Temperature-Sensitive Electrical Parameter (TSEP, here forward voltage drop of the diode) value during the cooling down phase.

The system is composed of the Phase 12 thermal analyzer, a liquid-cooled test fixture [7], and a recirculating chiller (National Lab GUPCPR020.03-NED [8]). In addition, a device calibration oven is used for the calibration of the semiconductor devices. Figure 6 shows a schematic of the thermal experimental setup.

$Z_{th}$  measurements are performed on the PCB samples with and without graphite heat spreader. First, the PCB is placed in a calibration oven to measure the relation between the forward voltage drop (using a small biasing current of 5 mA) and the junction temperature ( $T_j$ ). After



**Figure 6:** Schematic of thermal impedance experimental setup.



**Figure 7:** PCB sample clamped on the liquid-cooled test fixture of the thermal impedance experimental setup.

that, the PCB sample is clamped on a cold plate with a Thermal Interface Material (TIM: Sil-Pad®1500ST [9]) and a clamping pressure of 1.8 bar at the TIM level (**Figure 7**). An elastomeric mat (Viton) and a rigid PEEK block are used for homogenous distribution of the pressure on the PCB sample. An alignment jig fixed on the cold plate ensures all samples are tested at the same position on the cold plate to improve repeatability. Connectors are soldered on the PCB sample terminals to facilitate the electrical connection to power supply. The cold plate is cooled by water with an inlet temperature of 23°C, taken as the  $T_r$  for thermal impedance and thermal resistance calculation. The  $Z_{th}$  curve is obtained for each diode when the power is applied to only one diode.

The accuracy of measurements is  $\pm 0.5^\circ\text{C}$  for  $T_j$  measurements and  $\pm 0.5^\circ\text{C}$  for the “T-type” thermocouple that measures the water inlet temperature of the cold plate [10]. Also, some more uncertainties are introduced by the calibration curve of the die: calibrating the same SiC chip several times results in an estimated variation of  $\pm 1.7^\circ\text{C}$  in  $T_j$  due to calibration. The lower the  $T_j$ , i.e. a lower temperature difference ( $T_j - T_r$ ), the lower the accuracy of  $R_{thJA}$  measurement, so injected power is adjusted to achieve a  $T_j$  of around 70°C. Other sources of error (estimation of the dissipated power, etc.) are considered negligible here. As a result, the accuracy of the  $R_{thJA}$  measurements is predicted to be around  $\pm 6\%$  (or a total  $\pm 2.7^\circ\text{C}$  accuracy) for a temperature difference ( $T_j - T_r$ ) of 47 °C (assuming  $T_j = 70^\circ\text{C}$ ).

## 4 Modelling

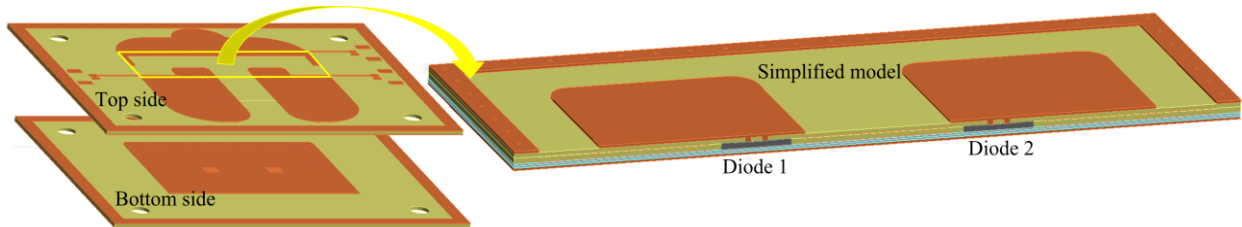
Transient thermal FEM simulations of both PCB variants (with and without graphite heat spreader) are performed using Ansys mechanical. Only half of the spreading area (graphite area 20x30 mm<sup>2</sup>) of the PCB is considered to limit the computational power with some simplifications to top side copper tacks as shown in **Figure 8**. **Table 1** shows the material properties used in the simulations.

**Table 1:** Material properties.

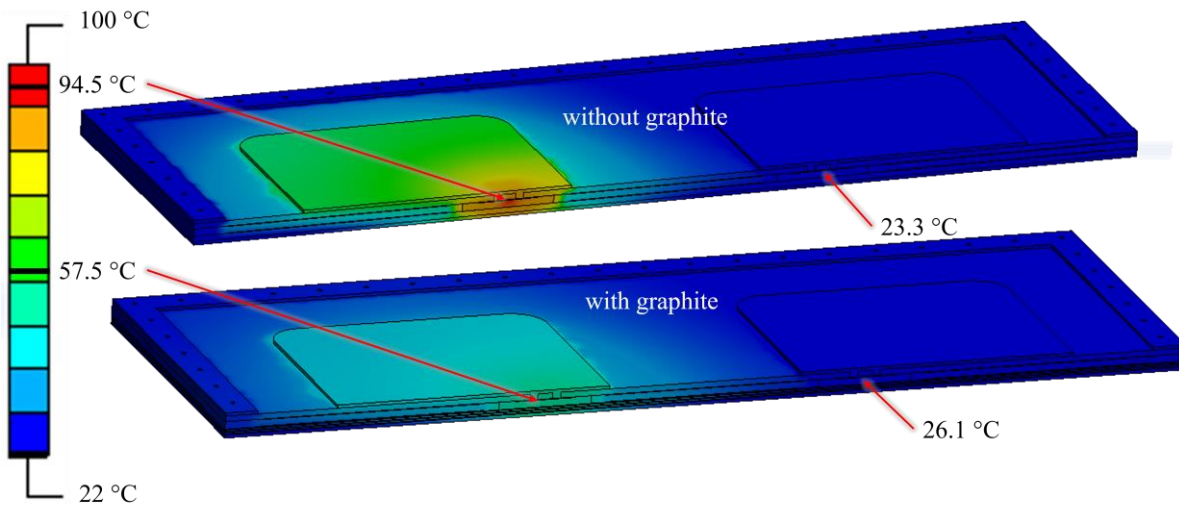
Material	Thermal conductivity (W/(m.K))	Specific heat (J/(kg.K))	Density (kg/m <sup>3</sup> )
Copper	385	385	8933
FR4	0.3	1150	1850
Graphite	1300 XY – 15 Z	850	1500
Adhesive	0.22	1926	1100
SiC	300	690	3210

**Table 2:** Boundary conditions.

Location	Type	Value
SiC chip	Internal heat generation	16 W
PCB top	Heat transfer coefficient	10 W/(m <sup>2</sup> .K)
PCB bottom	Heat transfer coefficient	6000 W/(m <sup>2</sup> .K)



**Figure 8:** CAD model of the dual-diode PCB package.



**Figure 9:** Temperature contours of showing the impact of embedding graphite on junction temperature.

The boundary conditions are set according to the experimental measurements. A heat transfer coefficient ( $h$ ) is assigned on the bottom side of the PCB to represent the behaviour of the TIM and the cold plate of the experimental test. This heat transfer coefficient is unknown. In order to identify it, a test is performed on the reference PCB sample (without graphite) and a  $RthJA$  is obtained. Then, the heat transfer coefficient is adjusted in the simulations so as to achieve the same  $RthJA$  value. This value of  $h$  allowing to achieve the same  $RthJA$  in simulation and experiment for the samples without graphite is  $6000 \text{ W}/(\text{m}^2 \text{ K})$ . it is then used for the FEM simulations with the PCB sample with graphite.

The applied power on the SiC chips is  $16 \text{ W}$  (considering an internal heat generation over the size of anode pad, so as not to impose any specific initial direction for the heat flux). Natural convection ( $h=10 \text{ W}/(\text{m}^2 \cdot \text{K})$ ) is assigned on the top side of the PCB. **Table 2** shows the boundary conditions applied in FEM simulations.

## 5 Results and discussion

### 5.1 $RthJA$ and thermal coupling

**Figure 9** shows the impact of embedding graphite on the maximum junction temperature in a dual-diodes PCB

stack when applying  $16 \text{ W}$  power loss on the first diode (D1) only and leaving the second diode (D2) without assigning any power loss.

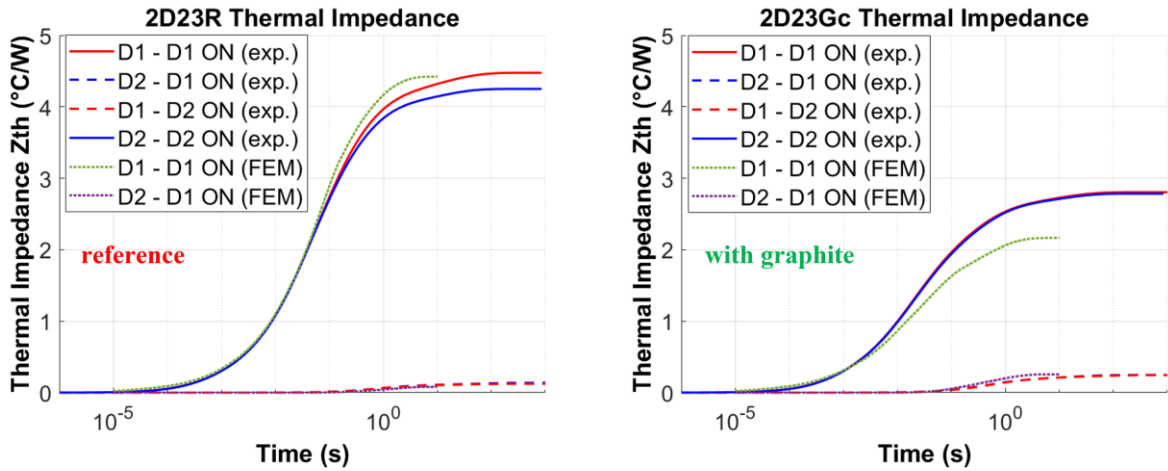
The maximum  $T_j$  of D1 (ON) drops from  $94.5 \text{ }^\circ\text{C}$  in the reference PCB sample down to  $57.5 \text{ }^\circ\text{C}$  in the PCB sample with graphite due to the better heat spreading achieved by graphite. At the same time, the  $T_j$  of D2 (OFF) increases by  $2.8 \text{ }^\circ\text{C}$  (from  $23.3 \text{ }^\circ\text{C}$  in the reference PCB sample up to  $26.1 \text{ }^\circ\text{C}$  in the PCB sample with graphite) due to the increase in the thermal coupling between the two diodes caused by graphite.

Embedding graphite heat spreader results not only in a significant reduction in  $RthJA$ , but also some increase in the thermal coupling between the two diodes.

The thermal coupling percentage can be defined by the following equation:

$$\text{Thermal coupling \%} = 100 \times \frac{RthJA_{D2-OFF}}{RthJA_{D1-ON}} \quad (2)$$

Where  $RthJA_{D1-ON}$  corresponds to the thermal resistance of diode D1 when it dissipates power, while  $RthJA_{D2-OFF}$  corresponds to the coupling thermal resistance for diode D2 (that is, the thermal resistance calculated using (1) considering the junction temperature of D2 and the power dissipated by D1).



**Figure 10:** Thermal impedance curves comparison. “Exp”: experimental results; “FEM”: finite elements (Ansys Mechanical) simulation results. D1/D2 correspond to diodes 1 and 2 in Figure 2; “DX – DX ON” correspond to “self” thermal impedances, while “DX – DY ON” correspond to coupling impedances. Due to the symmetry in FEM model, only the case when diode 1 is ON is considered for coupling impedance, since the other case is identical.

**Table 3:** Thermal coupling percentage by experiment and FEM simulations.

Method	PCB variant	D1-ON & D2-OFF		D1-OFF & D2-ON		Thermal coupling	
		$RthJA_{D1}$ ( $^\circ\text{C}/\text{W}$ )	$RthJA_{D2}$ ( $^\circ\text{C}/\text{W}$ )	$RthJA_{D2}$ ( $^\circ\text{C}/\text{W}$ )	$RthJA_{D1}$ ( $^\circ\text{C}/\text{W}$ )	D1-ON	D2-ON
Experiment	Without graphite	4.48	0.137	4.25	0.125	3.06 %	2.94 %
	With graphite	2.8	0.248	2.79	0.245	8.86 %	8.78 %
FEM	Without graphite	4.42	0.082	4.42	0.082	1.85 %	1.85 %
	With graphite	2.16	0.256	2.16	0.256	11.85 %	11.85 %

**Figure 10** shows the thermal impedance measurements of reference PCB sample (without graphite) and the PCB sample with graphite. The measurement of the thermal impedance is taken for each diode when the power is applied to only one diode (ON) as presented in the figure. Thermal impedance curves are compared to those obtained by transient FEM simulations. **Table 3** shows the values of  $R_{thJA}$  of the two diodes when applying the power to only one diode for both PCB samples with and without graphite. The experimental values are compared to those obtained from FEM transient simulations.

The  $R_{thJA}$  of the first diode (ON) is predicted by FEM simulations to be reduced by 51 % (from 4.42 °C/W in reference sample to 2.15 °C/W with graphite). The cross-coupling  $R_{thJA}$  is increased from 0.082 °C/W in the reference sample to 0.256 °C/W in with graphite due to the heat spreading effect caused by graphite. Regarding experimental results, the  $R_{thJA}$  of the first diode reduces from 4.48 °C/W down to 2.8 °C/W. This is corresponding to a 38 % reduction in  $R_{thJA}$ . The cross-coupling increases from 0.137 °C/W to 0.248 °C/W. When applying the power on the second diode (ON) instead of the first diode (OFF), the reduction achieved in  $R_{thJA}$  is 34%. In theory, both diodes should have the same thermal resistance, because of the symmetry in the sample. However, this difference remains within the expected accuracy for the measurements.

The percentages of the thermal coupling in reference PCB sample and the sample with graphite show a 3-fold increase in thermal coupling (from 2.94 % in reference sample to 8.87 % with graphite) due to graphite heat spreading effect.

Using simulations, this coupling effect was even expected to be stronger with the 6-fold increase in thermal coupling (from 1.85 % in reference sample to 11.85 % with graphite) thanks to the graphite heat spreading effect.

This increase in the thermal coupling gives an idea of the effectiveness of the heat spreading of the embedded graphite sheets despite the distance between the two di-

odes (10 mm between the centres of the two diodes). However, in some applications with multichip packaging, thermal coupling can be undesirable where the heat spreading of each chip needs to be separated from each others. This can be achieved by embedding separate graphite sheets for each chip instead of sharing the same graphite sheets, which increase the thermal coupling.

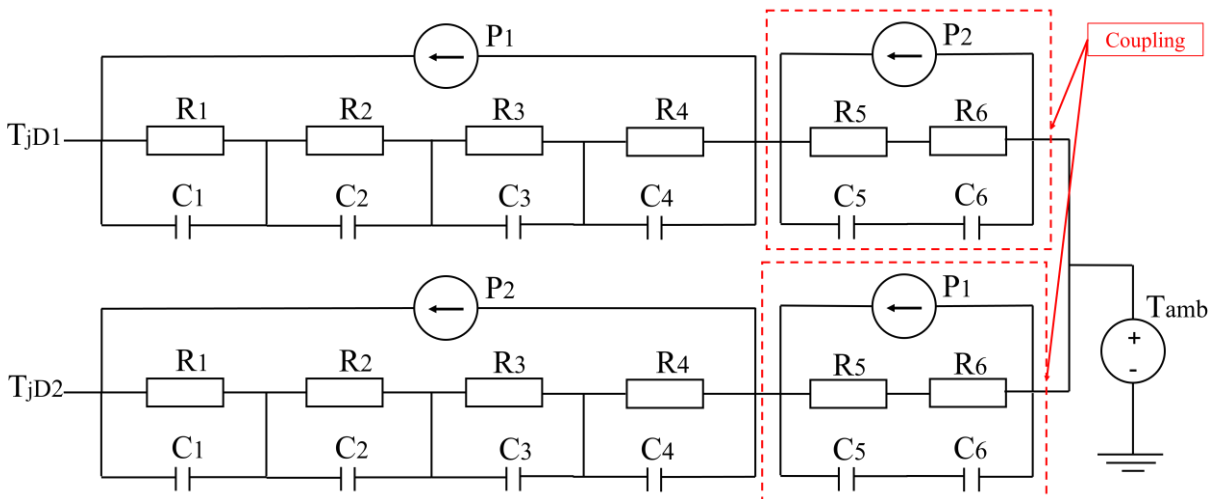
This difference in the simulated and measured thermal couplings is a consequence to the difference in  $R_{thJA}$  values between measurements and simulations. This difference means that all effects are not properly modelled (the characteristics of the graphite sheets may differ from their specified values, the various interfaces are not ideal in reality,...). In addition, the accuracy of the  $R_{thJA}$  measurements is considerably lower for the cross-coupling values: as shown above, the accuracy of the  $R_{thJA}$  measurements decreases significantly when  $(T_j - T_r)$  is low (which is the case when measuring the thermal impedance of a diode on OFF-state, for which temperature rises only a few degrees as a result of the cross-coupling).

## 5.2 TCEM generation

In order to describe the transient thermal behaviour of the thermal coupling between the two diodes, a TCEM (Thermal Equivalent Circuit Model) is generated. This model takes the form of a series of R-C cells (Resistance-Capacitance) which are represented in a Foster model. In such model, the temperatures are equivalent to voltages and the heat fluxes are equivalent to currents, which makes it easier to be implemented in an electrical circuit simulator.

The generation of this TCEM is based on the work described in [11], where an automatic generation of a thermal model for PCB-based power electronics is accomplished.

**Figure 11** shows the Foster model representation of the  $R_i-C_i$  cells where the index  $i$  represents the cell number. ( $i=1, 2, 3, 4, 5, 6$ ). **Table 4** shows the values of R-C cells obtained by measurements and FEM transient simulations data (red shaded rows show the values of thermal cou-



**Figure 11:** The generated TCEM (red dashed contours represent the values of thermal coupling).

**Table 4:** R-C cells values (red shaded rows show the values of thermal coupling).

i	Measurements				FEM simulations			
	Without graphite		With graphite		Without graphite		With graphite	
	R (°C/W)	C (W.s/°C)	R (°C/W)	C (W.s/°C)	R (°C/W)	C (W.s/°C)	R (°C/W)	C (W.s/°C)
1	0.518	0.003	0.446	0.003	0.235	0.002	0.209	0.0015
2	1.863	0.018	1.2	0.0161	0.745	0.0102	0.597	0.01
3	1.631	0.183	0.867	0.266	2.3	0.0304	0.852	0.0554
4	0.443	17.81	0.283	20.48	1.13	0.575	0.502	1.219
5	0.095	8.9	0.165	2.748	0.044	24.98	0.121	2.064
6	0.04	853.2	0.081	153.3	0.038	48.19	0.134	7.81

pling). The values are presented for the reference sample without graphite and the sample with graphite. Please that the values of the R-C cells are the results of identifications procedure and models can not be compared on a cell-by-cell basis.

## 6 Conclusion

This paper presents the impact of embedding graphite heat spreader in a PCB-based package on the thermal coupling between the embedded double-diode. The embedded graphite heat spreaders reduce the  $R_{thJA}$  by 38 % experimentally and causes a 3-fold increase in the thermal coupling experimentally compared to 6-fold as predicted by FEM simulations. This can help balancing the junction temperatures of a multichip PCB package. In addition, a TCEM model is generated in order to describe the transient thermal behaviour of the embedded diodes.

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