



**HAL**  
open science

## Automatic Generation of Thermal Models for PCB-based Power Electronics

Bahaeddine Ben Hamed, Ahmed Sabry Eltaher Ahmed, Guillaume Lefevre,  
Rémi Perrin, Guillaume Regnat, Cyril Buttay, Jacques Jay

► **To cite this version:**

Bahaeddine Ben Hamed, Ahmed Sabry Eltaher Ahmed, Guillaume Lefevre, Rémi Perrin, Guillaume Regnat, et al.. Automatic Generation of Thermal Models for PCB-based Power Electronics. Conference on Integrated Power Systems (CIPS 2024), VDE, Mar 2024, Dusseldorf, Germany. hal-04534359

**HAL Id: hal-04534359**

**<https://hal.science/hal-04534359>**

Submitted on 5 Apr 2024

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

# Automatic Generation of Thermal Models for PCB-based Power Electronics

Bahaeddine Ben Hamed\*

Ahmed Sabry Eltahir Ahmed

Guillaume Regnat, Rémi Perrin, Guillaume Lefèvre

Mitsubishi Electric R&D Centre Europe

1 Allée de Beaulieu, 35708 Rennes, France

Email\*: B.BenHamed@fr.mercede.mee.com

Cyril Buttay

CNRS, INSA-Lyon

École Centrale de Lyon

Université Claude Bernard

Lyon 1, Ampère, UMR 5005

69621 Villeurbanne, France

Jacques Jay

INSA Lyon, CNRS,

CETHIL, UMR 5008

69621 Villeurbanne, France

**Abstract**—An automated workflow transforms the board design of a power converter circuit into a thermal equivalent-circuit model (TECM) that describes the thermal behaviour of power chips. It uses commercial software (Altium, ANSYS Icepak, LTSpice), with custom code handling data transfer and model preparation in between. Some systematic simplifications are proposed to speed up the calculation. This workflow is illustrated using an example case and the results are compared with experimental measurements (thermal impedance measurement).

## I. INTRODUCTION

The design of power converters implies solving multi-physics problems: typically, electrical, magnetic, and thermal aspects must be considered, together with their couplings. Practically, because of the complexity of the problems, converter design relies heavily on hardware prototypes. Because of the cost and time involved, and because some internal parameters (currents, temperatures, etc.) are difficult to measure, a computer-based approach could be more efficient. However, generating models for a given converter design can also require a lot of time and effort [1].

In [2], we described a workflow to turn the description of a converter made using an Electronics Computer-Aided Design (eCAD) tool into a SPICE circuit model which includes layout effects. This effectively replaced hours or days of manual work with an automated process performed in minutes. Not only did that speed up model generation, but it also reduced the risks of errors and allowed the designer to iterate over design options and observe their effects.

Here, we present a similar approach aimed at generating the thermal model of a converter design. The aim is to generate a simplified Thermal-Equivalent Circuit Model (TECM) describing the thermal behaviour of the main power-dissipating components (typically the power semiconductor devices). Such a model takes the form of a series of R-C cells (typically 2 to 5) which describes the transient thermal behaviour of a given component, for time constants ranging from 10  $\mu$ s to the steady state. The cross-coupling effects (increase in temperature of a component due to the power dissipated by another) are also modelled by the same kind of R-C cells. TECM, in which temperatures are equivalent to voltages,

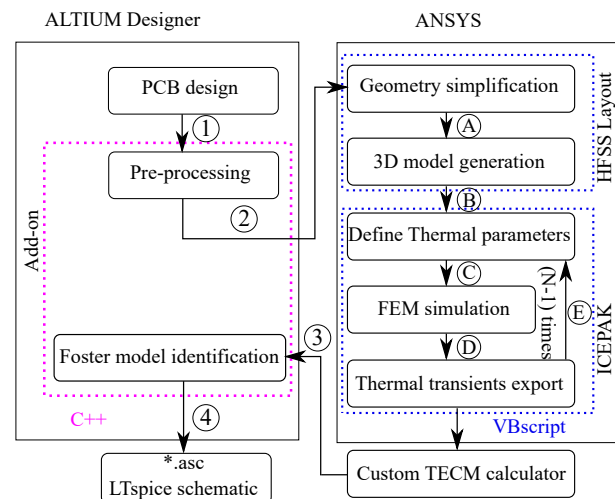


Fig. 1: Description of the toolkit workflow

and heat fluxes to currents, can be implemented in electrical circuit simulators such as SPICE, allowing for electro-thermal coupled simulations to be performed.

## II. THERMAL MODEL GENERATION

Here, we consider power converters built using Printed Circuit Board (PCB) technology, using surface-mount components or, as is the case in the examples presented below, bare semiconductor dies embedded within the PCB structure. The modelling approach described in this article uses a combination of existing software that is mature and capable of handling significant levels of complexity: Altium Designer (eCAD) for the layout description; ANSYS Icepak for the thermal Finite elements Method (FEM); LTSpice for the circuit simulation.

The workflow is summarised in Fig. 1, highlighting the different steps needed to produce a TECM schematic from a PCB layout.

### A. Data Pre-processing and export

Figure 2, details the complete data flux from the eCAD to the FEM software used for importing the geometry (Ansys suite). This flux is a combination of data that classically exists

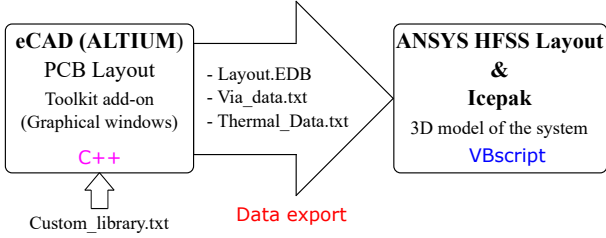


Fig. 2: Synopsis of the data transfer workflow

in the eCAD and custom information that is generated by our custom toolkit add-on (described below).

As presented in [2], the EDB format (a proprietary file format from ANSYS) is used to transfer board data. It offers the best performance (compatibility, preservation of the geometry's features, lack of errors) when compared with other file formats such as Gerber, ODB++ or IPC 2581. This EDB file format is thus selected for this work, using a free Altium plug-in provided by Ansys.

1) *Capturing the missing information:* The PCB layout description in the eCAD gives information on board size, layout, materials and each component (position, footprint). However, as eCAD aims at the design of electronic systems to provide the necessary fabrication files, it doesn't manage most of the data needed for thermal modelling. This includes materials properties ( $\lambda$ : thermal conductivity,  $C_p$ : heat capacity,  $\rho$ : density), boundary conditions (where heat is dissipated, and where and how it is removed from the PCB), and the internal structure of heat-dissipating components.

To capture some of this missing information, a custom graphical interface is implemented in the eCAD software. It is displayed when exporting the data. First, the user must pick in a list which of the components of the circuit must be considered for thermal analysis: indeed, many components in a converter have little to no power dissipation and can be safely ignored. Typically, the user will select the power devices only. Then, the cooling system must be described, considering a Thermal Interface Material (TIM) layer on the external surface of which is applied a heat transfer coefficient ( $H_{coeff}$ ). This coefficient corresponds to a convective heat exchange or to the thermal resistance of a solid heatsink. The thermal parameters and the dimensions of these two layers (TIM and heat exchange) are captured for the preparation of the system's thermal 3D model.

Regarding the third set of missing data (the internal structure, of the heat-dissipating elements), components models in eCAD are comprised of a symbol (for the schematics), a footprint (the pattern to be printed on the board to mount them on the board) and a `.step` model which is a 3D graphical representation of their external shape. The step model is used for 3D renderings of the boards but does not contain any description of the internal structure of the components or of the materials they contain. Therefore, we decided to add a fourth kind of model to the description of a component: it describes the power source dimensions, thermal parameters of the mate-

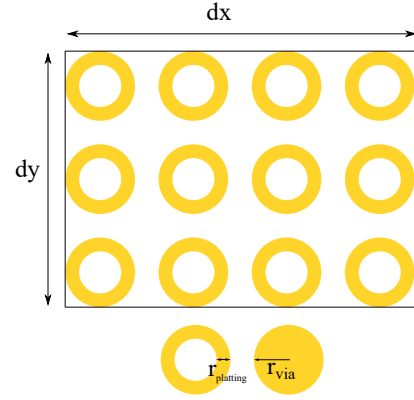


Fig. 3: Via group

rial and the heat source surface. At the moment such models simply describe rectangular parallelepipeds (as only bare dies have been used so far), but more sophisticated descriptions could be used. The data for the model are defined in a custom library as a readable text file (`Custom_library.txt`).

Once the user has entered the requested information, a file is generated (`Thermal_Data.txt`). In Ansys Icepak, another custom script reads it to create and place the correct 3D models in their corresponding positions, define the physical parameters for the used materials and set the boundary conditions.

2) *Simplifying the geometry:* The last step before actually exporting the eCAD data is to prepare some geometry simplification: in power PCBs, a large number (typically thousands) of Vias and  $\mu$ Vias are used to improve thermal conduction through the board. Such a quantity of small items dramatically increases the complexity of the 3D geometry and its associated finite elements mesh. Therefore, a simplification algorithm is implemented to identify "Via groups" (areas which contain many Vias placed along a regular pattern). When building the 3D model in the FEM tool, these Vias groups are then replaced with uniform blocks having an equivalent thermal conductivity computed according to the volume ratio method [3].

The algorithm implemented in our eCAD add-on processes the layout of the PCB design, detects the Vias and organises them according to their type (Via/ $\mu$ Via, start layer & end layer) to separate those which belong to different nets to stay away from short-circuit problems (this is required for the electrical modelling described in [2]). The algorithm then creates groups containing the maximum possible number of Vias that belong to the same type and net and computes the data needed (position and size of the equivalent blocks). Finally the thermal parameters of these equivalent blocks [3], [4] is determined by according to:

$$X_{eq} = X_{preg} \left( 1 + \frac{N \cdot (S_{cu} \cdot X_{cu} + S_{air} \cdot X_{air})}{S_{box} \cdot X_{preg}} \right) \quad (1)$$

$$with \begin{cases} X &= \lambda, C_p, \rho \\ S_{box} &= dx.dy \\ S_{cu} &= S_{via} - S_{air} \\ S_{via} &= 2\pi r_{via}^2 \\ S_{air} &= 2\pi(r_{via} - r_{plating})^2 \text{ if Via} \\ &= 0 \text{ if } \mu\text{Via} \end{cases}$$

In the end, a `Via_data.txt` file is generated, containing the results of the Via simplification algorithm. In Ansys HFSS Layout, this file is used by a custom script which replaces the Vias groups with the corresponding equivalent blocks when building the 3D model.

### B. TECM generation

1) *FEM simulation*: Once the export data export from Fig. 2 has been executed, the EDB file is opened using Ansys HFSS Layout and converted into an internal format which is useable by Ansys Icepack (Fig. 1, including the simplification of the Via groups).

The custom scripts running in Icepack then integrate the heat-dissipating components in the model and set the boundary conditions according to the information captured at the data export step. Geometry meshing is performed using the automatic tools provided by Icepak. Finally, transient thermal simulations are run, activating each of the  $N$  power sources sequentially, one at a time. For each simulation, the temperature of each of the  $N$  power sources is recorded as a function of time (regardless of whether they are active or not). This produces  $N$  transient temperature datasets for each of the  $N$  power sources.

2) *Post-processing*: These transient temperature datasets are then processed by a custom program that implements the algorithm shown in Fig. 4 to generate the corresponding Foster model (a series of parallel RC cells).

The thermal impedance of a chip can be expressed as

$$Z_{th} = \frac{T_J(t) - T_{ref}}{P(t)} \quad (2)$$

with  $T_J(t)$  the transient junction temperature of the chip,  $T_{ref}$  the (constant) reference temperature, also known as the ambient temperature, and  $P(t)$  the dissipated power waveform (in the simulations, a step starting at  $t = 0$ ). This expression can be expanded to include both self and mutual heating (cross-coupling effects):

$$\begin{aligned} Z_{th,ij}(t) &= \frac{T_{J,j}(t) - T_{ref}}{P_i(t)} \quad (3) \\ &= \sum_{i=1}^{N_k} R_{th,ij}^k \left(1 - e^{-\frac{t}{\tau_{ij}^k}}\right), \quad \tau_{ij}^k = R_{th,ij}^k C_{th,ij}^k \end{aligned} \quad (4)$$

with  $i$  the index of the heat-dissipating chip and  $j$  that of the chip for which the junction temperature is monitored (with  $i, j = 1 \dots N$ ).  $R_{th,ij}^k$  and  $C_{th,ij}^k$  are the R and C cells of the  $M$ -order foster model, with  $k = 1 \dots M$

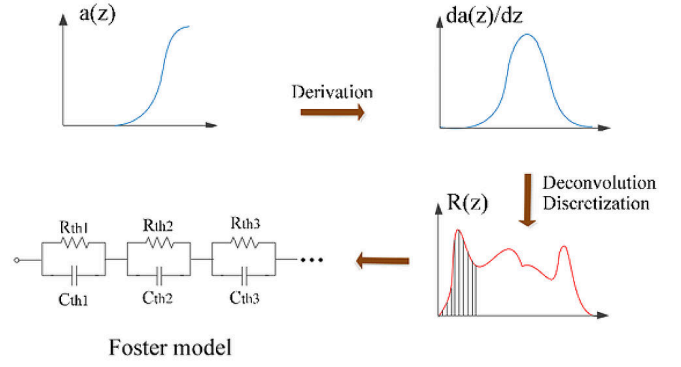


Fig. 4: Foster equivalent circuit computing algorithm [7]

Based on the method detailed in [5], [6], this thermal impedance is sampled following logarithmic time steps and differentiated. Then a Time-Constant Spectrum (TCS) can be written as in equation 5:

$$R(z) = \frac{da(z)}{dz} \otimes^{-1} w(z) \quad (5)$$

where  $\otimes^{-1}$  is the deconvolution operator and  $z = \ln(t)$ . An iterative deconvolution computing method is needed to calculate the TCS. In this case the accurate and robust iterative Bayesian deconvolution method is performed :

$$R_i^{(m+1)} = R_i^{(m)} \sum_k \frac{w_{ki} \left(\frac{da}{dz} \Big|_i\right)}{\sum_j w_{kj} R_j^{(m)}} \quad (6)$$

where,  $R_i$  is the discretized TCS,  $R_i^{(m)}$  is the estimated  $R_i$  after  $m$  iterations, and  $w_{ki} = \exp(z_k - z_i) - \exp(z_k - z_{i+1})$ .

So, a construction of the lumped Foster (i.e. identifying the  $R_{th,k}$  and  $C_{th,k}$  values) using the TCS in (6) is performed by:

$$R_{th,i} = \int_{z_1}^{z_2} R(z) dz \quad (7)$$

$$C_{th,i} = e^{z_i} / R_{th,i} \quad (8)$$

Where  $z_i$  is the index of the  $i^{\text{th}}$  peak in the  $R(z)$  spectrum and  $z_1$  and  $z_2$  are the indexes of the local minima surrounding  $R(z_i)$ .

Once all the RC pairs have been identified for each self and mutual thermal impedances, a SPICE netlist is generated, allowing for direct circuit simulation using LTSpice.

### III. APPLICATION CASES

The proposed approach is validated on two hardware prototypes for which the power semiconductor dies are embedded in the PCB: a single-chip PCB (Fig. 5) and a more representative half-bridge PCB (Fig. 6). In particular, we analyse the effect of simplifying the Via structures: both the full model (with micro-Vias, Fig. 7a) and the simplified geometry (where via groups are replaced with equivalent blocks Fig. 7b) are simulated and the results are compared with thermal impedance measurements.

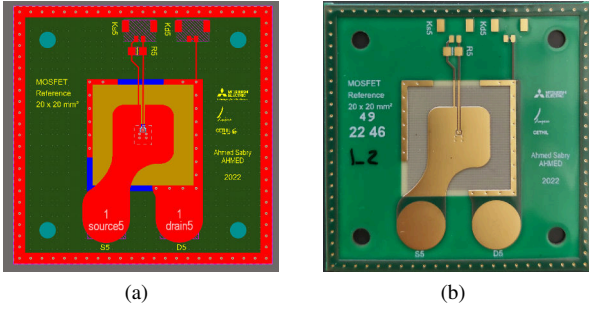


Fig. 5: Single-chip (SiC MOSFET) prototype: layout (a) and photograph (b). Sample size:  $46 \times 46 \text{ mm}^2$ .

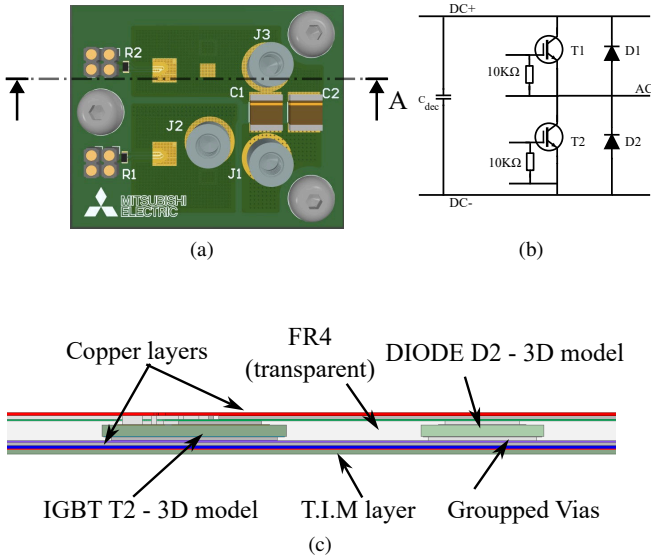


Fig. 6: Half-bridge PCB (2 IGBTs & 2 diodes): (a) upper view of the PCB, (b) circuit diagram and (c) Section view (AA) of the corresponding 3D model in Icepak.

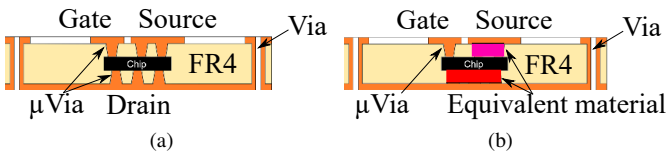


Fig. 7: The internal structure of the PCB under test (a) and the simplified Via structure (b)

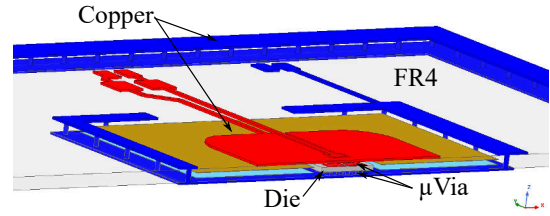


Fig. 8: 3D model of the PCB in Ansys Icepak (cutout view, without simplification of the vias).

#### A. Validation case 1: Single-chip PCB

This prototype embeds a single SiC MOSFET (Cree CMP2-1200-0080B chip) connected to the top and bottom copper layers using  $\mu$ Vias. A diagram showing the internal structure, as well as the corresponding simplifications which can be made is given in Fig. 7a. A cut-out view of the 3D model once it has been imported in the FEM simulation tool is given in Fig. 8.

In this case, because the PCB only contains one chip, a single transient thermal simulation is run, and no cross-coupling effect is computed. The experimental cooling conditions (TIM and water-cooled cold plate) are simulated by setting a bottom boundary condition for the PCB with  $H_{coeff} = 6000 \text{ W K}^{-1} \text{ m}^{-2}$ . The ambient temperature ( $T_{amb}$ ) is set to  $20^\circ\text{C}$ .

In this example, two geometries are considered: either the full geometry (including each via, used as a reference) or the simplified version which uses equivalent blocks instead of vias groups (to validate the simplification approach). In addition, two definitions are considered for the junction temperature: either the average temperature at the top surface of the chip or the maximum temperature of the chip. Both values are considered because the junction temperature estimation (used for the experimental measurement of the thermal impedance) is based on the monitoring of a Temperature-Sensitive Electrical Parameter (TSEP) of the transistor. This TSEP provides a so-called "virtual junction temperature" which is neither the area-weighted average temperature nor the maximum junction temperature [8]; it is in between, hence the use of both definitions for the simulation.

Fig. 9 shows the thermal impedance measured on the prototype using a thermal impedance analyser (Analysistech Phase 12B, plain line) and the 4 simulated thermal impedances (full geometry or simplified vias; maximum or average junction temperature).

Regarding the simulation results, the thermal impedances computed using the average temperature value (dashed lines) tend to be lower, which is to be expected: average temperatures are lower than the maximum temperature, hence the lower  $Z_{th}$  values according to 2. Also, considering a uniform equivalent block (blue lines) results in a smaller difference between impedance curves calculated using average and maximum  $T_J$  values than between curves calculated for the discrete  $\mu$ vias (red lines). This could also be expected: the equivalent blocks provide a uniform cooling over the die surface, while  $\mu$ Vias



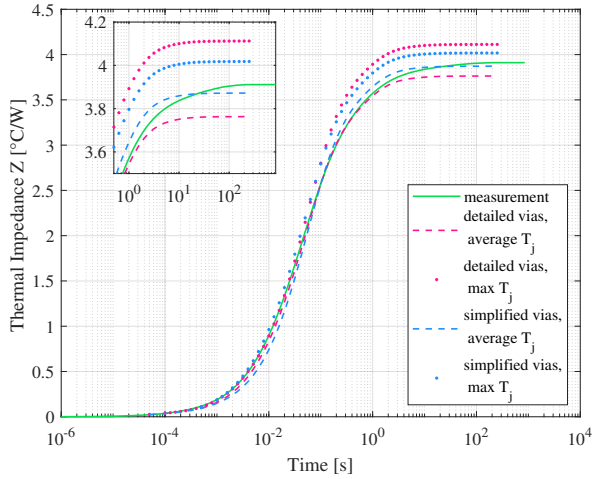


Fig. 9: Thermal impedance of the generated model, detailed Via model and measurement.

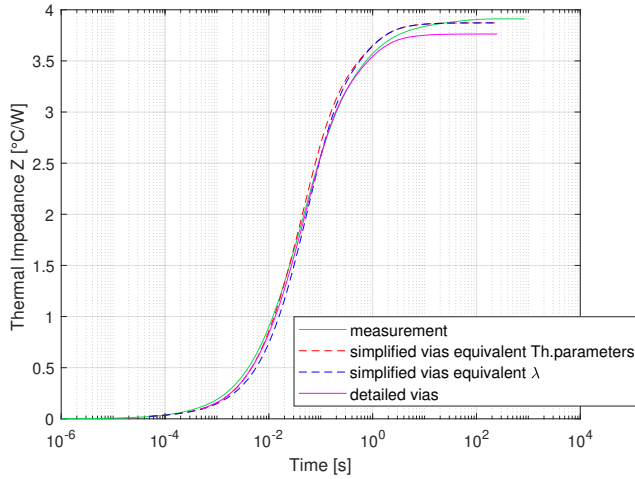


Fig. 10: Thermal impedance of the models: replacing the vias with a block with all equivalent thermal parameters ( $\lambda$ ,  $C_p$ ,  $\rho$ ); with only equivalent conductivity ( $\lambda$ ,  $C_p$  and  $\rho$  being those of copper); detailed Via model and measurement.

act like discrete heat sinks, resulting in more temperature variation over the chip surface (and more difference between the maximum and average values).

A noticeable difference between simulated and measured characteristics is the time to reach a steady state: in simulation, a steady state is reached at around 30 s, while the measurement reaches a steady state after  $\approx 200$  s. This is particularly visible in the inset from Fig. 9. This difference is a consequence of the boundary conditions used in simulation: the cold plate is represented using a simple heat-exchange coefficient, which adds no thermal mass to the structure. In reality, heat diffuses through the cold plate before reaching the cooling fluid, so the thermal dynamics of the plate add to those of the PCB, resulting in a longer time to reach a steady state. A more

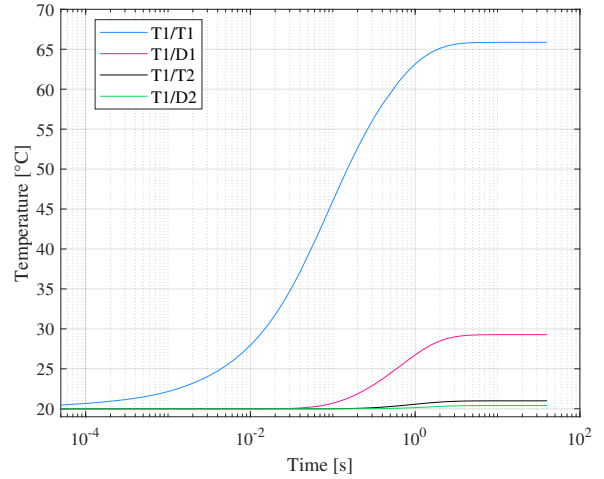


Fig. 11: Heat curve result of the conduction simulation done by Icepak for the 3D model generated by the toolkit. IGBT T1 is active heat source in this sequence ( $Power_{T1} = 20W$  and  $T_{amb} = 20^\circ C$ )

sophisticated modelling of the interface (for example including part of the cold plate in the model) would be required to achieve more realistic dynamics.

A smaller difference between simulations in Fig. 9: at around  $t = 10$  ms, the simplified models tend to predict a lower thermal resistance than detailed models (and simulation). This can be explained by the fact that for these models, only the thermal conductivity of the equivalent blocks was adjusted according to (1). In particular, the specific heat ( $C_p$ ) and density ( $\rho$ ) were considered to be those of copper. Adjusting both parameters (using a simple volume ratio between epoxy and copper in the via region) improves the fidelity of the simplified model, as can be seen in Fig. 10.

At this stage, however, the simulation using the average temperature and simplified geometry can be considered as satisfyingly close to the measurement results. This is the configuration which is used in the next validation case.

## B. Validation case 2: Multi-chip PCB

1) *Simulation:* The PCB in fig 6 is a prototype chosen to analyse the coupling effect, study the thermal model of a multi-chip system and the generation of the corresponding TECM. This half-bridge circuit consists of 4 embedded power chips (2 IGBTs and 2 diodes). The corresponding 3D model is built automatically in Ansys Icepak thanks to the the toolkit presented above. The cut view presented in Fig. 6c shows the simplified Via models and a 0.2mm TIM layer. A heat-exchange coefficient  $H_{coeff}$  of  $6000 \text{ W K}^{-1} \text{ m}^{-2}$  is applied to the bottom surface of the TIM layer.

Because the model contains 4 chips, 4 thermal transient simulations are run successively, with only one chip dissipating heat each time. As an example, Fig. 11 show the temperature profile (average  $T_j$ ) of the 4 chips simulated using Icepak when The IGBT  $T_1$  is active and the other power sources are

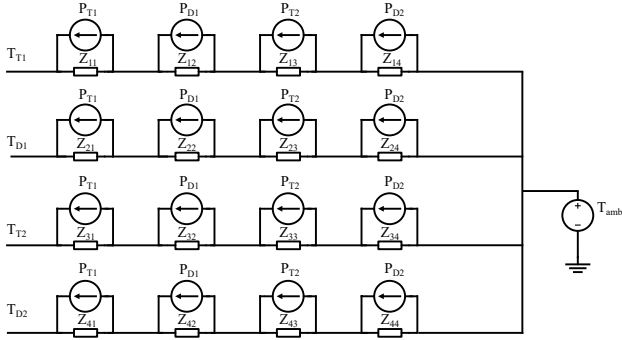


Fig. 12: TECM circuit model

off. In this case,  $T_1$  logically exhibits the largest temperature increase.  $D_1$ , which is attached to the same copper tracks as  $T_1$  also experience a significant temperature rise, despite dissipating no power.  $T_2$  and  $D_2$  which are further away show almost no temperature increase (i.e. negligible thermal coupling).

It is interesting to note that the simulation of this simplified 3D model takes 104 min on a desktop PC. Without Via simplification, the same PCB takes more than 30 hours.

The resulting TCEM model is shown in Fig. 12. For each junction temperature ( $T_{T_1}$ ,  $T_{D_1}$ ,  $T_{T_2}$ ,  $T_{D_2}$ ), 4 foster models ( $Z_{ij}$ ) are connected in series. Each model is supplied with a current source which represents the power dissipated in the corresponding components. Tab. I gives the parameters values for each of the  $Z_{ij}$  elements in Fig. 12. The order of each network (1, 2, 3 or 4 RC cells) is consistent with the intensity of the coupling: self thermal impedances have the highest order, strong couplings (e.g. between  $T_1$  and  $D_1$ ) have an order of 2, and weak couplings (e.g. between  $T_2$  and  $D_2$ ) are represented using a single RC cell. Please note that the order of each network is a result of the identification procedure, and was not set beforehand.

## 2) Comparison between simulation results and experiment:

For the measurement of the thermal impedances of the half-bridge PCB, the clamping system depicted in Fig. 13 is used: a gas cylinder applies force on the PCB through some pressure-distributing spreader; a TIM layer is placed between the sample and a cold plate. The thermal impedances of each IGBT and diode are measured with the thermal analyser using a TSEP ( $V_{CE}$  for the IGBT and  $V_F$  for the diode, both measured under a 5 mA reading current, while power is dissipated successively in each device.

The results obtained when dissipating power in  $T_1$  or  $T_2$  are presented in Fig. 14 (only the self impedances and the  $T_1/D_1$  and  $T_2/D_2$  couplings are shown). It can be seen that there is a good agreement between simulation and measurement when power is dissipated in  $T_2$  (red and green curves). However, when power is dissipated in  $T_1$  (blue and magenta curves), this is no longer the case, and the error in steady state can exceed 50% for the cross-coupling thermal impedance between  $T_2$  and  $D_2$ .

The main hypothesis for this discrepancy between simu-

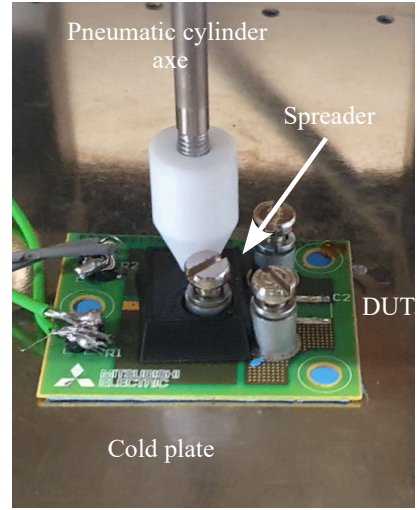


Fig. 13: Close-up on the clamping system used to press the PCB against the cold plate: a pneumatic cylinder applies a 110N force to the PCB through a plastic cap (white) and a 3D-printed spreader (black, used to balance the mechanical surface over the active parts of the PCB).

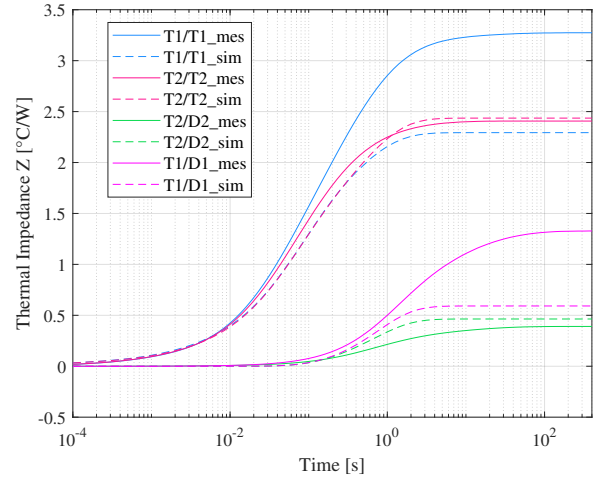


Fig. 14: Thermal impedance comparison between the simulated results and the measured values. Two sequences are presented: when  $T_1$  is active ( $T_2, D_1, D_2$  : OFF) and  $T_2$  active ( $T_1, D_1, D_2$  : OFF).  $T_1/T_1$  is the proper heating impedance and  $T_1/D_1$  is the coupling impedance of  $D_1$  when  $T_1$  is active

lation and experiment, when power is dissipated in  $T_1$ , is believed to be due to poor control of the pressure on the sample: while special care has been taken to maximise pressure uniformity (Fig. 13), this is hampered by the geometry of the board, with one of the screw connectors placed directly on top of  $D_1$ . This geometry also forces the pneumatic cylinder to be placed closer to  $T_2$  and  $D_2$  than to  $T_1$ . Furthermore, the PCB is thin, making it flexible. This shows that such PCB is very sensitive to the way it is mounted on its cooler. A rigid clamping mechanism, or a series of screws close to each other

j\i	1	2	3	4
1	$R1 = 0.079, C1 = 0.004$ $R2 = 0.288, C2 = 0.0371$ $R3 = 1.143, C3 = 0.0724$ $R4 = 0.779, C4 = 0.724$	$R1 = 0.464, C1 = 1.749$	$R1 = 0.05, C1 = 26.23$ $R2 = 2.44e^{-6}, C2 = 3.13e^6$	$R1 = 0.02, C1 = 96.24$ $R2 = 5.29e^{-4}, C2 = 6.63e^4$
2	$R1 = 0.437, C1 = 1.959$	$R1 = 0.48, C1 = 0.003$ $R2 = 1.744, C2 = 0.019$ $R3 = 1.286, C3 = 0.358$	$R1 = 0.024, C1 = 81.091$ $R2 = 2.22e^{-14}, C2 = 8.986$	$R1 = 0.014, C1 = 139.3$ $R2 = 5.1e^{-4}, C2 = 3.9e^4$
3	$R1 = 0.054, C1 = 23.71$ $R2 = 8.977e^{-7}, C2 = 3.59e^3$	$R1 = 0.024, C1 = 77.25$ $R2 = 2.221e^{-14}, C2 = 1.12e^{15}$	$R1 = 0.179, C1 = 0.010$ $R2 = 1.158, C2 = 0.049$ $R3 = 1.091, C3 = 0.509$	$R1 = 0.589, C1 = 1.552$ $R2 = 0.004, C2 = 232.05$
4	$R1 = 0.021, C1 = 91.93$ $R2 = 8.1e^{-4}, C2 = 4.33e^4$	$R1 = 0.015, C1 = 152.1$	$R1 = 0.587, C1 = 1.6$ $R2 = 2.06e^{-6}, C2 = 6.32e^6$	$R1 = 0.24, C1 = 1.35$ $R2 = 0.758, C2 = 0.012$ $R3 = 1.487, C3 = 0.043$ $R4 = 1.35, C4 = 0.451$

TABLE I: Thermal impedance parameters  $Z_{i=1..4, j=1..4}$  of the model TECM presented in Fig12,  $[R] = ^\circ C/W$ ,  $[C] = J/^\circ C$

should be used to ensure that pressure is properly applied to the PCB and its TIM.

Other parameters could also degrade the agreement between simulation and experiment, but most of them would affect all components in the same way. Many small differences exist between the design of the PCB and its fabricated prototype: the dimensions of the  $\mu$ Vias (the actual shape of the  $\mu$ Vias is conical, but cylinders were considered in the simplification stage). Also, a cross-section analysis of the PCB showed a difference in the layer thicknesses of 12 % to 22 % for the copper (70  $\mu$ m and 35  $\mu$ m in the design, 61.6  $\mu$ m and 27  $\mu$ m in reality) and of 10 % for the dielectric layers.

Overall, it means that the variability in the thermal resistance of the prototypes is large. Therefore, thermal models cannot be expected to predict the actual thermal resistance with more than probably 10-20 % accuracy, unless all manufacturing parameters are very well controlled, and very good contact is achieved with the cooling system.

#### IV. CONCLUSION

The workflow presented in section II allows to automatically go from the PCB layout of a power converter to a thermal equivalent circuit model. This model includes transient effects (thermal impedance) and cross-coupling between the devices. Although the eCAD software contains a detailed description of the PCB, it lacks data regarding the thermal behaviour, and some additional information is still required from the designer.

Commercial software (Altium, Ansys Icepak, LTSpice) is used, with custom code at the interfaces. This allows us to take advantage of the powerful features of this commercial software to process complex geometries.

Experimental validation is performed on PCBs with embedded chips. This shows that the simplification procedure which is used to speed up simulation time does not cause significant degradation in the simulation results. A half-bridge structure is used to demonstrate the capability to generate models which include cross-coupling effects. Finally, it is found that the accuracy of the modelling is limited by the variability of the measurements. In particular, the thermal resistances are very sensitive to the quality of the thermal contact between the PCB and its cooler, so special care must be given to designing proper clamping solutions.

#### REFERENCES

- [1] T. Lagier, P. Dworakowski, L. Chédot, F. Wallart, B. Lefebvre, J. Maneiro, J. Páez, p. ladoux, and C. Buttay, "How Good are the Design Tools in Power Electronics?" in *EPE'20 ECCE Europe*, Lyon (Virtual conference), France, Sep. 2020. [Online]. Available: <https://hal.archives-ouvertes.fr/hal-02968867>
- [2] B. Ben Hamed, G. Regnat, G. Lefèvre, and C. Buttay, "Automatic Model Generation for PCB-based Power Electronics," in *Conference on Integrated Power Electronics Systems (CIPS)*, Berlin, Germany, Mar. 2022. [Online]. Available: <https://hal.science/hal-03641121>
- [3] G. Regnat, P.-O. Jeannin, G. Lefèvre, J. Ewanchuk, D. Frey, S. Molloy, and J.-P. Ferrieux, "Silicon carbide power chip on chip module based on embedded die technology with paralleled dies," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2015, pp. 4913–4919, iSSN: 2329-3748.
- [4] Y. Shen, H. Wang, F. Blaabjerg, H. Zhao, and T. Long, "Thermal Modeling and Design Optimization of PCB Vias and Pads," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 882–900, Jan. 2020, conference Name: IEEE Transactions on Power Electronics.
- [5] V. Szekely and M. Rencz, "Thermal dynamics and the time constant domain," *IEEE Transactions on Components and Packaging Technologies*, vol. 23, no. 3, pp. 587–594, Sep. 2000, conference Name: IEEE Transactions on Components and Packaging Technologies.
- [6] S. Fukunaga and T. Funaki, "Transient thermal network model identification for power module packages," *Nonlinear Theory and Its Applications, IEICE*, vol. 11, no. 2, pp. 157–169, 2020. [Online]. Available: [https://www.jstage.jst.go.jp/article/nolta/11/2/11\\_157/\\_article](https://www.jstage.jst.go.jp/article/nolta/11/2/11_157/_article)
- [7] E. Deng, Y. Shen, Z. Zhao, J. Li, and Y. Huang, "The Algorithm and Software Implementation of the Thermal Transient Testing Technology Applied in High-Power Electronics," *Sensors & Transducers*, vol. 227, no. 11, p. 7, 2018.
- [8] J. Chen, E. Deng, L. Xie, X. Ying, and Y. Huang, "Investigations on Averaging Mechanisms of Virtual Junction Temperature Determined by  $V_{ce}(T)$  Method for IGBTs," *IEEE Transactions on Electron Devices*, vol. 67, no. 3, pp. 1106–1112, Mar. 2020. [Online]. Available: <https://ieeexplore.ieee.org/document/9003536/>