Interest of high frequency decoupling inductors for reducing common mode current in high speed switching cells

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Abstract

The increase of switching speeds in power converters thanks to wideband gap components has the positive aspect of reducing switching losses, but makes compliance with electromagnetic compatibility standards more complex. In this article, a method to reduce common mode currents is evaluated. This method is based on the use of a decoupling inductor set at the output of switching cell. The idea is to place a current source at the output of the cell, as it can be the case with the voltage and decoupling capacitors at the input. The first design rules of such inductor are presented, with a parallel made with decoupling capacitors. This is followed by a characterisation of the parasitic capacitances of a converter in order to carry out an electric simulation and design the decoupling inductor. Finally, experiments and simulations show a reduction of common-mode currents at high frequencies (>6MHz) with an off-the-shelf decoupling inductor. This paper therefore presents a proof of concept for the implementation of a decoupling inductor.

1 Introduction

Over the last decade, a revolution in power electronics has been underway thanks to new SiC and GaN components that offer much more interesting characteristics than conventional Si-based components [1][2][3][4][5]. These new properties offer the promise of more compact, more efficient and more reliable power electronics. Among their many advantages, their low values of parasitic capacitances (C_{oss}, C_{rss} and C_{iss}) can be especially mentioned. Such low values allow to reach switching speeds of the order of ten $V.ns^{-1}$ and thus to reduce drastically the switching losses [6][7]. On the other hand, such high dV/dt increase the common mode currents (CMC) generated via the parasitic capacitances present between the connectors and the ground [8]. Among all the existing parasitic capacitances, the most critical is the C_{mg} capacitance, which is usually represented schematically between the middle point of the switching cell and the ground. If left untreated, these CMC can disrupt the performance of the converter or even affect the performance of other devices connected to the same grid.

To avoid such an issue, the main techniques are based on the addition of a passive filter set at the input of the converter. However, those filters do not reduce the CMC generated by the converter, they only provide a low impedance path for the current in order to keep it within the converter. In this way, other devices which are connected to the same power source are protected [9]. The main drawback of those filter is mostly their volume. Another technique, used for 3 phases motors, consists of the addition of a passive filter set, this time, at the output of the inverter. The main goal is to reduce CMC passing through bearings which impact their reliability. Additionally, the passive output filter reduces also the overvoltage that can be observed at the wiring of the motor. This overvoltage is induced by the impedance mismatch between cables and motor. Like the previous solution, this technique does not reduce directly the CMC generation, and only protect the motor and cables from it [9].

In this paper, an original way to reduce common mode currents generated by switching cells based on the idea of a decoupling inductor implemented at the output of the cells is presented. A first section is dedicated to the comparison between decoupling capacitors and decoupling inductors in order to explain their interest. A second section is devoted to the presentation of the experimental setup used to highlight the interest of decoupling inductors. A third section is dedicated to the characterization of parasitic capacitances in a power converter in order to feed a LTspice simulation. This simulation should help future designers to size decoupling inductors. Finally, results from the experimental setup are presented and discussed.

2 Analogy between decoupling capacitors and decoupling inductors

The use of decoupling capacitors is becoming more and more popular in power electronics [10]. Their main role is to make the input voltage source as non-inductive as possible and limit the voltage overshoot during turn-off. In the most integrated solutions, they are generally materialized by SMD ceramic capacitors placed close to the switches.

2.1 Principle

The idea developed in this article is to present a similar approach, no longer on a decoupling capacitor at the input, but, this time, on a decoupling inductor at the output. The main idea is to allow the switching cell output to be connected to a current source to reduce CMC. In order to fully understand the utility of decoupling inductors, the interest of decoupling capacitors will first be explained. The explanation will be done with the help of figure 1 which presents a schematic of a standard Buck converter.

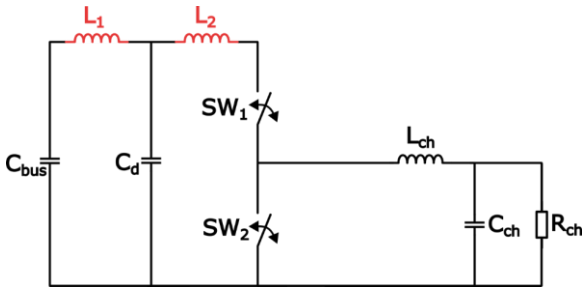


Figure 1: Buck converter with its decoupling capacitor

On this figure, there are two switches (SW_1 and SW_2), a capacitor C_{bus}, representing the chemical and film input capacitors, a capacitor C_d representing the decoupling capacitor and a load materialized by an inductor L_{ch}, a capacitor C_{ch} and a resistor R_{ch}. Moreover, two parasitic inductances L_1 and L_2 can be noticed.

An analysis of the current flowing through these parasitic inductances will now be performed. When SW_1 is closed and SW_2 is open, these two inductances store, each one, an energy proportional to the value of their inductance as well as the square of the load current I_{ch}. When SW_1 is turned-off, the current in the inductors suddenly drops to 0. The energies that were then stored in them must be evacuated. Generally, these energies can be visualized by measuring the overvoltage across C_d for L_1 and the overvoltage across SW_1 for L_2. Here, the interest of using a capacitor C_d can be understood: its presence allows the energy stored in the inductor L_1 to be evacuated by a path with very low impedance compared to the parasitic inductor L_2. Without it, all the energy stored in this inductance would be added to the energy of L_2 and would generate a much higher overvoltage across the terminals of SW_1. C_d therefore allows to "cut" the stray inductance of the switching cell into 2 distinct stray inductances L_1 and L_2.

The idea with the decoupling inductances is basically the same. The goal is to "cut" the parasitic capacitance C_{mg} existing between the output of the switching cell and the ground by adding a dedicated inductor. The explanation can be repeated with the help of Figure 2, on which the same components as before can be found, but with, this time, the capacitances C_2 and C_1 present between the output of the cell and the ground (Gnd), as well as the decoupling inductance L_d. Practically, C_1 corresponds to the parasitic capacitance between the output connexion going from the power module to the load inductor and the ground, when C_2 corresponds to the parasitic capacitance between the power module layout and the ground. Note also that C_{mg}, mentioned previously, is equal to the sum of C_1 and C_2.

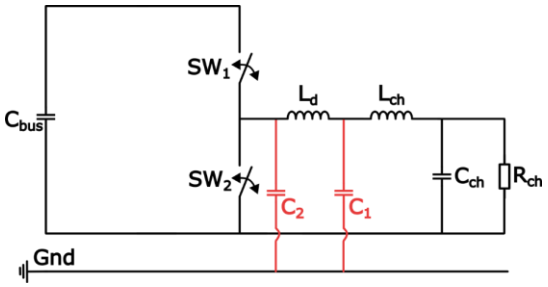


Figure 2: Buck converter with its decoupling inductor

The same explanation based on energy can be done, but this time for C_2 and C_1. When SW_2 is closed and SW_1 is open, C_1 and C_2 store, each, an energy proportional to the value of their capacitance as well as the square of the voltage across their terminals. When SW_2 is turned-off and SW_1 turned-on, the voltage across capacitors changes. A part of the energy which was then stored in them must be evacuated through Gnd. As before, the interest of L_d can be seen: its presence allows to limit the peak current produced by the capacitor C_1 at each switching, by presenting it a path with high impedance at high frequency. In that case, the value of the maximal current generated by the parasitic capacitor C_1 is reduced, thanks to the decoupling inductor.

This statement highlights that, like decoupling capacitors, it might be useful to place multiple inductors in series at the output of switching cells, each with its own bandwidth and inductance value to handle different issues. Typically, a high value inductor such as L_{ch} will always be needed at the output to smooth the load current, but the designer could also consider to use a lower value inductor placed closer to the midpoint of the switching cell, to decrease the common mode currents that flow through the parasitic capacitors.

In the following section, the limits of decoupling inductor design will be presented.

2.2 Limits

Decoupling inductors, like decoupling capacitors, are subject to significant constraints, which can make their design very challenging.

Firstly, the inductors must have the smallest practical volume in order to be positioned as close as possible to the output of the switching cell. In this way, the parasitic output capacitance can be "cut" more favourably, by reducing the value of the capacitance C_2 as much as possible regarding the value of C_1. In the case of decoupling capacitors, SMD ceramic capacitor technology is generally preferred for this reason.

Secondly, constraints linked to the load current make their design complex. Unlike decoupling capacitors, decoupling inductors are placed in series with the load and not in parallel in the circuit. The decoupling inductor must therefore be able to carry a high RMS current without overheating and without damaging its properties. Indeed, the first obvious effect of the load current will be to increase the temperature of the inductor, but it will also have the effect of polarising the inductor at an operating point on its B(H) curve. If this operating point is too close to the saturation field of the decoupling inductor in question, its inductive behaviour will no longer be guaranteed and the common mode current passing through the parasitic capacitance C_1 will not be filtered correctly. The maximum current flowing through the inductor must therefore not be too close to the saturation current, otherwise the inductor will no longer play its role as a filter. In this case, the possible analogy with decoupling capacitors is the impact of the DC bus voltage on the capacitance value of decoupling capacitors. Most capacitors see their capacitance value drop drastically as a function of the DC voltage seen at their terminals. This is why, the capacitor technology must be carefully selected.

Thirdly, there are filtering issues to consider: the decoupling inductor must have the highest possible bandwidth value. This value needs to be compared with the limits of the EMC standards (150kHz to 30MHz). The bandwidth limit is directly linked to the value of the parallel parasitic capacitor of the decoupling inductance. Unfortunately, this value is generally inversely proportional to the number of turns of this inductor, which is itself proportional to the value of the inductance. This illustrates the difficulty to have a high value inductance with a high bandwidth.

Finally, the value of the inductance of the decoupling inductor must be chosen. If the case of the decoupling capacitor is looked first, it is shown in [10] that its design is relatively easy as its value is directly related to the parasitic inductance L_1, the switched current I_{max} and the acceptable voltage bus oscillation ΔU_{bus}. This value can be obtained with the following equation:

$$C_d = L_1 \frac{I_{max}^2}{\Delta U_{bus}^2} \quad (1)$$

The most difficult part of the design is to get the value of L_1 which is, by nature, a parasitic inductance. The most efficient way to do it is to extract it with 3D electromagnetic simulations. Concerning the decoupling inductance, it must be sized in relation to the parasitic capacitance C_1. Ideally, the impedance of the L_d/C_1 pair must have at least an inductive behaviour in the range corresponding to the EMC standard. From the cut-off frequency f_c needed for the application, the value of the decoupling inductance can be thus defined as:

$$L_d = \frac{1}{4\pi^2 f_c^2 C_1} \quad (2)$$

However, it is necessary to know the value of the parasitic capacitance C_1 in order to size L_d. And unlike the parasitic inductance L_1, it is not easy to get the value thanks to simulation software. Its value must therefore be deduced from experimental measurements. One way to measure it will be presented later in this paper.

In this section, the concept of decoupling inductor and some limitations associated with its design have been presented. In the following section, the experiment setup carried out to evaluate the benefits of using a decoupling inductor will be presented.

3 Experiment

3.1 Setup

To demonstrate the benefits of the decoupling inductor, an inverter with a capacitive leg was built. The electrical diagram can be seen in Figure 3a. This inverter is made from 2 films capacitor C of 200µF, a load inductor L of 12µH and a TAPIR switching cell presented in Figure 3b [11]. The switching frequency is set to 10kHz. The inverter output current has a triangular shape with a peak value of 38A (22Arms).

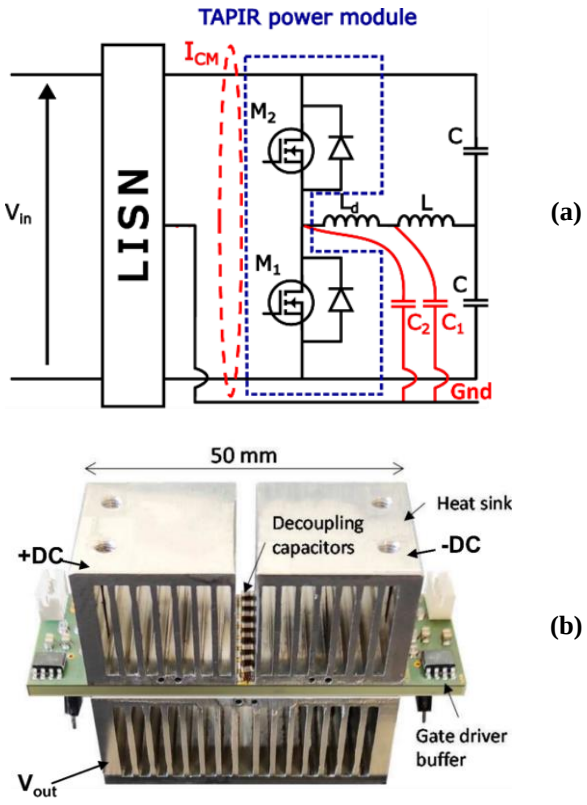
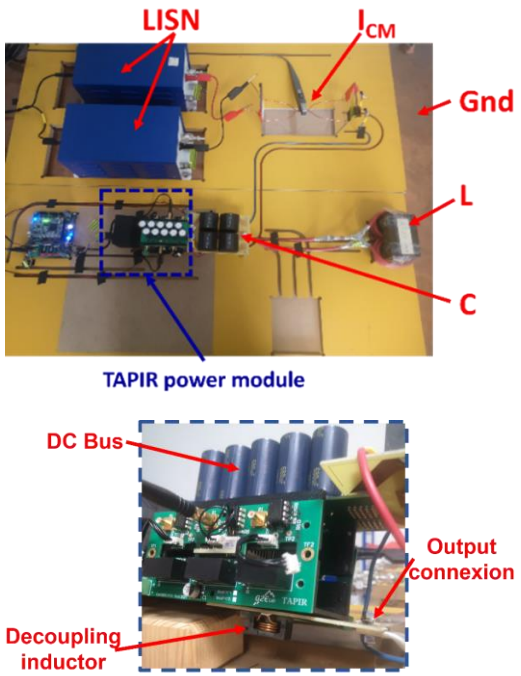


Figure 3: (a) Circuit schematic; (b) TAPIR power module [11]

Regarding the switching cell, it is composed of 2 MOSFETs embedded in a PCB. Currently; the components used are 100V-250A Silicon MOSFETs. The special feature of this switching cell is that its heat sinks act as coolers and as electrical connectors. In this way, it is possible to avoid the use of electrical insulators which are generally poor thermal conductors. The design of TAPIR cells is therefore made to improve chip cooling. However, from an EMC point of view, the fact that heat sinks are used as connectors makes them a potential major source of electromagnetic emission.

Apart from the inverter, two Line Impedance Stabilization Networks (ref: LI-325C) are added at the input to provide a known return path to CMC. CMC are measured thanks to a current prob P6021 – 60MHz. Since the results of EMC tests are very sensitive to cable positioning, a special care has been taken to create a holding board for all parts of the experiment. It enables us to obtain repeatable results. This 2 cm thick wooden board is placed on a copper plate connected directly to both LISNs. The wooden board can be seen with the converter in Figure 4a in yellow.



(a)

(b)

Figure 4: (a) Experimental setup; (b) Zoom on TAPIR power module with its decoupling inductor

To highlight the benefits of the decoupling inductor, a dedicated PCB has been produced. This PCB allows to connect or not the decoupling inductor at the output of the switching cell. During the PCB design, special care was taken not to modify the parasitic capacitance between the 2 tests so that they would be comparable. The PCB with the SMD decoupling inductor can be seen in Figure 4b at the bottom of the switching cell.

Finally, a decoupling inductor was selected. Regarding our setup specification (38Amax and 22Arms), the goal is to have an inductor with a saturation current greater than 50A, a maximum rms current value greater than 30A that would take as little space as possible. It was therefore decided to select in the Coilcraft SER series the SMD inductor corresponding to these criteria, with the highest possible inductance value (SER2011-901ML – 900nH). This SMD inductor can be seen in Figure 4b.

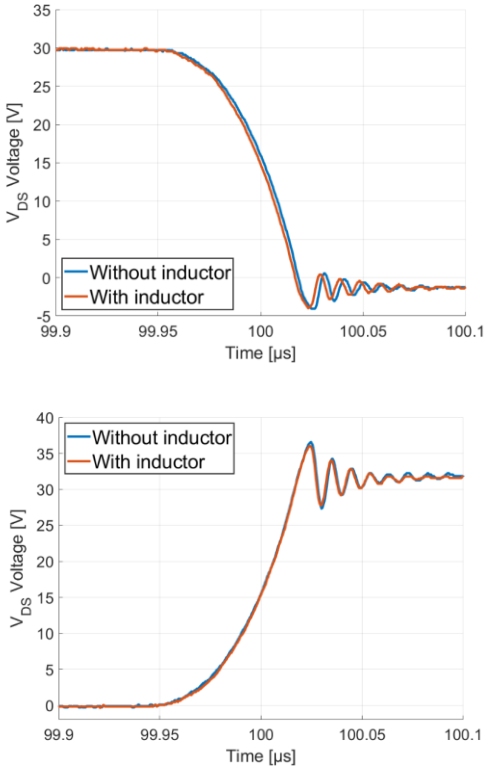
Moreover, it was mentioned earlier, that the decoupling inductor could be of interest in the case of a wide band component (GaN or SiC type). However, in this setup, TAPIR switching cells currently have Si components, which cannot have switching speeds exceeding 1 $V.ns^{-1}$. For this reason, a ceramic capacitor is added between the midpoint and the ground plane in order to artificially increase common-mode currents. Typically, the switching speeds of SiC cells can reach values of $50V.ns^{-1}$, so the value of the parasitic output capacitance is increased by a factor of 50 by estimating the parasitic capacitance at 10pF. A ceramic capacitor with a value of 470pF is therefore placed between the output of the switching cell and the ground plane.

In the following subsection, switching waveforms with and without decoupling inductance will be presented.

3.2 Waveform verification

In order to compare the impact of this inductance, its introduction into the switching cell must not modify the switching speeds, otherwise CMC spectra with and without inductance will not be compared fairly. The following figures show the voltage V_{DS} of the low-side MOSFETs with and without decoupling inductor during turn on and off (Figure 5). These curves indicate that adding a decoupling inductor does not change the switching speed of the MOSFETs. The CMC spectra can be therefor compared with each other.

In the following section, a method for characterising the parasitic capacitances will be presented.



(a)

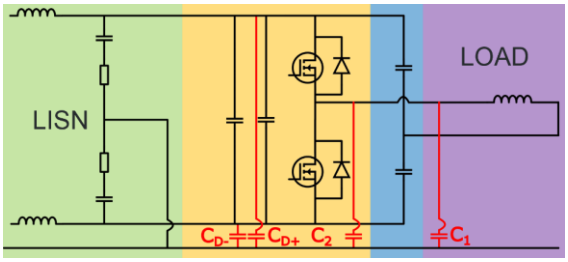
(b)

Figure 5: (a)V_{DS} voltage during turn-on with and without decoupling inductor; (b) V_{DS} voltage during turn-off with and without decoupling inductor

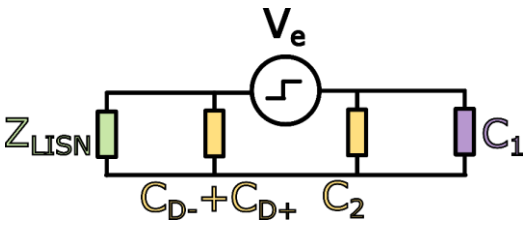
4 Parasitic capacitances extraction

Before looking at the experimental results, a method for characterising parasitic capacitances of the setup using an Impedance Analyzer (Keysight E4990A 120MHz) will be presented. As mentioned earlier, the design of the decoupling inductor is directly related to the value of the capacitance C_1, it is therefore mandatory to measure it.

Figure 6a shows the electrical circuit of the inverter with its 4 parasitic capacitances (C_1, C_2, C_{D+} and C_{D-}) and the circuit corresponding to the LISN. Figure 6b shows the equivalent common-mode electrical circuit, with the voltage generator corresponding to the evolution of the voltage across the switches.



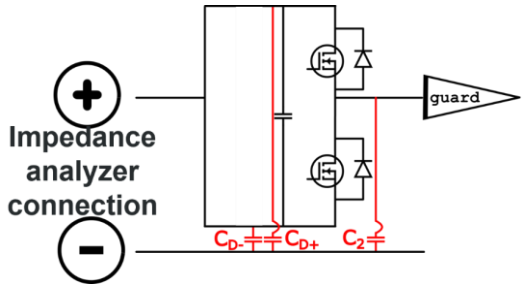
(a)



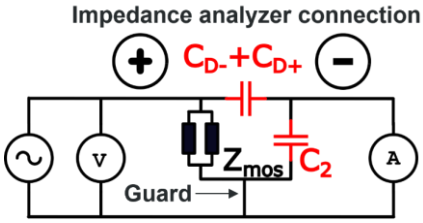
(b)

Figure 6: (a) Inverter circuit with its parasitic capacitances; (b) Equivalent circuit in common mode.

The first capacitance that is characterizable is C_1. To measure it, the load inductor should be disconnected from the circuit (leaving the cable length and position unchanged), connectors should be short-circuited together and the impedance should be measured between the copper plate (Gnd) and the short-circuited terminals. By doing this, the value obtained is equal to 485pF. This value is very close to the added 470 pF SMD capacitor.



(a)



(b)

Figure 7: (a) Connexion to measure C_{D+} and C_{D-} of the switching cell; (b) Equivalent measurement circuit.

Measurements of C_{D-}, C_{D+} and C_2 are much more challenging because of the nature of the switching cell which is quadripolar. In order to get the right value, the guarding connexion of the impedance analyser should be used. The main goal of the guarding technique is to reduce the impact of paralleled impedance. The details of the guard effects are described as follow with the help of Figure 7a and b. Figure 7a shows the connection that must be done on the setup to measure the value of C_{D+} and C_{D-}. To do so, the DC bus is short circuited and connected to one output of the impedance analyzer, the output of the switching cell is connected to the guard and the copper plate is connected to the other output of the impedance analyzer. Figure 7b shows the equivalent circuit obtained if those connexions are made. The impedance analyzer is modelized with an AC voltage source, a voltmeter and an ammeter.

In this configuration, the current coming from the voltage AC source and passing through Z_{MOS} does not flow into the ammeter thanks to the guard. This current is therefore not counted for the measurement of C_{D+} and C_{D-}. The measured impedance is therefore not impacted by Z_{MOS}. On the other side of the schematic, the current passing through C_2 should be negligeable because of the internal impedance of the ammeter which is very small. Almost no current should be going through C_2 thanks to the guard. With this short explanation the effect of the guard connexion has been highlighted. However, this kind measurement has their limits. For example, all cable lengths must be carefully reduced to avoid any impedance-related problems, and the compensation (open, short, 50Ω) should be carefully made before each measurement.

Figure 8 presents the impedance measurement of C_{D+} and C_{D-} with and without guard connexion. Results show a value of 6pF for this impedance at low frequency. Results at higher frequency have not been interpreted as measurement can be highly impacted by cable impedance. Note that the measurement without guarding is providing the sum of C_{D-}, C_{D+} and C_2. The impedance of the MOSFETs does not impact the measurement because the value of theirs C_{OSS} is much more important than C_2.

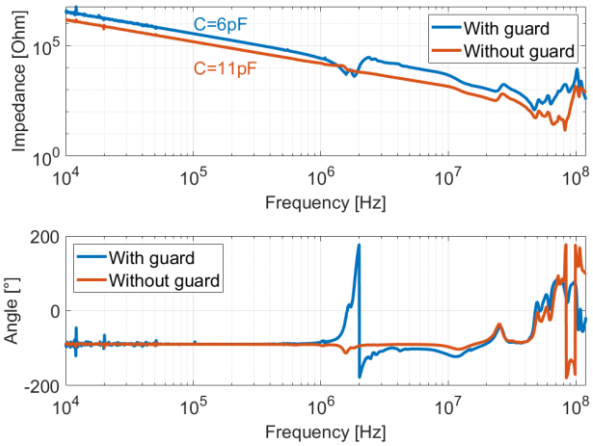


Figure 8: Impedance and phase angle vs. frequency seen from the ouput of the switching cell with and without output guarding

The same measurement has been done to get the value of C_2. This time, the impedance analyzer has been connected to the output of the switching cell and the guard connection to the DC bus (which is still short circuited). Results can be seen in Figure 9. Measurements at low frequency show a value of 5pF for C_2 which is consistent with results of Figure 8.

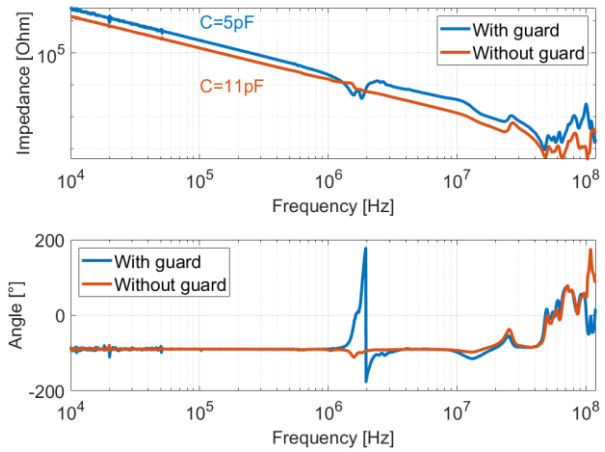


Figure 9: Impedance and phase angle vs. frequency seen from the ouput of the switching cell with and without output guarding

Finally, the capacitive leg (blue in Figure 6a) has not been characterized, and the impedance of the LISN is assumed to be 50Ω.

In this section, a method for characterising the parasitic capacitances of power converters was presented. This method was then used to measure the parasitic capacitances of our experimental device. In the next section, the impact of the decoupling inductance on the common-mode currents will be evaluated with experiments and simulations.

5 Impact of the decoupling inductance

In this section, the results of the tests will be presented. Figure 10 presents the envelope of the measured CMC spectra with and without decoupling inductor. This curve shows that adding a decoupling inductor has 2 distinct impacts.

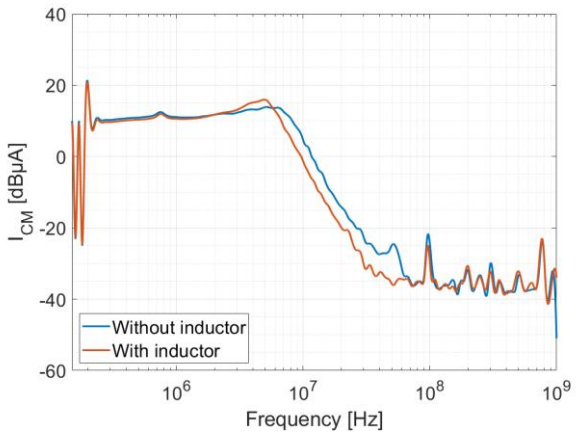


Figure 10: Envelope of CMC spectra with and without decoupling inductor

The first corresponds to a 5 dBµA reduction in common-mode current (approximately a factor of 2) at high frequency, from 6 MHZ to 60MHz in this case. Curves after 60MHz should not be interpreted because of the bandwidth of the current prob which is limited to 60 MHz (ref: P6021 Tecktronix). The second impact that can be noticed is an increase of CMC at lower frequencies, between 3MHz and 6 MHz. This increase is due to the generation of oscillations between the decoupling inductor L_d and the parasitic capacitor C_2. This is a parasitic effect analogous to the voltage bus oscillations induced by the use of decoupling capacitor at the input of switching cells. This phenomenon is highly detrimental to the implementation of the decoupling inductor as it could get CMC of the converter out from EMC standards.

The comparison with the simulation can be performed now. In the previous section, all capacitances have been characterised. The simulated electrical circuit can be seen in Figure 11. The voltage source V_e corresponds to the voltage excitation coming from the changing voltage from +DC to -DC of the middle point. According to the real switching waveforms in the setup (Figure 5), it has been modelled as a 30V squared source with a frequency of 10 kHz, and a voltage slope of ±0.5 $V.ns^{-1}$.

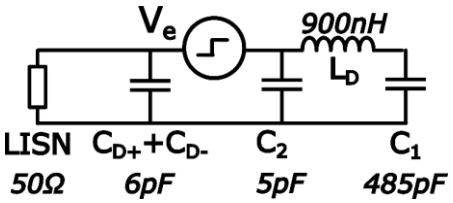


Figure 11: LTspice simulated circuit

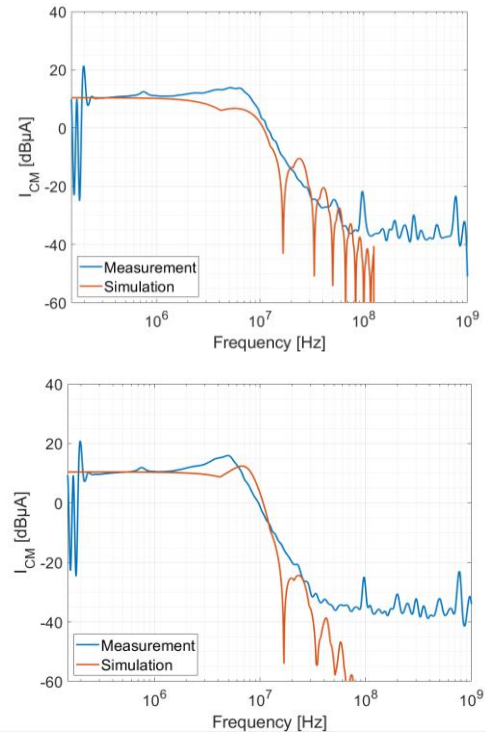


Figure 12: (a) Envelope of CMC spectra without decoupling inductor for measurement and simulation; (b) Envelope of CMC spectra with decoupling inductor for measurement and simulation

Comparison between simulations and measurements with and without decoupling inductor can be seen in Figure 12. Results indicate good modelling of low-frequency CMC. However, at higher frequency results from manipulation and simulation diverge. This comes mainly from the fact that the current prob is not well simulated in LTspice, its bandwidth being not taking into account. Frequencies

simulated after 60MHz should therefore not be interpreted. It can be also noticed that resonance frequencies are different between measurements and simulations in Figure 12b (i.e. with the decoupling inductor). The resonance frequency between the 900 nH decoupling inductor and the 485 pF C_2 capacitor should be equal to 7.6 MHz. This is what can be find for the simulation in Figure 10b, but the measurement provides a value around 5MHz. This error in modelling could come from 2 factors: the value of the output capacitance C_2 might have been not well measured, or the inductance L_d of 900 nH does not well model the real output inductance. Figure 12a can be observed to answer this question. In this figure, a resonance frequency can also be seen for the measured curve around 6 MHz. This resonance is coming from the output capacitance of 485pF and from the inductance of the output connexion of the switching cell (i.e. without the decoupling inductor). This could explain the difference between simulation and real measurement.

Nevertheless, this resonance should be reduced. For the decoupling capacitor, the reduction of DC oscillation is mainly answered by the use of a damping resistor [10]. This damping resistor can be set in series with the decoupling capacitor and has no effect on the main current path. For the decoupling inductor, this is different. No damping resistor can be set in series with it without production of lot of losses. An interesting away to reduce them could be to use inductor that have a low DC resistance, but a high AC resistance. Works to produce such inductors already exist and are mainly based to the addition of a coating made of other conductive materials such as Nickel [12]. It could be interesting to try such an inductor to reduce the resonance peak.

6 Conclusion

In this paper, the benefits of using a decoupling inductor at the output of the switching cells were studied. At first, a parallel was drawn between these inductors and decoupling capacitors that can be used at the input of switching cells to reduce voltage spikes. This parallel highlighted their numerous similarities. Then, limits of the use of such inductors were presented, in particular with regard to thermal and saturation issues which limit the volume reduction of the inductance. Initial design rules have been established.

Next, a technique for characterising the parasitic capacitances regarding the ground of a converter was presented using an impedance analyser. This technique enabled us to make measurements while avoiding issues linked to parallel impedance, in particular to the C_{oss} capacitances of MOSFETs. Results enabled us to make LTspice simulations that can be helpful to select the right decoupling inductor in the future. Finally, the results of the experiments with and without the use of decoupling inductor showed a reduction in CMC generated by the cell by 5dBµA at high frequencies. On the other hand, an increase in CMC was also observed around the resonant frequency of the decoupling inductor and the parasitic output capacitance C_2. This increase could be highly detrimental to the use of decoupling inductor. One way to reduce them has been mentioned but more investigation will have to be done.

To conclude, many things need still to be investigated to confirm the benefit of decoupling inductors, this paper corresponds only to a proof of concept. Next step will be to use such an inductor in high switching speed SiC cells. The inductance will have to be carefully sized and the CMC emission of the switching cell will have to be compared to EMC standards.

Acknowledgment

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