# Fault Analysis for a MTJ-based Spiking Neural Network

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Leonardo Miceli *, Elena Ioana Vatajelu †, Victor Champac*
* National Institute for Astrophysics, Optics and Electronics, INAOE, Mexico
† Univ. Grenoble Alpes, CNRS, Grenoble INP, TIMA, 38000 Grenoble, France

***Abstract*—Interest in Spiking Neural Networks (SNN), which mirror brain functionality, within the Artificial Intelligence (AI) domain stems from their potential for energy efficiency. Recent advancements have introduced novel synapse and neuron-implementation devices, promising further energy efficiency enhancements. However, the susceptibility of hardware-based SNNs to manufacturing defects raises concerns. This study investigates the impact of manufacturing defects on SNN performance, leveraging Magnetic Tunnel Junction (MTJ) devices for synapse and neuron implementation. Circuit-level simulations are conducted by building a basic SNN and intentionally introducing defects. Input spikes are applied to the SNN to evaluate its performance in the presence of defects. Furthermore, our investigation delves into the effects of timing alterations during integration and the synapse operation's leakage windows on defective SNNs. The results from our analysis offer valuable guidance for formulating fault models that generate high-quality test vectors.**

***Index Terms*—open defects, spiking neural network, fault analysis, magnetic tunnel junction**

## I. Introduction

Artificial Intelligence is a field of computer science that aims to perform tasks exhibiting attributes of human intelligence, such as learning and decision-making. AI-based systems use algorithms and mathematical models to process data and learn from it, thus making decisions. Carver Mead's seminal work on neuromorphic computing [1] [2] paved the way for utilizing Very-Large-Integration-Systems (VLSI) to emulate neuro-biological structures, aiming for enhanced computational efficiency and learning complexity. Based on the Von Neumann architecture, traditional computing systems face challenges such as high power consumption and limited information transfer due to the separation between memory and processing units. In response, neuromorphic computing emerges as a promising paradigm to address these limitations by introducing Spiking Neural Networks (SNNs) [3] [4]. Unlike conventional neural networks, SNNs transmit information using spikes, mirroring the communication patterns observed in the human brain.

In recent years, there has been a surge in the development of emerging silicon devices tailored for implementing synapses and neurons, leading to significant advancements in energy efficiency. These novel devices can emulate various characteristics or functions of the nervous system, rendering them invaluable for constructing artificial neural network systems. Prominent among these neuromorphic devices are Memristors [5], Phase Change Memory (PCM) [6], and Magnetic Tunnel Junctions (MTJs) [7], [8]. Spiking Neural Networks (SNNs) leveraging emerging devices for synapses and neurons can be seamlessly integrated into CMOS technology processes, albeit with additional manufacturing steps for incorporating the emerging devices. However, the fabrication process of SNN architectures may be susceptible to manufacturing defects, such as bridges and opens. These defects can arise due to the intricacies of highly reduced geometries and complex manufacturing processes [9]. Addressing such challenges is crucial to ensure the reliability and functionality of neuromorphic computing systems in practical applications.

Researchers have investigated the behavior of Spiking Neural Networks (SNNs) in the presence of defects, aiming to assess their impact on system functionality and reliability. Bishnoi et al. [10] investigated fault behaviors within the magnetic layers of Magnetic Tunnel Junctions (MTJs), providing insights into potential vulnerabilities. Vatajelu et al. [11] analyzed the reliability of functional modules composed of spintronic-based synapses. They proposed fault-tolerant training methods and performed reliability assessments on modules utilizing MTJs for neuromorphic computing. Anghel et al. [12] proposed testing strategies to verify the proper operation of neurons and synapses within SNNs. Furthermore, Vatajelu et al. [13] delved into the fault behavior within fully connected layers of neurons, focusing on "Dead Synapse Faults (DSFs)" and "Dead Neuron Faults (DNFs)." Their findings highlighted the impact of these faults on pattern recognition accuracy, emphasizing that DSFs had a non-significant effect on accuracy when affecting less than $10\%$ of the synapses. In another study [14], the focus was on defects potentially arising during the manufacturing of MTJs and their implications on neuromorphic system operation. Additionally, [15] characterized defect behaviors in SNNs based on memristors, introducing fault models such as "Slow Integration Faults (SIFs)" and "Fast Integration Faults (FIFs)," which provide insights into the diverse manifestations of defects and their impact on SNN operation. These investigations collectively contribute to the understanding of fault tolerance and reliability in SNNs, paving the way for the development of robust and resilient neuromorphic computing systems..

This work examines the influence of open defects on the performance of Spiking Neural Networks (SNNs) employing Magnetic Tunnel Junction (MTJ) devices to realize synapses and neurons. Our investigation operates at the circuit level, where SNN input stimuli are encoded temporally into spikes. Specifically, defects are injected into the SNN structure to assess their impact on network performance and functionality.

The remainder of this paper is structured as follows: Section II presents the MTJ devices and the design of bit-cells alongside their associated circuits. Section III introduces the neural network utilized for fault analysis. Section IV presents the fault

analysis conducted on the neural network under study. Section V delves into an extended fault analysis of the same neural network considering the Integrate and Leaky windows. Section VI provides a comprehensive summary of our findings and pertinent remarks. Lastly, Section VII presents the conclusions drawn from this study.

## II. MTJ AND BIT-CELL DESIGN

### A. Magnetic Junction Tunnel Devices

The MTJ device (See Fig. 1a) is composed of two plates of ferromagnetic material and a dielectric material between them called the *tunnel barrier* [7] [8]. The change in resistance is achieved by reorientating the magnetic dipoles when a current is applied. The low resistance (*RL*) state of the MTJ occurs when the magnetic orientation of the free layer (*FL*) and the fixed layer (*FX*) are in the same direction, known as the parallel state (*P*). On the other hand, the high resistance (*RH*) state of the MTJ occurs when the magnetic orientation of the FL layer is in the opposite direction to the FX layer, known as the antiparallel state (*AP*).

Figure 1b illustrates the Magnetic Tunnel Junction Spin Hall Effect (MTJ SHE) device, which is an MTJ mounted on a Heavy Metal bar (*HM*) that could be Platinum (Pt) or Tantalum (Ta). The free layer (*FL*) of the MTJ in contact with the HM generates a physical effect known as the Spin Hall Effect (SHE). This Hall effect influences the spins of the ferromagnetic material, allowing them to change orientation [16].

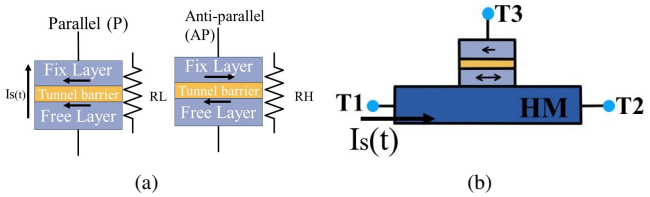



Fig. 1: Magnetic tunnel junction device.

### B. Bit-cell design

Figure 2 shows the building blocks of a bit-cell, the neuron and the potentiation circuit [17] [18] [19]. This work uses 40nm UMC CMOS technology with a supply voltage $V_{DD} = 1.1V$. The minimum channel length for the transistors is 40nm. A self-contained magnetic tunnel junction (MTJ) SPICE model is used [20]. SPICE simulations are conducted at room temperature.

The potentiation circuit generates a slow ramp signal. The magnitude of the specific voltage of the ramp used to program the bit-cell is determined by the time difference between the input and output spikes. pMOS transistor $M_{pot}$ has a channel width of 240nm and a channel length of 80nm. pMOS transistor $MPre_{pot}$ has a channel width of 240nm and a channel length of 40nm. A capacitor $C_{pot}$ of 100fF was chosen [21].

The function of the bit-cell (See Fig. 2) is to adjust the conductance of the MTJ SHE to the values required for the connections between input and output neurons. Subsequently, a current resulting from the MTJ conductance goes to the output neurons. When multiple bit-cells are present in this architecture, it is referred to as a Crossbar, which sums the currents from each connection directed towards the output neurons [17]. Table I shows the dimensions of the MTJ used in the bit-cell and the values of some important parameters. The channel width of nMOS transistors MA1 and MA2 are 108nm, the nMOS MA3 and MA4 are 108nm, and the pMOS transistor MPot channel width is 240nm. The minimum channel length allowed by the technology is used.

Figure 2 shows the neuron on the right side. At the top, there is a reference MTJ whose resistance remains constant regardless of the applied voltages or currents, and at the bottom, there is an MTJ SHE that adjusts its resistance with the incoming current. The MTJ SHE can change its magnetic orientation thanks to the current from the bit-cells [22]. Table II shows the MTJ and MTJ SHE dimensions used for the neuron. In the case of $M_{WR}$, since it has to handle a high current, it must be sized to withstand the flow of the current, as mentioned in the literature [17], [21], [23]. The channel width of nMOS transistors $M_{WR}$ and $M_{read}$ are 6$\mu$m and 180nm, respectively. The minimum channel length allowed by the technology is used.

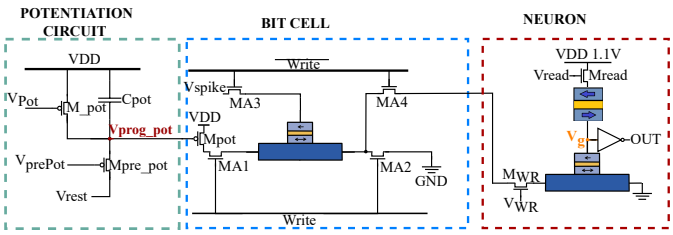



Fig. 2: Schematic circuit of the designed bit-cell, the neuron with the potentiation circuit [17], [18].

| Description | Values |
|---|---|
| Magnetic saturation $M_s$(A/m) | 1000K |
| Oxide thickness (nm) | 1 |
| Product Resistance-area ($\Omega$-$\mu m^2$) | 10 |
| Damping factor $\alpha$ | 0.0122 |
| Free layer sizes, Lm×Wm (nm) | 45×45 |
| Heavy metal $L_{SHM}$×$W_{SHM}$×$T_{SHM}$ (nm) | 60×45×5 |

TABLE I: Characteristics of the MTJ and parameters in the bit-cell.

| Description | MTJ Fix | MTJ SHE |
|---|---|---|
| Magnetic $M_s$(A/m) saturation | 750 | 1335<br>1 |
| Oxide thickness (nm) | 0.45 | 1 |
| Product resistence-area ($\Omega$-$\mu m^2$) | 2 | 710 |
| Damping factor $\alpha$ | 0.3 | 0.45 |
| Free layer sizes, Lm×Wm (nm) | 45×45 | 45×45 |
| Heavy metal $L_{SHM}$×$W_{SHM}$×$T_{SHM}$ (nm) | -<br>- | 60×45×5<br>60×45×5 |

TABLE II: Characteristics of the MTJ and MTJ SHE in the neuron.

## III. Design of the Spiking Neural Network Under Analysis

An SNN comprising four inputs (See Fig. 3) with preassigned weights has been instantiated, obviating our study's need for a learning process. This SNN operationally discerns whether the four inputs correspond to pixels of black color, generating an output spike when the criteria are met; otherwise, it remains quiescent. The SNN has undergone binarization, where weights are discretized into binary values of 0 or 1. This binarization process leverages the inherent binary states of Magnetic Tunnel Junctions (MTJs), which exhibit either high resistance (RH) or low resistance (RL). In a related work by Kheradpisheh et al. [24], they proposed a similar approach of utilizing binary weights constrained within the absolute values of 0 or 1 in SNN implementations.

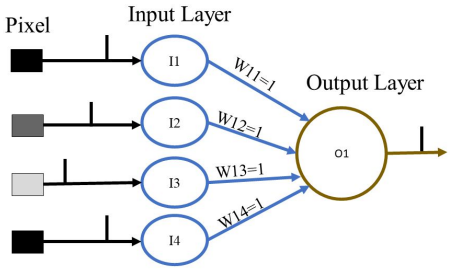



Fig. 3: Structure of the SNN under analysis.

The encoding technique of *Single-spike temporal coding* proposed by Kheradpisheh et al. [24] is adopted to represent the input data. Figure 4 illustrates the encoding scheme utilized for pixel intensities. In this framework, the encoding window is bounded by a maximum time $t_{max}$ of 10ns, and the highest intensity value ($I_{max}$) considered is 2. After the encoding process (depicted in Figure 4), resistance values are assigned to individual bit-cells. Following the notation employed in this study, an RL (low resistance) value corresponds to $W_{ij} = 1$, while an RH (high resistance) value aligns with $W_{ij} = 0$.

$$t_i = \left[ \frac{I_{\max} - I_i}{I_{\max}} t_{\max} \right] \quad (1)$$

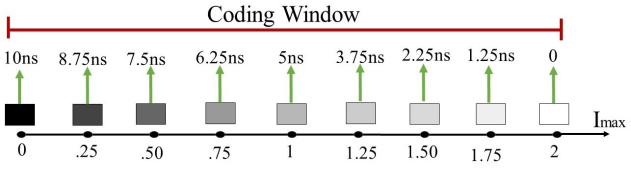



Fig. 4: Coding of the pixels intensity using Single-spike Temporal Coding.

The crossbar configuration of the SNN, showcasing potential open defect locations in the interconnections carrying synaptic currents of each bit-cell, is depicted in Figure 5. Each square labeled with a weight ($W_{ij}$) represents a distinct bit-cell. Table III shows the total accumulated synaptic current ($IM_{WR}$) across the bit-cells for various combinations of input *spikes*. The SNN architecture is tailored to produce an output spike only when all input pixels are black, signifying that all inputs are set to 1-logic.

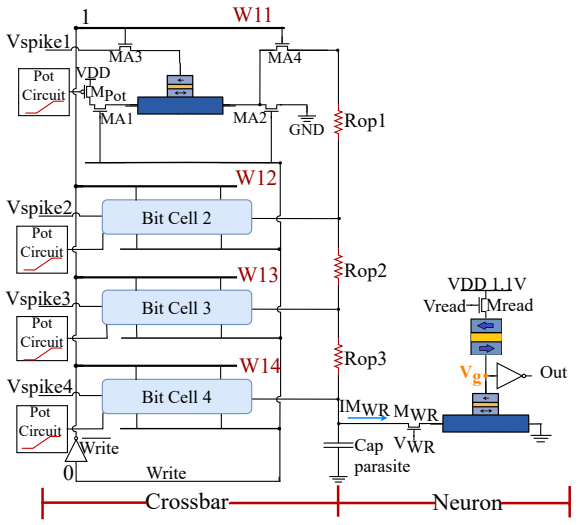



Fig. 5: Crossbar of the SNN under analysis with possible open locations.

| IN1 (*Vspike1*) | IN2 (*Vspike2*) | IN3 (*Vspike3*) | IN4 (*Vspike4*) | $IM_{WR}$ ($\mu A$) |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 27.07 |
| 1 | 1 | 0 | 0 | 54.17 |
| 1 | 1 | 1 | 0 | 81.3 |
| 1 | 1 | 1 | 1 | 108.44 |
| 0 | 0 | 0 | 0 | 0 |

TABLE III: Accumulated synaptic current from the bit-cells according to the input spikes.

## IV. Fault Analysis of Open Faults in a SNN

### A. Set-up conditions for the fault analysis of the SNN

The behavior of the Magnetic Tunnel Junction (MTJ) adheres to the principles of the Leaky Integrate-and-Fire (LIF) Neuron Model [25]. The neuron's activity is characterized by a coding window, within which a *spike* must occur to elicit a response. For the configured system, it is considered that the coding window lasts for 10ns. This window is further segmented into two distinct intervals, as illustrated in Figure 6:

The *Integrate Window* denotes the period during which the *spike* arrives, and for our system, it is fixed at 1ns [8], [17], [23]. The *Leaky Window* denotes the duration when no *spike* is received, and it is set to 9ns.

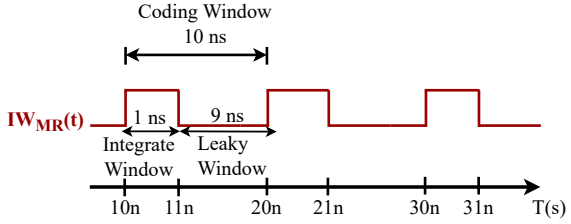
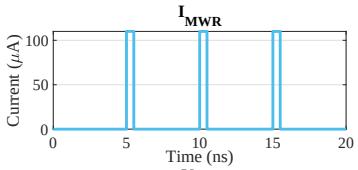


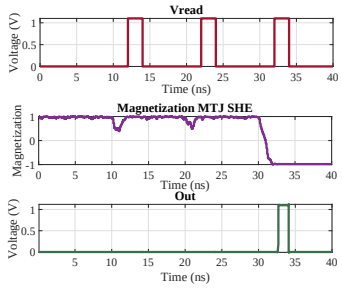

Fig. 6: Timing conditions of the Integrate Window and Leaky Window of the neuron.

### B. Fault-free behavior of the SNN

Figure 7 illustrates the performance of the fault-free crossbar (See Figure 5) under the condition where input signals are set to 1-logic (representing all 4 pixels as black). In this scenario, three write pulses are necessary to induce magnetization change, producing an output spike.

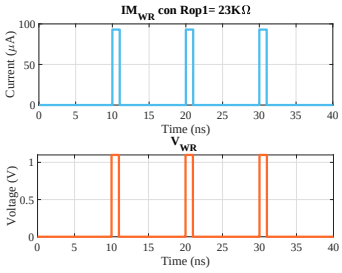



(a)

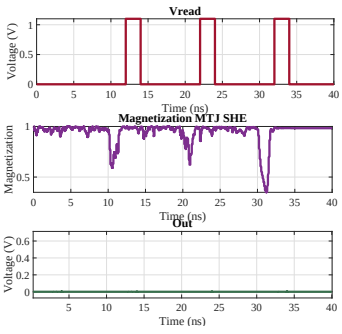



(b)

Fig. 7: Behavior of the fault-free crossbar of the SNN.




(a)




(b)

Fig. 8: Behavior of the crossbar of the SNN with open $R_{op1}$ with a resistance of 23KΩ.

### C. Behavior of the SNN with opens in the interconnection carrying the synaptic currents

Figure 8 illustrates the behavior of the crossbar with an open defect, specifically with a resistance of $R_{op1} = 23K\Omega$ (See Figure 5). Due to the open defect, the synaptic current originating from the upper bit-cell (See Figure 8a) is reduced. Consequently, the diminished current supplied to the Spin Hall Effect (SHE) of the neuron's MTJ fails to induce a complete magnetization change, resulting in the absence of a spike at the output neuron.

Figure 9 presents the accumulated synaptic current ($IM_{WR}$) plotted against the resistance value of the open defect for various open locations (See Fig. 5). It can be observed that the accumulated synaptic current diminishes with the increasing number of affected bit-cells. Consequently, lower values of minimum detectable resistance for the open defect are anticipated as more bit-cells are impacted. Table IV gives the specific values of minimum detectable resistance corresponding to three distinct open locations (See Fig. 5).

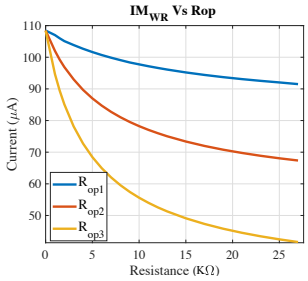



Fig. 9: $IM_{WR}$ when the input (1,1,1,1) is applied to the crossbar for different open locations.

| | Minimum detectable resistance |
|---|---|
| $Rop1$ | 16KΩ |
| $Rop2$ | 4KΩ |
| $Rop3$ | 1KΩ |

TABLE IV: Minimum detectable resistances of the opens under original conditions of the coding window.

### D. Opens into the bit-cell

Figure 10 delineates several critical open defects that might arise within the bit-cell. Notably, it has been observed that these open defects typically exhibit behavior similar to that of opens occurring within the bit lines. The minimum detectable resistance values for these open defects within the bit-cell are provided in Table V. Of particular note, open $R_{op5}$ is deemed non-detectable, while opens $R_{op6}$ and $R_{op7}$ share identical minimum detectable resistance values.

| | Minimum detectable resistance |
|---|---|
| $Rop4$ | 67KΩ |
| $Rop5$ | No detectado |
| $Rop6$ ($Rop7$) | 19KΩ |

TABLE V: Minimum detectable resistances of the opens in the bit-cells under original conditions of the coding window.

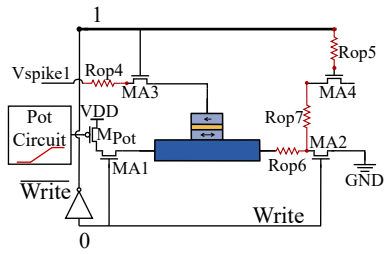


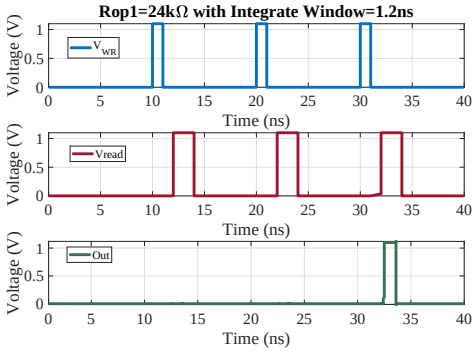

Fig. 10: Bit-cell with some open locations.

## V. Extended Fault Analysis of the Open Faults in a SNN

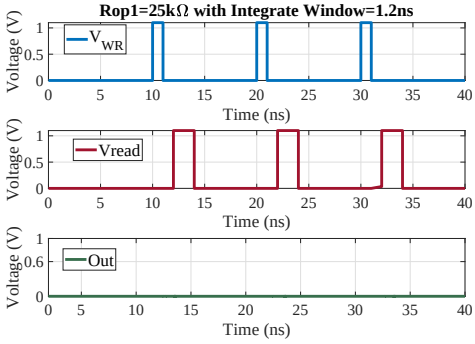
This analysis focuses on open defect occurrences within the interconnections that carry synaptic currents.

### A. Modifying the Integrate Window

The performance evaluation of the SNN in the presence of a resistive open $R_{op1}$ is conducted by adjusting the initial setup conditions of the Integrate Window depicted in Figure 6. Initially, the Integrate Window was configured with a width of 1ns, spanning from 10ns to 11ns. However, for the subsequent analysis, the Integrate Window is extended by 0.2ns, ranging from 10ns to 11.2ns.




(a)



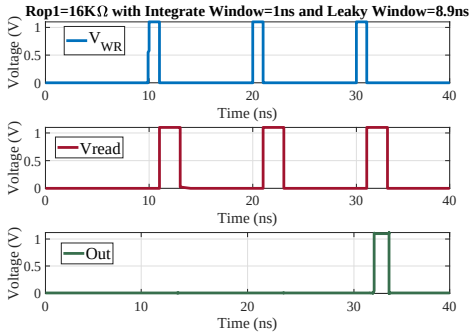

(b)

Fig. 11: Fault analysis modifying the Integrate Window.

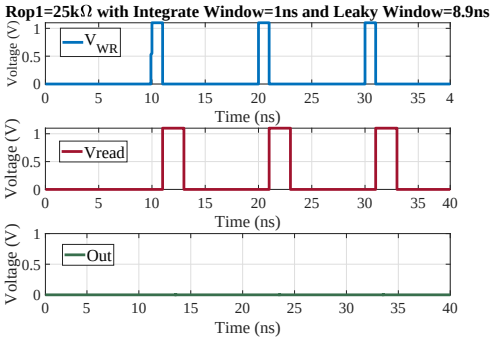
It is pertinent to note that the minimum detectable resistance for open $R_{op1}$ is $16K\Omega$ under the setup conditions of the original Integrate Window (See Table IV). Figure 11a illustrates the behavior of the SNN when $R_{op1} = 24K\Omega$ for an increased Integrate Window. Remarkably, the SNN is capable of generating an output spike. This observation suggests that the SNN, with the enlarged Integrate Window, can operate even with higher resistive opens than the SNN designed with the original Integrate Window. Conversely, Figure 11b demonstrates that the SNN fails to produce an output spike for $R_{op1} = 25K\Omega$, under the same increased Integrate Window. Hence, these findings underscore that the minimum detectable resistive open is contingent upon the size of the Integrate Window. More specifically, the minimum detectable resistive open increases with the enlargement of the Integrate Window.

### B. Modifying the Leaky Window

In this case, the performance evaluation of the SNN in the presence of a resistive open $R_{op1}$ is conducted by adjusting the initial set-up conditions of the Leaky Window (See Figure 6). In this experimental analysis, the *Leaky Window* duration is adjusted to 8.9ns instead of the original duration of 9ns. Meanwhile, the Integrate Window time remains unchanged from its original setting.




(a)




(b)

Fig. 12: Fault analysis modifying the Leaky Window.

It's important to recall that the minimum detectable resistance for open $R_{op1}$ is $16K\Omega$ under the original set-up conditions of the coding window (See Table IV). Figure 12a shows that the SNN can generate an output spike for $R_{op1} = 16K\Omega$ when the Leaky Window is extended. Conversely, Figure 12b illustrates that the SNN fails to produce an output spike for $R_{op1} = 24K\Omega$ when the Leaky Window is reduced. These results indicate that the minimum detectable resistance of the open depends on the size of the Leaky Window. Specifically,

the minimum detectable resistance of the open increases as the Leaky Window decreases.

## VI. Summary

Table VI presents the minimum detectable resistance for opens within the interconnection of synaptic currents, with modifications to both the Integrate Window (IW) and the Leaky Window (LW). The original configuration consists of an IW of 1ns and an LW of 9ns. In the second scenario, IW is extended to 1.2ns while maintaining LW at 9ns. In the third scenario, LW is decreased to 8.9ns while IW remains at 1ns. It is evident from the results that the minimum detectable resistive open increases with an increase in the Integrate Window, and the minimum detectable resistive open also increases with a reduction in the Leaky Window. Consequently, these findings suggest a dependency between the minimum detectable resistive open and the dimensions of the integrate and leaky windows. Moreover, the results advocate the consideration of additional fault models beyond the previously proposed "Slow to Integrate" and "Fast to Integrate" models [15]. Specifically, introducing "Slow to Leak" and "Fast to Leak" fault models is recommended to enhance test coverage.

| Open | Original | IW increases | LW decreases |
|---|---|---|---|
| $Rop1$ | 16KΩ | 33KΩ | 25KΩ |
| $Rop2$ | 3.1KΩ | 3.9KΩ | 3.3KΩ |
| $Rop3$ | 1KΩ | 1.5KΩ | 1.5KΩ |

TABLE VI: Minimum detectable resistance of the opens when the Integrate Window (IW) and Leaky Window (LW) are modified.

## VII. Conclusions

The investigation into the impact of manufacturing defects on SNN performance utilizing Magnetic Tunnel Junctions (MTJs) for synapse and neuron implementation has yielded significant insights. The SNN's behavior in the presence of injected defects has been studied through circuit-level simulations coupled with input spike application. Our findings reveal that resistive opens alter the accumulated synaptic current, impeding the neuron's ability to generate an output spike, particularly evident with sufficiently high resistance values of the open. Moreover, the results show that the open's minimum detectable resistance depends on the integrate and leaky window sizes. This observation prompts the consideration of additional fault models, specifically "Slow to Leak" and "Fast to Leak," alongside the previously proposed "Slow to Integrate" and "Fast to Integrate" models, to augment test coverage comprehensively. Our results have implications for refining fault models for generating high-quality test vectors, thereby contributing to more reliable SNN hardware implementations.

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