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Investigation of Single Event Effects in a Resistive RAM memory array by SPICE level simulation

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Abstract—Emerging non-volatile memories, based on resistive switching mechanisms and known as Resistive Random Access Memory (RRAM), are attractive candidates to overcome power, cost and integration density limitations of conventional memories. Moreover, RRAM has shown very good tolerance to radiation. In this context, this paper proposes to investigate Single Event Effects in RRAM memory arrays. The decoding circuitry of the memory array, including bit line and source line drivers is targeted. Currents generated by an ionizing particle crossing the memory array are first injected at specific nodes of the memory circuit. Their impact is evaluated by extracting the resistance state of each cell of the memory array before and after the ionizing particle strike. Worst cases scenarios are studied in order to point out the most sensitive configurations able to induce SEE.

Keywords – OxRAM, RRAM, SEE, SPICE simulation.

I. INTRODUCTION

Among the most promising technologies to meet the ITRS requirements for non-volatile memories, Resistive RAM (RRAM) [1-4] are attractive candidates, due to their appealing performances. Indeed, compared to conventional floating gate technologies, they gather fast write/read operations, low power consumption, CMOS compatibility and high endurance. It is worth noticing that in literature, the generic term RRAM is often used to refer to both Oxide Random Access Memory (OxRAM) and Conductive-Bridging Random Access Memory (CBRAM). In the rest of the paper, OxRAM technology will be considered. As radiation effects are nowadays recognized as a real reliability concern, it is mandatory to evaluate the hardness of these particular devices against radiations. Studies exist about the specific radiation constraint [5-9], but available works often address dose effects in the resistive switching element. Alternatively, RRAMs elementary cells based on hafnium oxide have demonstrated a tolerance against various kinds of radiations [10-15].

The aim of the paper is to perform a complementary analysis of the ones presented in [16,17], which focus on Single Event Effects (SEE) in the close proximity of the OxRAM cell (i.e., selection transistors). In these papers, the studied OxRAM cell has shown limited sensitivity to SEE. A threshold effect was pointed out and quantified in terms of current features. It was shown that the only configurations inducing effects were simultaneous impacts in a NMOS and a PMOS transistors, one being connected to the Bottom Electrode (BE) node and the other to

the Top Electrode (TE) node of the OxRAM cell. Then it was observed that the sensitive NMOS should be physically close to the sensitive PMOS for SEE occurrence. Depending on the considered technology and on the memory array, the distance between two sensitive transistors can vary from tens to hundreds of microns. So, only a particle crossing the structure (i.e., a particle with a long range), could impact the OxRAM memory array behavior. Then, the occurrence of such a case would probably be low but possible. Moreover, the simulations were performed for a specific structure corresponding to the worst case for single event radiation effects. However, in order to improve integration density and scalability in emerging technologies, 3D stacking technology is adopted where NMOS and PMOS transistors could be physically close. In that case, the OxRAM technology sensitivity to SEE could increase.

In OxRAM memories, MIM (Metal-Insulator-Metal) structure is used as a single-bit memory cell, while the semiconductor transistor subsystem enables performing all the peripheral operations (input/output, coding/decoding, line driving, and sense amplification). In the complementary study presented in this paper, as in previous investigations, the case of an ion crossing the MIM (Metal-Insulator-Metal) structure of an OxRAM cell is not considered. However, considering the insulator thickness and the probability of occurrence of such an event, it can be supposed that the impact on the global SER should be low if only SEE are considered (no combined effects with dose).

The remainder of this paper is organized as follows. Section II presents the OxRAM technology. In Section III, SEE is analyzed at the memory array level. Section IV presents simulation results showing the effect of SEE. Finally, Section V concludes this paper.

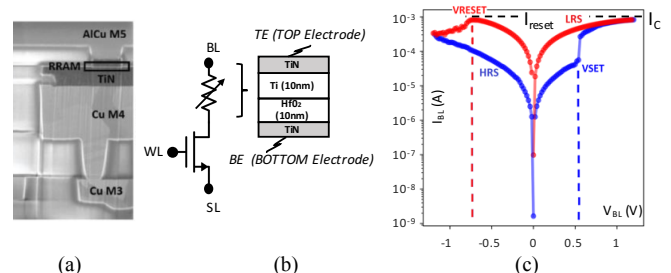


Fig. 1. (a) TEM cross-section of an OxRAM device (b) symbol view of a 1T-1R cell (c) OxRAM I-V characteristic in log scale.

II. RRAM TECHNOLOGY

An OxRAM memory cell consists of two metallic electrodes that sandwich a thin dielectric layer serving as a permanent storage medium. Its resistance may be switched between ‘0’ and ‘1’ states. The OxRAM Metal-Insulator-Metal (MIM) structure can be easily integrated in the Back-End Of Line (BEOL) on top of the CMOS subsystem [6-10]. Oxide-based resistive random access memory (so-called OxRAM) elements present a lot of interesting features like high integration density, high-speed operations (write/erase/read) and satisfactory reliability performances in terms of retention and cycling. Fig. 1b shows the basic 1T-1R memory cell where one MOS transistor is connected in series with an OxRAM cell. Fig. 1c presents a typical 1T-1R OxRAM I-V characteristic in logarithmic scale. Based on the I-V curve, the memory cell operation can be seen as follows: after an initial electro-FORMING (FMG) step [18], the memory element can be reversibly switched between the Low Resistance State (LRS) and the High Resistance State (HRS). Resistive switching corresponds to an abrupt change between the HRS and the LRS. The resistance change is triggered by applying specific biases across the 1T-1R cell, i.e., V_{SET} to switch to LRS and V_{RST} to switch to HRS. In the 1T-1R configuration, the transistor controls the amount of current flowing through the cell according to its gate voltage bias. The maximum current allowed by the select transistor is called the compliance current and is referred to as I_C in Fig. 1c. I_C controls the LRS resistance value in the SET state as well as the maximal RESET (RST) current I_{reset} .

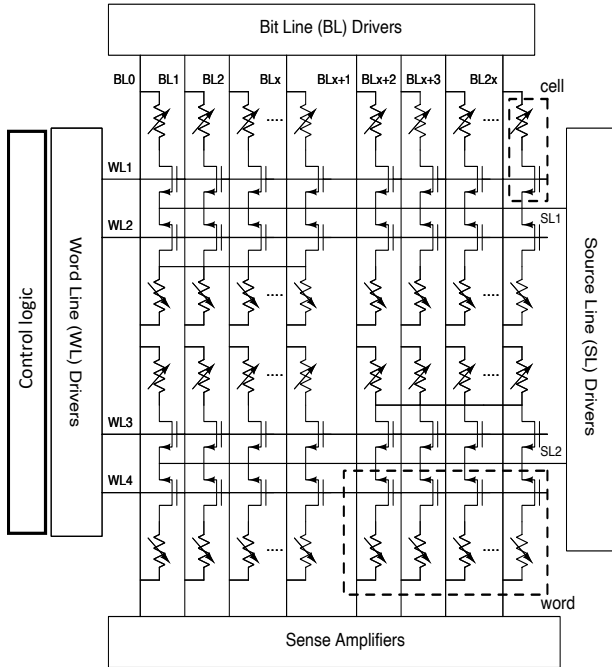


Fig. 2. Elementary memory array architecture used for simulations

III. SEE IN THE OXRAM MEMORY ARRAY

Fig. 2 presents the OxRAM memory array, considered in this work, which is composed of a word line driver to select the active row (WL_x), a bit line driver to select active bit lines (BL_x) during a FORM/SET and READ operations and a source line driver to select a specific source line (SL_x) during RST. Sense amplifiers are used to convert the cell current into a logical value at the circuit output during a READ operation. Memory cells are usually grouped into 8, 16 or 32 bits to form a memory word (dashed line). During the READ operations, the sense amplifier compares the cell current to a strictly controlled reference current.

The whole structure will be simulated using Eldo simulator at transistor level (SPICE simulation). The effect of a particle crossing the structure is simulated by adding a parasitic current source at the impacted node(s). The current value is negative when a NMOS transistor is struck and positive when a PMOS transistor is struck. The current source comes from the realistic simulation of a particle crossing a silicon volume using TCAD device simulation tools (Synopsys ©). The effect of the ion strike is simulated using the *Heavy Ion* module of Synopsys [19], considering an electron-hole pair column centered on the ion track axis. The Linear Energy Transfer is defined as the energy lost by the particle, by unit of length and varies along the track depending on the initial energy of the particles [20]. An actual variation of the LET was integrated in our simulations, based on the value given by SRIM tables [21]. Two kinds of ions are simulated: Alpha and Aluminum ions. The simulated Alpha particle is supposed to cross the device with an initial energy of 0.6MeV, which corresponds to a range of 2.3 μ m in the silicon volume. It corresponds to the end of the of an Alpha particle of 1.47MeV generated by the initial interaction of thermal neutron with boron-10 (Alpha contamination). The case of a more energetic particle is also considered. It is a 50MeV Aluminum which could be produced by the interaction of fast protons with silicon, for instance [22]. Two geometries are simulated for the two ions: crossing horizontally (hor.) or diagonally (diag.) the silicon volume. The associated currents are presented in Fig. 3. Al hor. corresponds to a total deposited charge of 723fC, Al diag. to 398fC, He hor. to 44fC and He diag. to 43fC.

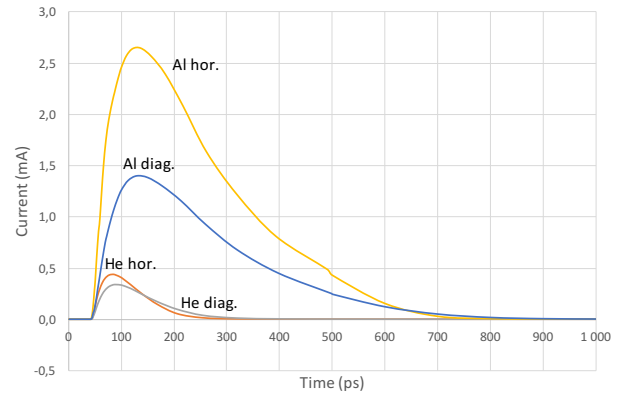


Fig. 3. Currents generated by Alpha and Aluminum particles in two different configurations: horizontal (hor.) and diagonal (diag.).

Thus, SEE is evaluated by injecting and simulating sequentially parasitic current source using the electrical simulator. Current sources, reflecting SEE, are injected at specific nodes of the memory array presented in Fig. 2. The goal is to determine which current source causes logical failures and which one does not but causes an important shift of OxRAM resistances (“analogue” faults). To evaluate the impact of each source on the memory circuit, the simulation process is automated. Currents are injected sequentially and the circuit responses are automatically extracted.

As the aim of this study is to get information about the worst-case configuration, the configurations able to induce a change in the initial state will be the only ones studied here. The investigation will focus on the most sensitive peripheral circuits to demonstrate the impact of a particle strike on the steady-state of the transistors directly involved to program the RRAM value. Among possible states (RST, SET, READ, WRITE, STBY), the standby operation is the longer state in term of duration. Then the probability for a radiation event to occur during standby is the highest and this configuration will be particularly explored.

IV. EFFECT OF SEE IN THE OXRRAM ARRAY

1) Fault simulation strategy

We implemented the memory circuit presented in Fig. 2 using a 0.13 μm High Voltage CMOS technology offering a 3.3 V supply voltage. A 3.3 V technology is required as the FMG operation involves high voltages. To verify the operation of our design scheme, SPICE simulations are performed using the *Eldo* simulator. Table I presents typical voltage levels applied to the memory cells during FMG, RESET, SET, READ and STBY operations. These voltage levels are provided by the Bit Line drivers (BL), the Source Line drivers (SL) and the Word Line (WL) drivers of Fig. 4.

TABLE I. OPERATING VOLTAGE LEVELS

	FMG	RST	SET	READ	STBY
BL	HV	L	H	HI	HI
SL	L	H	H	H	L
WL	H	H	H	H	H/L

^a H:2.5V, HV:3.3V, L:0V

Transient simulation results are presented in Fig. 4 considering the voltage levels presented in Table I. One cell of the memory

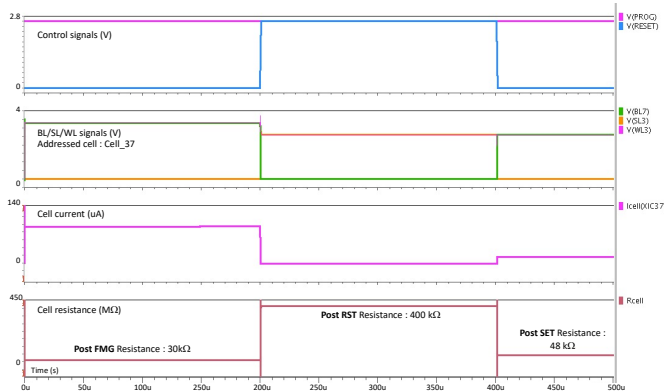


Fig. 4. Transient simulation results after FMG, RST and SET operations

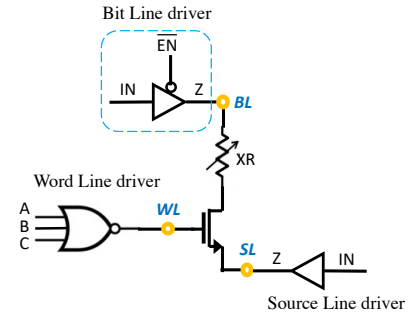


Fig. 5. Schematic diagram of one memory point and its peripheral circuit.

is addressed (Cell_37) by activating WL3, BL7 and SL3. The cell current I_{cell} (XIC37) and the final cell resistance (R_{cell}) are extracted after FMG ($\sim 30 \text{ k}\Omega$), RST ($\sim 30 \text{ k}\Omega$) and SET ($\sim 45 \text{ k}\Omega$) operations.

In this study, the investigation is focused on the peripheral circuit of one memory point (XR) depicted in Fig. 5. As shown, three logic gates are involved in the memory configuration, namely the bit line (BL), the word line (WL) and the source line (SL) drivers.

In order to better understand the electrical mechanism managing the bias voltage of each terminal (BL, WL and SL), the transistor level schematic of each CMOS driver is depicted in Figs 6.

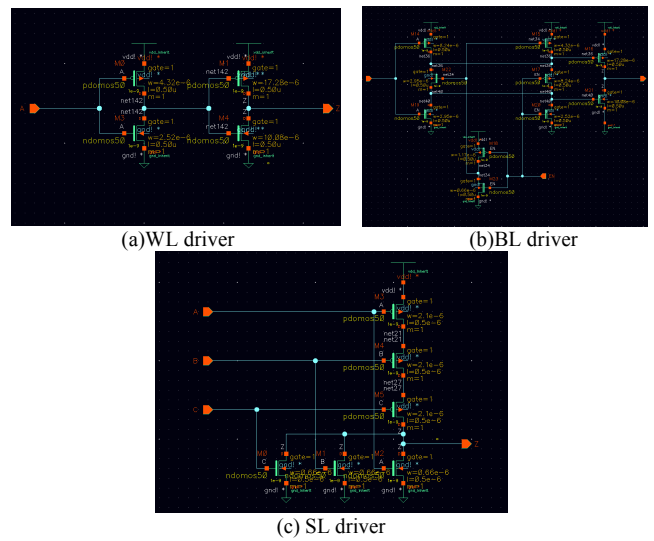


Figure 6. Sensitive node location at the memory driver level

The schematic diagram of one memory point is presented in Fig. 7 where only the transistors directly connected to the memory nodes are shown. As we can state, each terminal (BL, WL and SL) are faced with PMOS and NMOS transistors that are used to set the good operating voltage, according to the chosen configuration, as summarized in Table I.

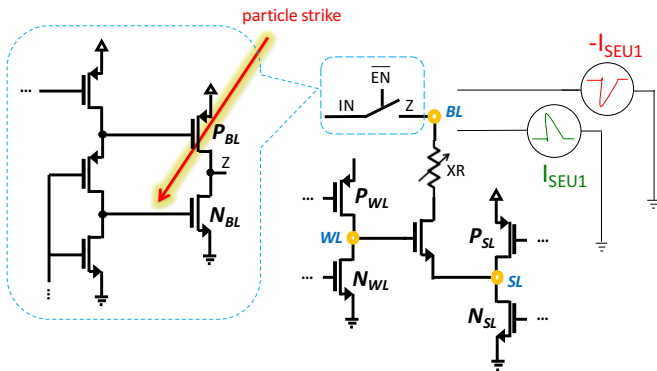


Fig. 7. Schematic diagram of one memory cell and its peripheral circuit at transistor level

Particle strike is supposed to cause a transient error on the nominal value of the bias voltage at each node (BL, WL and SL) directly connected to the RRAM memory. These specific nodes are considered as sensitive nodes regarding fault simulation due to particle crossing. Current spikes resulting of particle strikes are injected at these sensitive nodes and the state of each memory cell of the array is evaluated. Based on the considered memory array architecture, the only operating stage subject to SEE errors, leading to resistance drift is the STBY stage (Table II). In this configuration, the electrical values of the RRAM terminals (BL, SL and WL) are respectively high impedance (HI), low (L) and high or Low (H/L). To well understand the STBY configuration, we simulated the electrical operation of each driver (Fig. 8) focusing on the BL driver with HI value (depicted as a controlled switch in the Fig. 5). The BL driver is in fact a CMOS tri-state gate. When the EN terminal is set, the gate is *on* and the output voltage at the terminal Z (BL) is the same as the input one (IN). From an electrical point of view, these values correspond to $V_{DD}=2.5V$ (H) or $GND=0V$ (L). However, when the gate is *off*, the voltage value at Z terminal is around $V_{DD}/2$ depending on the voltage value at the input. This value corresponds to a metastable one (HI). This configuration is associated

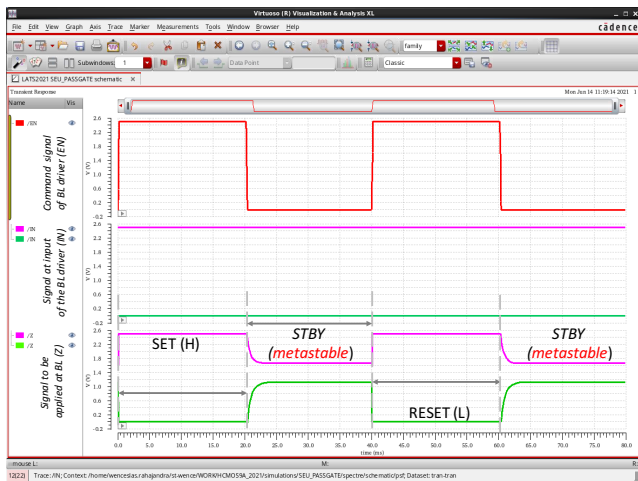


Fig. 8: Electrical value simulated at the output of the BL driver (BL node)

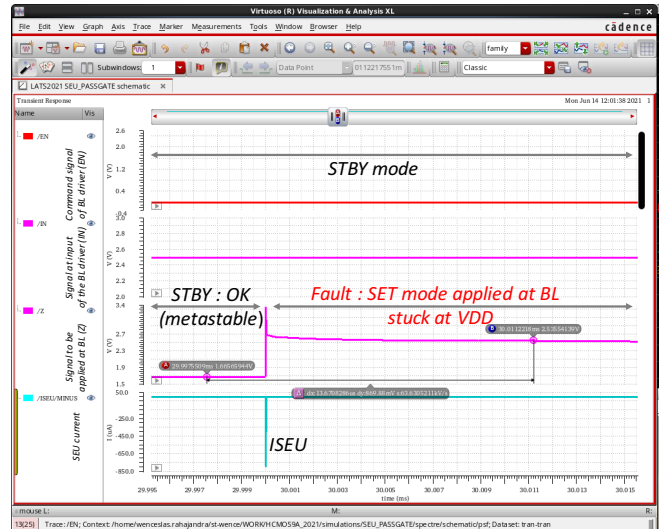


Fig. 9: Simulation of SEU strike on the BL driver (passgate).

with the STBY state. as given Fig. 9. shows the impact of a particle striking the peripheral transistor N_{BL} of Fig 6 during the STBY mode. This is done by injecting a very short current pic (I_{SEU}) at the Z node of the BL driver. We can see in Fig. 9 that the voltage value at node Z switches to V_{DD} (stuck at V_{DD}) leading to a fault on the memory configuration.

Several scenarios are possible depending on the path and the energy of the particle. We will focus in this paper only on the particles striking the peripheral transistors (P_{BL} ; N_{BL}), (P_{WL} ; N_{WL}) and (P_{SL} ; N_{SL}) of Fig 7. Indeed, these transistors act directly on the potential difference between the memory terminals. The next section will be dedicated to the worst case scenario identification.

TABLE II. PARTICLE STRIKE IMPACT

	FMG	RST	SET	READ	STBY
Impact	NO	NO	NO	NO	YES

2) Worst cases scenarios simulation

The worst-case scenarios are related to a particle strike impacting both the Bit Line voltages and Source Line voltages in STBY mode. Thus, extensive simulations are performed to assess the robustness of the memory array versus particles striking at these specific locations. Two configurations are studied. The first one considers a memory cell is LRS (Low Resistance State: 48 k Ω). The second one considers a memory cell is HRS (High Resistance State: 400 k Ω).

Fig. 10 shows the impact of a particle (at 50 us) on a HRS cell in STBY mode. The simultaneous impact of the particle on BL and SL nodes induces a voltage difference across the cell of the memory array connected to the impacted drivers. Then, a programming current through the cell is triggered and a change of

the cell resistance from HRS to LRS is detected. This event is named Single Event Upset (SEU) as the memory state is

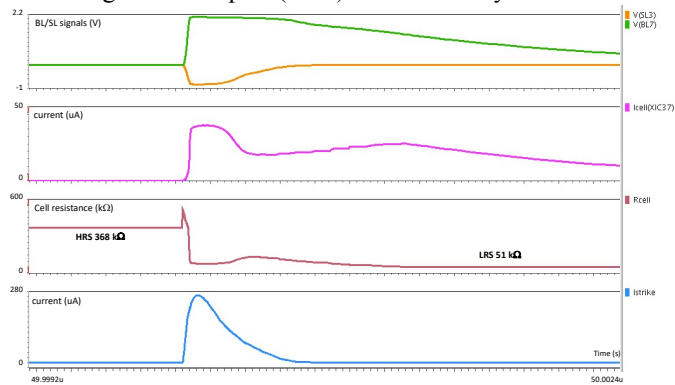


Fig. 10. Transient simulation results for a particle *Al hor.* striking a cell in HRS state

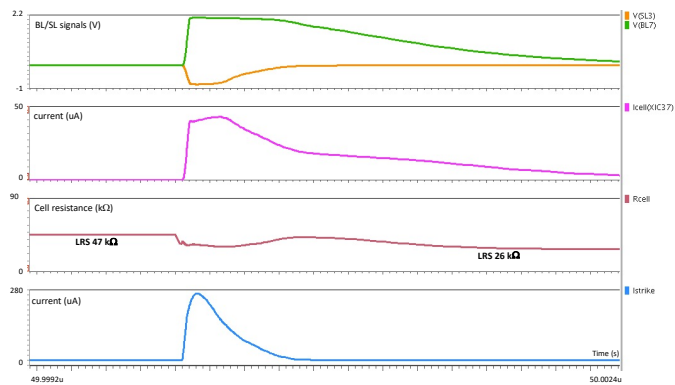


Fig. 11. Transient simulation results for a particle *Al hor.* striking a cell in LRS state

switched with respect to the OxRAM nominal values. For each simulated configuration in this work, a PMOS is simultaneously impacted with a NMOS. Then a negative current is injected when a NMOS is supposed to be struck, and a positive current for a PMOS.

Fig. 11 shows the impact of the *Al hor.* particle on a LRS cell in STBY mode. In this configuration, a shift of memory cell resistance towards lower LRS levels is observed. This resistance shift improves the LRS. However, going deeper in the LRS state can lead to programming issues during the next RESET operation. Indeed, if the LRS resistance value is to low, resetting the cell to HRS can be difficult or even impossible [18]. Then a stuck at fault will occur.

Table III summarizes the particle ~~the~~ impacts on the cell resistance when the cell is in an initial HRS or LRS state. Resistance shift, compared to the resistance nominal value before the strike, or radiative event (SEU or stuck-at-fault) are captured and presented. The analysis was conducted for the different current sources correlated with Alpha and Aluminum particles and presented in Section III. From this table, we can conclude than SEU will occur only in the HRS state and for a particle striking simultaneously a NMOS connected to the BL node and a PMOS

connected to the SL node. The opposite configuration does not induce errors but resistance shifts. Concerning the initially LRS state, for each configuration the LRS state is reinforced, potentially leading to stuck-at-faults. The resistance shift is then related to the injected current and the occurrence of stuck-at-fault will depend on the threshold of the RRAM cell. The resistance shift seems to be linked to the peak value of the generated currents. From Tab. III and from Fig. 3, we can note that the resistance shift is 28% for the Alpha particles, 39% for the Aluminum in the diagonal configuration and 45% for the Aluminum in the horizontal configuration. This clearly follows the trend of the current peaks presented in Fig. 3. This peak is linked to the deposited energy. Then the stuck-at-fault occurrence will depend on the energy deposited by the particle in the sensitive transistors surrounding the RRAM.

TABLE III. WORST CASE SCENARIOS RESULTS IN STBY MODE

	State	Negative current	Positive current	Resistance shift (%)	Effect
He diag.	HRS	BL	SL	-80	SEU
He hor.	HRS	BL	SL	-80	SEU
Al diag.	HRS	BL	SL	-85	SEU
Al hor.	HRS	BL	SL	-86	SEU
He diag.	LRS	BL	SL	-28	Stuck?
He hor.	LRS	BL	SL	-28	Stuck?
Al diag.	LRS	BL	SL	-39	Stuck
Al hor.	LRS	BL	SL	-45	Stuck
He diag.	HRS	SL	BL	0	NO
He hor.	HRS	SL	BL	0	NO
Al diag.	HRS	SL	BL	0	NO
Al hor.	HRS	SL	BL	0	NO
He diag.	LRS	SL	BL	-28	Stuck?
He hor.	LRS	SL	BL	-28	Stuck?
Al diag.	LRS	SL	BL	-39	Stuck
Al hor.	LRS	SL	BL	-45	Stuck

V. CONCLUSION

This paper provides a complementary analysis of Single Event Effect in a RRAM memory cell. As it was shown in [17], some specific configurations can induce effects in this kind of device, particularly when striking simultaneously a NMOS and a PMOS transistors, in standby operation. The configurations simulated here show that SEU could occur in RRAM cells for some specific topologies. This is the case if a NMOS connected to BL node is close enough to the PMOS connected to the SL node to be crossed by a single particle when initially at HRS. By avoiding this topology, SEU could be reduced. Other configurations, related to the LRS, can induce stuck-at-fault which could be more difficult to address than SEU because the cell then remains permanently in LRS.

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