Efficient Co-Design Methodology combinig Fast and Accurate System-level Simulations with Transistor-level Characterization

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Abstract— The Charge-Pump PLL (CP-PLL) stays one of the most popular circuit topologies used for frequency synthesis. Because of its mixed-signal nature, no established linear theory allows an exact description of its behavior, making its design challenging. In this paper an efficient design approach of the CP-PLL is presented achieving accuracy and time efficiency while considering nonlinear and non-ideal effects. A very efficient event-driven simulation model is combined with a CMOS-based design approach. The extracted macroscopic parameters are used at the behavioral level in order to allow a very fast but accurate closed-loop simulation, leading to a robust top-down and bottom-up co-design methodology.

Keywords— PLL, mixed-signal system, event-driven model, transistor-level simulation

I. Introduction

Nowadays, wireless communications and mobile applications are becoming more important and need the implementation of power efficient and high-density devices. Hence, mixed-signal systems are increasingly fully integrated. These systems mix analog and digital parts which can involve a nonlinear pulse-width modulated (PWM) sampling behavior. Thus, it is difficult to use general theories of feedback systems to characterize their dynamic behavior [1], [2] and a robust mixed-signal system design remains challenging [2], [3].

The PLL, as a typical example of mixed-signal systems, is an important component of modern electronic systems and is used among others for frequency synthesis, clock/data recovery, clock synchronization, jitter suppression, instrumentation and sensors [4], [5]. For its design, a time and computer resource efficient characterization methodology, taking into account all nonlinear and non-ideal effects, is necessary. The Charge-Pump PLL (CP-PLL) is one of the most popular PLLs used in the frequency synthesis application. It consists of five analog and digital blocks, as shown in Fig. 1 [6], [7]. It is featured with a digital phase and frequency detector (PFD), a charge-pump (CP) circuit, a loop filter (LF), a voltage controlled oscillator (VCO) and a divided-by-N counter (DIV). The PFD detects the relative phase error between the edges of the reference (Vref) and divider (Vdiv) signals. Then, it commands the charge pump to apply a correction signal whose pulse width is proportional to the detected phase error. A real charge-pump has several non-ideal effects, e.g. leakage current, finite switching slopes, current glitches and a current mismatch. The required loop filter damps the high frequencies of the signal and generates a voltage (Vctrl) that controls the VCO signal. Ideally, the oscillation frequency is a linear function of the input voltage. However, in reality, it shows a saturation curve with diverse slopes which affects the loop gain of the PLL and thus directly the stability of the system and its sensitivity to phase noise. Also, as the components of the different blocks exhibit parameter variations due to manufacturing drifts, the performances of the PLL vary accordingly. These variations can deeply influence the transient behavior (overshoot, settling) of the system.

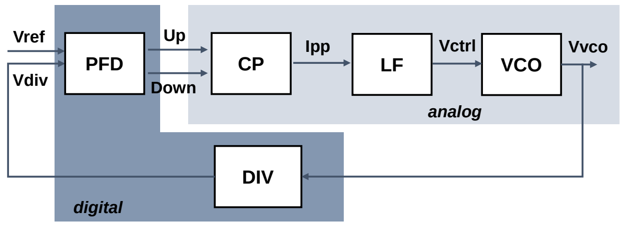

Figure 1. Mixed signal CP-PLL system representation

To simplify the design procedure of CP-PLL and to explore their nonlinear and non-ideal behavior, analytical models and simulative models are involved. Transistor-level (TL) models are very accurate, whereas behavioral models allow an easier handling of parasitic effects. The main bottlenecks of these approaches are the long processing times, the huge computational consumption and the overall design costs [3], [8]. Thus, a quick insight into the system behavior is made difficult endangering the guaranty of a robust design. In addition, at TL all non-ideal effects are considered at once, making the analysis of their singular and combined influences on the performances even more complex [1], [9]. Therefore, linear continuous-time models and linear discrete-time models are introduced as a simplified prediction criterion for their design [5], [6], [10]. These linear models allow to directly design the system regarding stability, loop bandwidth, overshoot and settling time. Since they are based on an early linearization, nonlinear and non-ideal effects are not considered [11]. However, it is essential to take them into account for a robust design, since they affect the stability, frequency purity and transient dynamic behavior [12], [13]. Additionally, the validity of these modeling approaches is limited to the domain close to the operation point, discarding them for transient pull-in predictions which are essential when considering frequency synthesis. They cannot characterize the

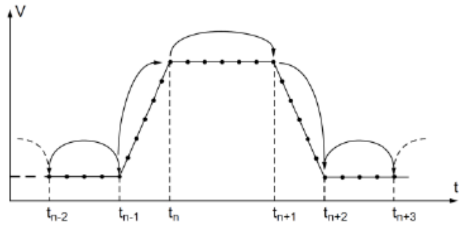

Figure 2. Transient behavior of an event-triggered CP-PLL

complex system properties like switching, pull-in process and chaotic behavior [14]. Design tools based on SystemC and SystemC-AMS [15] combine the system level representation with the circuit level. However, these tools are also based on conventional sampling methods which lead to high simulation durations, in the order of one hour or more, and thus, limit the ability of achieving a robust and optimized design [2], [8]. So, it is essential to investigate a more time and computer resource efficient modeling method which allows an exhaustive description of all nonlinear and non-ideal characteristics. To combine the accuracy of TL simulations and the efficiency of linear models, a CP-PLL can be represented by an event-triggered (ED) approach as illustrated in Figure 2 [16]. This approach calculates only the time points at which a change of the system dynamics occurs, reproducing exactly its expected system-level behavior. This methodology reduces drastically the processing time and the generated data (by a factor of around 10000), simplifying the interpretation of the results. The ED approach can be advantageously used to fully characterize and analyze the system in order to derive new and robust design criteria taking into account nonlinear and parasitic effects. Furthermore, this method can be used to characterize the highly chaotic behavior of mixed-signal system [9], [17]. The won knowledge will lead to a more robust design procedure which supports the designer to minimize the malfunction risks and therefore to reduce the overall realization costs.

An efficient design approach of CP-PLL is presented in this work. It achieves time and therefore cost efficiency together with accuracy considering several nonlinear and non-ideal effects. In section II, the proposed ED modeling and design approach is presented. Section III describes the design of the separate building blocks of the CP-PLL using Cadence tool. Their extracted parameters are presented and will be used in the ED tool simulator for the whole PLL simulation. The obtained results are compared and analyzed in section IV. Conclusion is given in section V.

II. EVENT-DRIVEN BASED DESIGN APPROACH

The complexity in analyzing the CP-PLL is inevitable due to the fact that the PFD-CP is a sampling system, resulting in a quantization-like effect. In fact, a quantization effect appears since the PFD reacts to the edges of input signals at the discrete time point. This effect produces further ripple at the control node of the VCO [5], [18]. The ED approach uses the phase equations of the reference and feedback signals on the PLL unlike the event-triggered simulations using behavioral models [19]. The approach presented in [9] has been applied mostly to the current-switched CP-PLL architecture, and also has been extended to voltage-switched CP-PLL [17]. The principle of the ED technique is based on calculating the sequence of switching instants at which falling (or rising) edges of the reference and the divider signals trigger the tri-state PFD [20]. The efficient ED algorithm is depicted in Fig. 3 [14], [21]. To simulate the dynamics of the CP-PLL, a set of state variables characterizing the ED model are defined. All macroscopic parameters of the system at t_n can be grouped within a vector M_n:

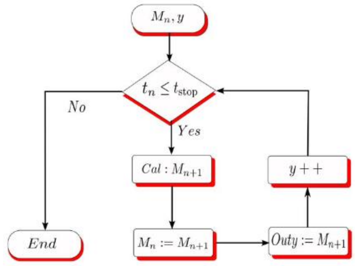

Figure 3. Simulation algorithm of the ED model

$$M_n = [t_n, \phi_{div}(t_n), \phi_{ref}(t_n), V_{ctrl}(t_n), V_p(t_n)]^T \quad (1)$$

where ϕ_{div} and ϕ_{ref} are the phases of divider and reference signals, respectively.

By knowing M_n, all the system macroscopic parameters in vector M_n and simulation step index y has to be initialized at the beginning. Then, the algorithm calculates and memorizes all the system variables at the next triggering event M_{n+1}. Before the next iteration step, M_{n+1} is assigned to M_n and saved in an output matrix at the y^{th} column and so on. The algorithm breaks when it reaches the stop time t_{stop}. By using this approach, it is sufficient to determine the instant at which a falling edge from Vref or Vdiv occurs. Taking into account these instants, state variables are calculated [17].

The proposed design methodology utilizes both this efficient ED model to optimize the design process of CP-PLL and TL simulations to characterize the system building blocks separately. This characterization step generating a library of several blocks of CP-PLL is done only once. The resulting characteristics, included in the library, are translated into the ED model. This enhanced ED model allows to describe the complete behavior of the CP-PLL considering all major nonlinear and non-ideal effects. On the one hand, the ED model can be used to perform time and computer resource efficient simulations which accompany the design process. On the other hand, it can be utilized to efficiently characterize system properties in detail. The gathered knowledge enables the investigation of new, reliable, optimized and analytical design criteria which will be finally useful to configure the TL components in relation to the requirements given by the application. Afterwards the obtained design is validated using the full circuit simulation at transistor-level and is adapted, if necessary, by the optimized design criteria. Once the library and the optimized and analytical design criteria are obtained, future designs will be even faster, reducing drastically the time-to-market of a PLL and thus the overall design costs.

III. DESIGN OF CP-PLL BUILDING BLOCKS

The design methodology consists, first, in simulating the CP-PLL building blocks separately. Then, the main performances are automatically extracted and supplied to a tool based on ED model developed during this project. Each unitary block, made up of a few dozen transistors at most, is characterized in a very short time (of the order of a second). Nevertheless, transistor-level simulations of a complete PLL can represent hours of simulation for a single simulation corner. It is therefore essential to use the event-driven approach to greatly reduce simulation time and computer resources and also to be able to cover all cases of process, temperature and voltage (PVT) because it remains mandatory to verify these operating conditions before manufacturing the circuits.

The blocks of the PLL, presented in Fig. 1, are designed using Cadence Virtuoso in 130nm CMOS technology, followed by transistor-level simulations using Spectre simulator. In this work, a quartz crystal is used to generate oscillations at a high precision reference frequency of 18.94 MHz. The frequency divider is used to divide the oscillation frequency that comes from the VCO. The implemented circuit consists of high-frequency D-flip-flops, positioned in series, based on true signal phase clock (TSPC) structure since it is faster and less power-hungry. The PFD compares the phases of the reference and feedback signals and produces two output pulses (Up and Down) depending on the phase difference. The designed tristate PFD is a digital circuit based on SR laches with feedback NANDs and OR delay cells. Each Up and Down portion is connected with a capacitance to reduce the glitches due to Vref and Vdiv pulses lead-lag operation. Then, PFD outputs are connected to a current-switched charge-pump (CSCP) block, shown in Fig.4, that converts the logic voltages Up and Down into current. The Up and Down signals control the activation of two MOS transistor switches. It allows either injecting a current Ipp_Up into the filter, which will increase its output voltage, or injecting a current Ipp_Dn that will reduce the output voltage. Based on cascoded sources, its main aim is to deliver a stable current with precise matching between Ipp_Up and Upp_Dn. The sources used to generate these currents are identical. Two NMOS transistors (N4) are used to provide the reference current, which is adjusted via the R2-R3 resistor bridge and the values of R1 degeneration resistors. The reference current is then amplified by cascoded sources (P1-P2 and N1-N2 for Ipp_Dn and P3-P4 for Ipp_Up).

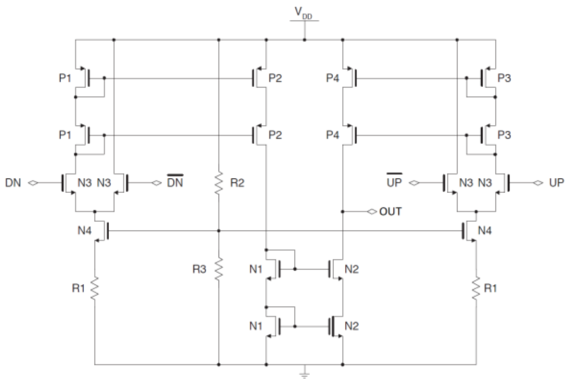

Figure 4. Current-Switched Charge-Pump schematic

Nevertheless, in reality, the CMOS CSCP suffers from non-ideal effects related to the circuit implementation such as a delayed current pulse and a current mismatch between Ipp_Up and Ipp_Dn current sources [9]. These issues are considered through an optimal sizing of the current mirrors of the CP.

The loop filter adjusts the output signal and minimizes the ripples to maintain stability and to reduce the noise. The designed LF is a second order low-pass filter consisting in a resistance (R1) in series with a capacitor (C1) and a second capacitor (C2). A loop filter of order 2, sufficient to ensure PLL stability, results in a complete order 3 system. The components have been sized based on an extraction from a Matlab program and then simulated with Spectre to optimize the minimal damping factor and the phase margin.

The VCO is a key component in the PLL generating a high oscillation frequency that can be controlled by the LF voltage swing. In this design, a differential ring oscillator with 2 delays cells has been used. Each delay cell consists of a differential pair of NMOS differential pair whose transistors drains are connected to an active load. This load is realized by a cross-coupled differential pair of PMOS and a pair of PMOS transistors connected as a diode [22]. Table I summarizes the main parameters extracted from the TL simulations of the blocks considered separately.

Table I. Extracted parameters from transistor-level simulation of CP-PLL.

Parameter	Unit	Description	Typical Value
REFERENCE SOURCE			
F_clk	MHz	Reference frequency	18.94
Jitter_std	ps	Noise jitter standard deviation	3
PHASE FREQUENCY DETECTOR			
Delay_Up	ns	Time delay of output signal (ns)	0.80
Delay_Dn	ns	Time delay of output signal (ns)	0.84
CHARGE-PUMP			
Ipp_Up	µA	Output UP current	5.14
Ipp_Dn	µA	Output DOWN current	-4.97
Ipp_leak	nA	Leakage current	34.4
I_slope_Up	MA/s	Linear slope of rising current	13.5
I_slope_Dn	MA/s	Linear slope of falling current	-20.4
LOOP FILTER			
R1	Ω	First stage resistor	235.1
C1	fF	First stage capacitor	198.0
C2	fF	Second stage capacitor	19.8
OSCILLATOR			
Kv	GHz/V	Linear VCO gain	-0.386
Noise_stdev	ps	Jitter standard deviation	0.52
FREQUENCY DIVIDER			
delay	ps	Propagation time of each flip-flop stage	566.0

IV. FULL-PLL RESULTS

Once the representative parameters of standalone block have been extracted from transistor-level simulations, the full PLL can be simulated. By considering the identical parameters, TL simulations are run using Cadence Virtuoso and ED simulations are run using the tool developed during this project.

The simulation time for TL simulations is 15 minutes, while only 0.11 second for the ED simulations. Fig. 5 shows the evolution of the Vctrl voltage at the loop filter output. As the role of this voltage is to control the PLL output oscillation frequency, it represents a crucial parameter to exhibit the accuracy and the validity of the ED model.

It can be seen that both curves are visually close. A number of parameters can be used to judge the accuracy of the ED simulation compared to the TL simulation, including the final value of Vctrl (Vctrl_Final_Val), the settling time (t_settle) after which the value of Vctrl no longer varies from its final value +/-5%, or the number of oscillations of Vctrl before settling. These parameters are listed and compared in Table II. The usefulness of ED simulation becomes all the more apparent when numerous simulations are required. For example, in order to simulate the crossed corners of the full PLL, all the parameters that can vary independently of each other, such as temperature, supply voltage, process corners of the components must be take into account.

To cover all these crossover cases, 1215 simulations are required, which represents, for the simple PLL schematic view, 13 days of TL simulation. This is given that it is possible to extract the performances of all the blocks individually and

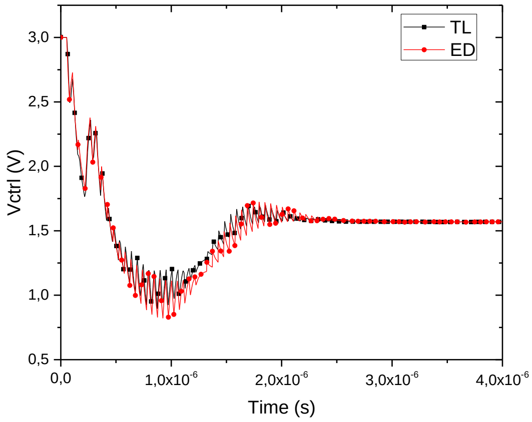

Figure 5. Transient Vctrl response using transistor-level and event-driven simulations

in each manufacturing corner, notably using automated characterization tools such as Cadence-Ocean. Nevertheless, all these cross-cases can be simulated using ED simulation in less than 2 minutes.

As an example, Fig. 6 shows an ED simulation of the transient evolution of Vctrl voltage for 3 extreme PVT cases of the loop filter. Component values (resistors and capacitors) are modified by +25% and -25% for the "best" and "worst" cases, respectively, compared with the typical case. This makes it possible to study the effects of PVT variability in one or more blocks on the overall operation of the PLL. Fig. 6 shows that increasing the capacitance values results, in the "best" PVT corner, in better damping of Vctrl oscillations.

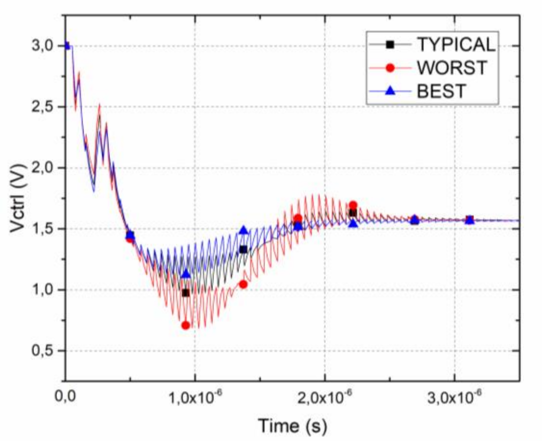

Fig. 6 Transient Vctrl response of the PLL for 3 LF process corners

Another important parameter concerns the size of the generated data during simulations. For the same complete PLL simulation, Cadence simulation generates 107MB of data, while the ED simulation generates only 315kB, while still providing voltages and currents plots at the most important nodes of the circuit.

Table II. Comparison of the full PLL results using TL and ED simulations

Parameter	ED simulation	TL simulation	Difference
t_settle	2.13 µs	2.08 µs	2.3 %
Vctrl_Final_Val	1.5688 V	1.5687 V	0.01 %
Oscillations Number	45	45	0%
t_Simulation	0.11 s	900 s	+82000%
Generated simulation data	315 kB	107 Mb	+340000%

V. Conclusion

This paper presents an efficient co-design methodology for non-ideal CP-PLL. It combines fast and accurate event-driven simulations together with transistor level characterization using Cadence Virtuoso. This methodology shows nearly the same PLL behavior with an extremely shorter simulation time (-82000%) and low amount of produced data (-340000%) compared to a standard approach.

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