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Wafa Zitouni, Rémy Vauché, Hassen Aziza, Laila Ayache, Alaa Makdissi. Cortex-M0+-based Pacemaker: CMOS Technologies Benchmark to Achieve Ultra-Low Power Operations. 2023 IEEE International Conference on Design, Test and Technology of Integrated Systems (DTTIS), Nov 2023, Gammarth, France. pp.1-5, 10.1109/DTTIS59576.2023.10348200 . hal-04524656

HAL Id: hal-04524656

<https://hal.science/hal-04524656>

Submitted on 28 Mar 2024

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Cortex-M0+-based Pacemaker: CMOS Technologies Benchmark to Achieve Ultra-Low Power Operations

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Abstract—Continuous progresses in biotechnology and microelectronic are constantly pushing the limits of miniaturization and power consumption for active implantable medical devices such as pacemakers. Implanted pacemakers are battery operated embedded systems for which autonomy is an important constraint to extend the device lifetime. However, the pacemaker’s processor consumes most of the battery energy since it must analyse in real time the heart activity. Thus, the choice of the appropriate CMOS technology for the processor manufacturing is a crucial point. In this context, this paper proposes a method to mainly estimate ARM-based processor power consumption. This method has been applied to three manufacturing technologies from STMicroelectronics. Simulation results show that considering a temperature of 27°C, the average leakage powers consumed by a Cortex-M0+ for HCMOS9A (1.2 V), CMOS065 (1 V) and FDSOI (1 V) technologies are respectively 300 nW, 136 nW and 486 nW and the active energies are respectively 398 μ W/MHz, 49.9 μ W/MHz and 20.3 μ W/MHz. However, the FDSOI technology can obtain leakage power consumption similar to the CMOS065 one by reducing the supply voltage to 0.8 V. Finally, regarding the power consumption, the area, and the price criteria, the CMOS065 seems to be the technology which offers the best compromise regarding power dissipation, area, and cost, even if an increase of 10 °C has led to an average leakage power increase between 30% and 54,5% for the three technologies.

Keywords—digital design, ultra-low power, pacemaker, Cortex-M0+, FDSOI, HCMOS9A, CMOS065.

I. INTRODUCTION

Modern pacemakers are designed to be energy-efficient in order to ensure long battery autonomy and also to minimize the battery replacements frequency [1]. The first step to design a microprocessor-controlled pacemaker is also to select an appropriate processor based on the requirements of the pacemaker, such as computational capabilities, power consumption, and communication interfaces. Processor selection is a critical decision as it determines performances and features of the pacemaker.

The processor, augmented with the memory system, peripherals, and other system support components (power management, clock generation circuits, debug interface, etc.), is then integrated into a microcontroller, itself integrated in the overall pacemaker system which can include various electronic components, such as sensors and batteries. Next, the microcontroller firmware which controls pacemaker operations must be developed. Finally, the pacemaker design methodology ends with rigorous tests and verifications, and compliance with regulatory standards. It is worth noticing that the processor is equally called the Central Processing Unit (CPU) and that it is generally the central component in

an electronic system since it performs most of the processing tasks, including executing instructions and computations, in addition to manage data flows.

Processor options for pacemakers include Application Specific Integrated Circuits (ASICs). The ASIC is designed to meet the specific requirements of a pacemaker, including power management, communication, pacing and sensing. However, ARM Cortex-M processors are specifically designed to offer a good balance between performance and power consumption [2]. Moreover, ARM processors are provided as Intellectual Properties (IPs) intended to be integrated at the ASIC level and are available in a range of configurations to meet different requirements.

Nevertheless, at the design level, no systematic approach is available to evaluate power consumption regarding the targeted manufacturing technology. For this reason, the proposed work introduces a methodology to quickly evaluate power consumption of an ARM Cortex processor for different manufacturing technologies and before silicon implementation. In this paper, only the Cortex-M0+ have been considered due to its better energy efficiency compared to other Cortex processors [2].

The main contributions of the paper are:

- a Cortex-M0+ processor core block has been synthesized up to the gates level;
- the overall Cortex-M0+ consumption has been assessed in terms of leakage power and active energy (power consumption divided by switching frequency) for the HCMOS9A 130 nm, the CMOS065 65 nm and the FDSOI 28 nm technologies from STMicroelectronics using their low power standard cells;
- a benchmark is conducted to point out the optimal technology regarding power consumption, area, and cost.

The paper is organized as follows. A presentation of an implantable pacemaker is provided in section II, in addition to an overview of an ARM processor and a presentation of the digital design flow. Section III is dedicated to the manufacturing technologies, the methodology used to evaluate the power consumption of the Cortex-M0+ core, and the results obtained at 27°C. Finally, temperature effect has been studied in section IV and section V concludes the paper.

II. BACKGROUND

A. Implantable Pacemaker

A pacemaker is an implantable electronic device used with patients suffering from bradycardia to increase their heart rate by sending electrical pulses when it is required. The implantable pacemaker is an integrated real-time battery-

powered system that should be small and operates with a low power to increase battery life and surgical time [1].

Cairdac [3] is developing an autonomous leadless pacemaker using a Piezoelectric Energy Harvester (PEH) that converts the kinetic energy of the heart to electrical energy. Fig. 1 describes the basic elements of the Cairdac's leadless pacemaker. The pacemaker is also composed of three chips:

- the Power Management Unit (PMU) ASIC which is connected to a harvester [4] and a rechargeable battery;
- the Therapy ASIC which is responsible for the electrocardiogram acquisition, the heartbeat detection, and the cardiac stimulation through two electrodes (tip and ring);
- the CPU chip which is a microcontroller chip containing the processor designed to handle control and computational tasks.

The CPU chip communicates with the two ASICs via multiple interfaces: serial peripheral interface (SPI), universal asynchronous receiver transmitter (UART) and several general-purpose input-outputs (GPIO). Finally, the CPU chip typically also contains a memory subsystem (e.g., Flash memory Boot ROM and Static Random-Access Memory) [2] as shown in Fig. 2.

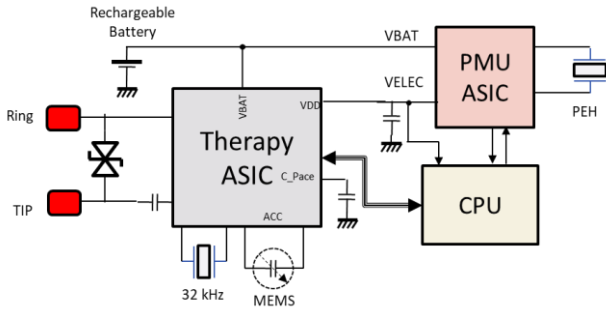


Fig. 1. Cairdac implantable pacemaker architecture

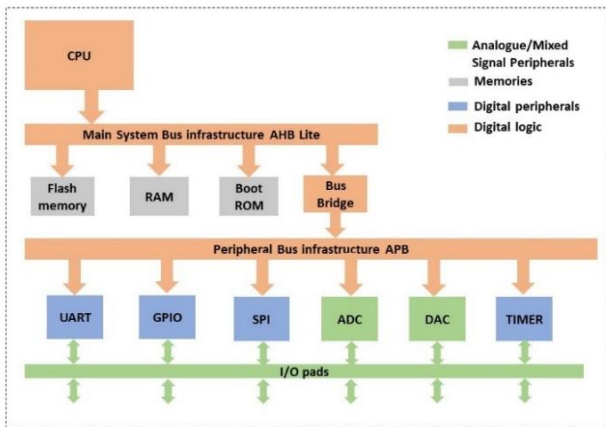


Fig. 2. The CPU ASIC components [2]

In this context, pacemaker must offer at least two modes of operation: an active mode and a sleep mode. Implantable pacemakers should be in sleep mode most of the time and in active mode only for a short time duration [5]. Fig. 3 shows an example of the CPU ASIC's current consumption during its different modes (sleep and active modes). Nevertheless, several sleep modes can be available, such as deep sleep modes which allow an ultra-low power consumption at the cost of a partial or full RAM content lost.

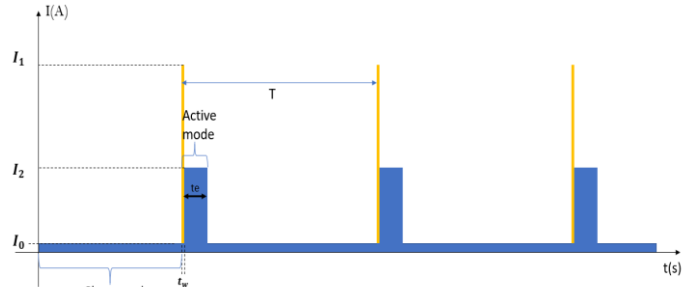


Fig. 3. Example of CPU ASIC current consumption having an active and a sleep mode

In the Fig. 3, the CPU chip consumes I_0 during sleep mode. Next, the CPU wakes up and consumes I_1 during t_w second (wake-up phase). Finally, during active mode which has a duration of t_e , it consumes I_2 . The average of the current consumption of the CPU chip over a period T can also be calculated as follows:

$$\langle I \rangle = \frac{I_0 (T - t_w - t_e) + I_1 t_w + I_2 t_e}{T} \quad (1)$$

where I_1 should be higher than I_2 and I_2 should be higher than I_0 .

The overall system consumption is affected by the sleep time duration, as demonstrated in equation (1). Therefore, decreasing the wake-up and the active times (t_w and t_e) will enhance the energy efficiency of the CPU chip.

B. ARM Processor Family

The Cortex-M processors are designed for the mainstream microcontrollers market where the sleep modes performances are less critical but must be low power enough especially for battery-powered systems. Nevertheless, the Cortex-M0+ is the most energy efficient ARM processor [2].

The cortex M0+ is a 32-bit RISC processor, having a frequency up to 50 MHz with a 2-stage pipeline von Neumann architecture [6]. Fig. 4. shows the cortex-M0+ processor diagram. The most important block is the processor core which consists of the control unit, the arithmetic logic unit (ALU) and some registers. Optional features are provided for the cortex-M0+: a debug system, a memory protection unit (MPU) to avoid access to some registers, and the micro trace buffer (MTB) that provides a trace of instructions [2].

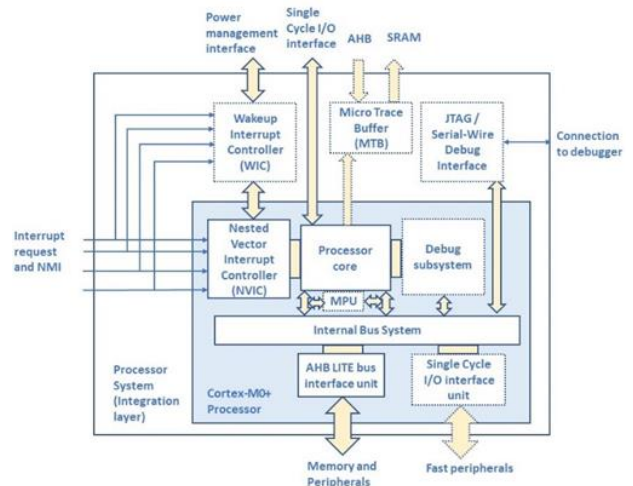


Fig. 4. Block diagram of the Cortex-M0+ processor [2]

Developing low-power applications using ARM Cortex-M0+ can be achieved through a variety of approaches [2]. The most common approach is to increase the clock frequency as much as possible, to run quickly the application, and then go to sleep. However, the downside of this approach is that the peak current could be higher and not compliant with the battery characteristics. Besides, enabling and boosting the clock may be required whenever the microcontroller wakes up, which may take some time. Slowing down the clock's frequency as much as possible can be another option. It can lead to a significant decrease in the active current and it is suitable only for application that require periodic tasks. An alternative approach is the Dynamic Voltage and Frequency Scaling (DVFS) technique which is widely used to match system power consumption with required performance [2].

C. Digital Design flow & Technology

Most of the microcontrollers are designed with Complementary Metal Oxide Semiconductors (CMOS), although some other technologies like Bi-polar CMOS could be used. Technologies classification is primarily based on the channel length of the transistor. The smaller the channel length is, the smaller the transistor is and the faster its switching frequency is. Thus, moving to smaller transistors can reduce dynamic power but it can also significantly increase the leakage power. As a result, it is common for microcontrollers to be lagging behind high-end SoC designs in terms of used semiconductor technologies, especially for applications which requires ultra-low leakage power consumption. In this work, the targeted technology nodes are the HCMOS9A (130nm), the CMOS065 (65nm), and the FDSOI (28 nm) from STMicroelectronics.

At the digital design level, ASIC design complexity is alleviated by using the high-level description language (HDL) such as the Very high-speed integrated circuit Hardware Description Language (VHDL) and Verilog language. A classical digital design flow is presented in Fig. 5. The flow starts with the description of the system in HDL. The next step is the logic synthesis which allows to obtain a circuit description at the gate level. The software used for logic synthesis generates a synthesized netlist and post-synthesized simulations must be performed to validate the design. Once the post-synthesis simulations are performed, the placement and routing step provides a physical implementation of the integrated circuit (IC). If this step is not performed properly, it may have a significant impact on the final design of the IC in terms of performance, power, and area [7].



Fig. 5. Classical digital design flow

III. INTEGRATION AND IMPLEMENTATION

A. Choice of standard cells libraries

The basic elements of a digital circuit are logic gates. Most of technologies provide foundry libraries with logic gates which are called standard cells. Each logic gate of a standard cells library is standardized in terms of layout size in order to be easily interconnected with the others library cells. Moreover, a standard cells library generally uses a particular type of MOS flavours such as high speed (HS) equally called for example low threshold voltage (LVT), or low leakage

(LL) equally called for example on high threshold voltage (HVT), according to the expected performances.

In this paper, the goal is to minimize the average leakage power and the internal energy. For this reason, libraries based on MOS transistors with the highest threshold voltage and the lowest supply voltage will be considered since more the threshold voltage is, less the average leakage power is and less the supply voltage is, less the active energy is.

HCMOS9A offers ultra-low leakage transistors with a supply voltage of 1.2V. The digital library *CORE9ALLPULL* based on this flavour of MOS has been used in this paper.

CMOS065 supports various supply voltages (2.5V, 1.2V and 1V) and proposes high threshold voltage transistors. The digital library *CORE65LPHVT* based on this MOS flavour and optimized for low power applications (1V operations), has been used in this work.

Finally, the FDSOI technology supports several standard cells. Nevertheless, the digital library *C28SOI_SC_12_COREPBP16_LR* based on regular threshold voltage MOS transistors has been used for this work, firstly with the native supply voltage of 1V, but equally with an experimental supply voltage of 0.8V (which is not officially supported by the founder) as in [8].

B. Digital design methodology

The Cortex-M0+ IP delivered by ARM is written in Verilog language [6] and *Synopsys design vision* has been used as synthesis tool. The associate synthesis flow is also presented in Fig. 6.

The input files are the register transfer level (RTL) files, clock constraints and the library files. The RTL files contain the description of the circuit in VHDL and Verilog languages. The clock constraints contain clock-related information such as system clock frequency, and signals to system clock delays. Finally, the library file contains the standard cells which are related to power, timing, and area specifications.

Synopsys design vision outputs are the synthesized gate level netlist (based on the used standard cells) and the standard delay format file containing the timing details of the synthesized chip. Moreover, report files which contain different information related to the gate level netlist (such as area, used standard cells, etc.) are also generated. Finally, a *Synopsys* design constraint file (SDC) provides timing, power, and area constraints of the design.

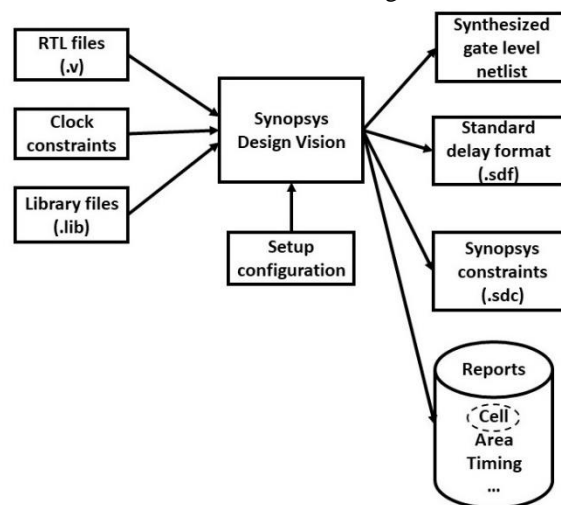


Fig. 6. Synthesis flow

The synthesis flow first step is also to elaborate the design which means to transform the Verilog description language files to an intermediary file based on *Synopsys* database technology. At this level, the design uses an abstract *Synopsys* technology library called *GTECH*.

The next step is to implement the clock tree and to add various constraints to make the synthesis result workable. Next, the compilation is intended to map the intermediary file to the standard cells of the targeted technology. During this “elaborate” step, the *GTECH* file report is used as the entry point for the estimation of the Cortex-M0+ power consumption at the gate level for the three targeted technologies. Indeed, this file provides the number and the type of logic cells used in the design.

The Cortex-M0+ synthesis has been firstly done with the HCMOS9A technology. The returned design is composed of 8728 logic cells disturbed as illustrated in Fig. 7. In this paper, the same logic gates, having the same or approximatively the same fan-out, have been considered for CMOS065 and FDSOI technology. The design is composed mostly of AND2 and OR2 gates. Others blocks include multiplexers, buffers and some combination of basic gates such as AO2 gates (52 double input AND into 2 input OR).

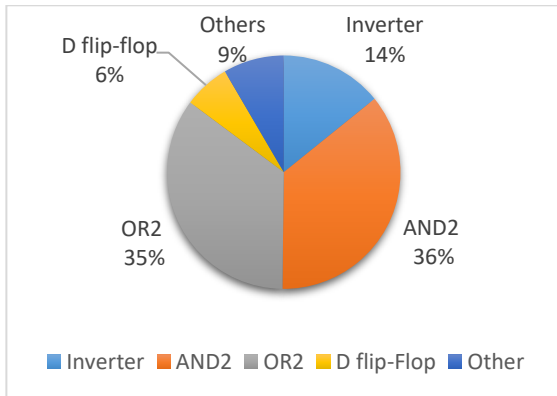


Fig. 7. Cortex-M0+ logic cells distribution with HCMOS9 technology

Next, the methodology for power consumption estimation consists in the evaluation of the average leakage power consumption and the active energy for each logic cell using simulations. All the input logic combinations of each standard cell have been considered and the worst-case scenario has been kept.

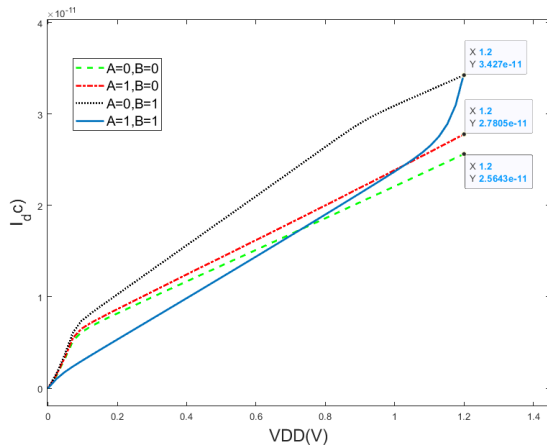


Fig. 8. Leakage Power consumption of the HCMOS9A 2 inputs AND

Table I shows an example of the determination of the average leakage current consumption of a 2 inputs AND cell (A and B are inputs and Z is the output) of the HCMOS9A technology based on the simulation presented in Fig. 9.

TABLE I. HCMOS9A 2 INPUTS AND ULTRA-LOW POWER CELL LEAKAGE CURRENT CONSUMPTION

A	B	Z	I_{dc} (pA)
0	0	0	25,64
0	1	0	34,27
1	0	0	27,8
1	1	1	34,27

The considered total average leakage power consumption P_{and2} related to all the required 2 inputs AND cells has been computed as follows:

$$P_{and2} = N_{and2} \frac{(I_{max0} + I_{max1})}{2} \times VDD \quad (2)$$

where N_{and2} is the number of the AND2 cells, I_{max0} is the maximum leakage current consumed for a ‘0’ output, I_{max1} is the maximum leakage current consumed for a ‘1’ output, VDD is the supply voltage. It has also been supposed that the probabilities on the output logic states are equilibrate. The output of the two combinations (A=0, B=1 and A=1, B=0) in table I is identical, but the leakage current consumption is slightly different since the AND gate is composed of a NAND gate followed by an Inverter and the two NAND NMOS transistors are in series (and also does not have the same V_{gs} for the both configuration).

The active energy of a cell has been determined by extracting the average current consumption for two very different inputs switching frequencies (example: 10 MHz and 100 MHz applied on a one or more inputs, depending on the worst case), which allows to deduce the power consumption for the both frequencies, as shown in Fig. 9. in the case of the HCMOS9A 2-inputs AND cell. Thus, the active energy of this logic gate is equal to the slope of this curve. It is also obviously necessary to multiply this result by the number of required 2-inputs AND cells to obtain the total active energy related to 2-inputs AND cells in the Cortex-M0+.

Finally, these steps must be repeated for every required logic gate and added together to obtain the total average leakage power consumption and the total active energy consumption of the Cortex-M0+.

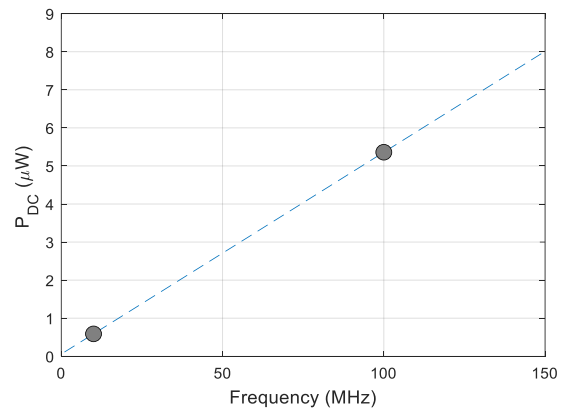


Fig. 9. Power consumption of the HCMOS9A 2 inputs AND versus switching frequency for active energy estimation.

C. Results

Table II summarizes the synthesized Cortex-M0+ processor performances in terms of average leakage power, active energy, area, and price for the three considered technologies. Indeed, this methodology allows not only to estimate the power dissipation, but also the area of the chip since the area of every standard cell used in the Cortex-M0+ is known. Thus, it can be seen that, as expected, the surface reduction factor is proportional to the square of the minimal channel length reduction factor.

Moreover, it appears that FDSOI guarantees the smallest size for the pacemaker CPU chip and the minimal active energy for a supply voltage of 0.8 V. However, CMOS065, which has a lower manufacturing price, leads to the lowest leakage power consumption. Nevertheless, depending on the number of operations required by the pacemaker algorithm, the CMOS065 and the FDSOI technology can be the optimal choice in terms of power consumption.

TABLE II. CORTEX-M0+ TECHNOLOGIES BENCHMARK AT 27°C

	Average leakage power (nW)	Active Energy ($\mu\text{W}/\text{MHz}$)	Area (mm^2)	Price ($\text{€}/\text{mm}^2$) ¹
HCMOS9A 130 nm (1.2 V)	300	398	1.97E-01	2,500
CMOS065 65 nm (1 V)	136	49.9	3.99E-02	4,500
FDSOI 28 nm (1 V)	486	20.3	9.34E-03	9,000
FDSOI 28 nm (0.8 V)	180	8.22	9.34E-03	9,000

1: EuroPractice IC schedules & prices 2021

IV. TEMPERATURE EFFECT

All the results obtained in Table II are simulated at 27 °C. However, pacemakers are implanted in human body, which has an internal temperature regulated around 37 °C and temperature can affect the leakage power consumption. For this reason, the power consumption of the Cortex-M0+ has been extracted at 37°C for the three technologies. Results presented in Table III show an increase of the average leakage power of 30.3% for the HCMOS9, 54.4% for the CMOS065, and 47.8% for the FDSOI technology. The active energy has increased too but with a smaller amount (0.5% for the HCMOS9, 8.21% for the CMOS065, and +0.98% for the FDSOI technology). Thus, it appears that the average leakage power obtained with the CMOS065 technology and the active energy obtained with the FDSOI technology for a supply voltage of 0.8 V are the most temperature sensitive consumptions. Nevertheless, the CMOS065 technology seems to stay the best compromise.

V. CONCLUSION

In this paper, a method to estimate ARM-based processor power consumption and area at the gate level (and also before silicon implementation) has been proposed and applied to three different manufacturing technologies from STMicroelectronics. Considering a temperature of 27°C, the average leakage powers consumed by a Cortex-M0+ for HCMOS9A (1.2V), CMOS065 (1V) and FDSOI (1V) technologies are respectively 300 nW, 136 nW and 486 nW

and the active energies are respectively 398 $\mu\text{W}/\text{MHz}$, 49.9 $\mu\text{W}/\text{MHz}$ and 20.3 $\mu\text{W}/\text{MHz}$. About the surface, it has been shown that, as expected, the surface reduction factor is proportional to the square of minimal channel length reduction factor.

However, leakage power and active energy of a FDSOI Cortex-M0+ can be highly improved, until obtain similar results, in terms of average leakage power, by reducing the supply voltage to 0.8 V. Nevertheless, the FDSOI 28nm technology offers other ways to reduce average leakage power and active energy such as the reverse body-biasing (RBB) [8] which allows to tune the MOS threshold voltage at the cost of chip complexity.

Moreover, temperature effect has been studied and it has appeared that average leakage power is very sensitive to temperature. Indeed, an increase of 10 °C has led to an average leakage power increase between 27.7% and 54.4%. Thus, designers must really consider the human body temperature when the studied chip operates in an implantable device such as a pacemaker.

Finally, regarding the power consumption, the area, and the price criteria, the CMOS065 seems to be the technology which offers the best compromise regarding power dissipation, area, and cost.

TABLE III. TEMPERATURE EFFECT ON STATIC AND DYNAMIC POWER CONSUMPTION

Temp.	27°C		37°C	
	Average Leakage Power (nW)	Active Energy ($\mu\text{W}/\text{MHz}$)	Average Leakage Power (nW)	Active Energy ($\mu\text{W}/\text{MHz}$)
HCMOS9A (1.2 V)	300	398	391 (+30.3%)	400 (+0.50%)
CMOS065 (1 V)	136	49.9	210 (+54.4%)	54.0 (+8.21%)
FDSOI (1 V)	486	20,3	621 (+27.7%)	20.5 (+0.98%)
FDSOI (0.8 V)	180	8,22	266 (+47.8%)	9.35 (+13.7%)

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