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Abstract

This paper introduces the concept of a new packaging concept, TAPIR, compacT and modulAr Power modules with IntegRated cooling in an improved version. In comparison with the first generation, the manufacturability, disassembly for easier end of life processing and expected reliability have been targeted. However, these modifications lead to a change in the electrical path of the switching cell, which might increase the stray inductance of the power module. This work therefore proposes a deep investigation of all geometrical parameters involved in the TAPIR#2 design, in order to estimate if the increase of the stray inductance is acceptable. All results will be very helpful for a global design including the trade-off between electrical, thermal and mechanical behaviours.

1 Introduction

Wide bandgap power semiconductor materials such as Silicon Carbide (SiC) bring possibilities for technological breakthroughs, achieving switching speeds much faster than the equivalent devices in silicon. This allows reducing losses and/or manufacturing more compact converters. The drawback of this outstanding speed is that conventional packaging developed for usual silicon devices actually limits the semiconductor performances. First, the stray inductances of switching cells must be dramatically reduced (nanohenry requirement [1]) to avoid voltage overshoots and ringing. Second, the reduction of semi-conductor size for the same current rating increases the heat density in comparison with silicon devices. To overcome limitations of classical power electronics packaging based on 2D assemblies, alternative power module structures have been proposed by numerous research groups. States of the art of new assemblies are given in [2-5].
Thus, design of power modules for high switching speed devices relies on global trade-off between effective thermal management and adapted 3D layout. This trade-off must consider other constraints like electrical insulation and reliability. Additionally, other parameters such as manufacturability, modularity and end-of-life should be considered.
On a thermal point of view, the main design objectives are the limitation of the maximum junction temperature and the management of thermal transients. The reduction of the junction temperature can be done by:
- reducing the number of thermal interfaces,
- cooling the devices on their both sides,
- spreading the heat close to chips,
- placing the devices as far as possible from each other in the volume of the assembly…

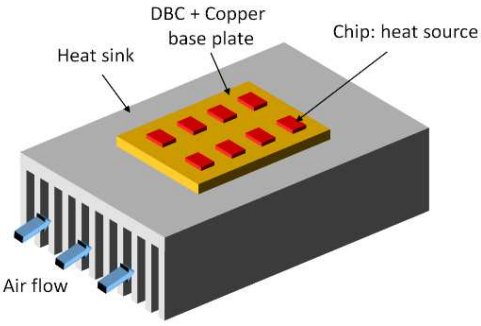
On the other hand, the 3D layout must allow reducing voltage spikes during switching and electromagnetic interferences (EMI). Ideally, the architecture should provide copper tracks with:
- low parasitic inductance,
- adapted stray capacitances to limit EMI, and to not slow down switching events,
- balanced parasitics in switching cells [6]

To limit stray inductance of switching cells, it is also recommended to include decoupling capacitors inside assemblies.
It can be seen that some requirements for thermal management and layout are contradictory. It is the case of the distance between chips which must be as far as possible for reducing the temperature but as close as possible to limit the stray inductance. Bikinga et al. [7] proposed a power module architecture called TAPIR (compacT and modulAr Power modules with IntegRated cooling) to manage this trade-off. This solution allows spreading heat sources in the entire volume of the converter by keeping low stray inductances of switching cells. This solution also allows reducing the number of thermal interfaces, the spreading of the heat and the balance of parasitics thanks to a flip-chipped arrangement of the dies in the switching cell.
The aim of this paper is to propose a new architecture based on the TAPIR concept but which can be easily manufactured and disassembled, and which provides more flexibility for building any converter topology. This new generation of TAPIR will be presented in section 3, the first generation being reminded in section 2. In particular, in the proposed solution, the distance between chips of the same switching cell is increased. Thus, the loss of performance in term of stray inductance is deeply analysed in this paper (sections 4-5).

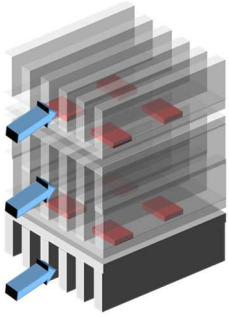
2 TAPIR: Architecture of the 1st Generation

Fig. 1a presents the classical implementation of a power module assembled on an air heat sink. The heat sink area is generally higher than the one of the power modules in order

to improve convection heat transfers. Fins or equivalent solutions are also used to increase the heat exchange surface. By only focusing on thermal issues, this assembly presents several drawbacks:
- the heat dissipation is not well distributed on the heat sink area,
- there are a lot of thermal interfaces.
On a thermal point of view, Fig. 1b shows the ideal solution with a global integration of power dies inside the volume of the system which allows reducing the size of the cooling system. However, it is necessary to consider electrical issues for this type of implementation. The TAPIR architecture aims to propose a solution for that.



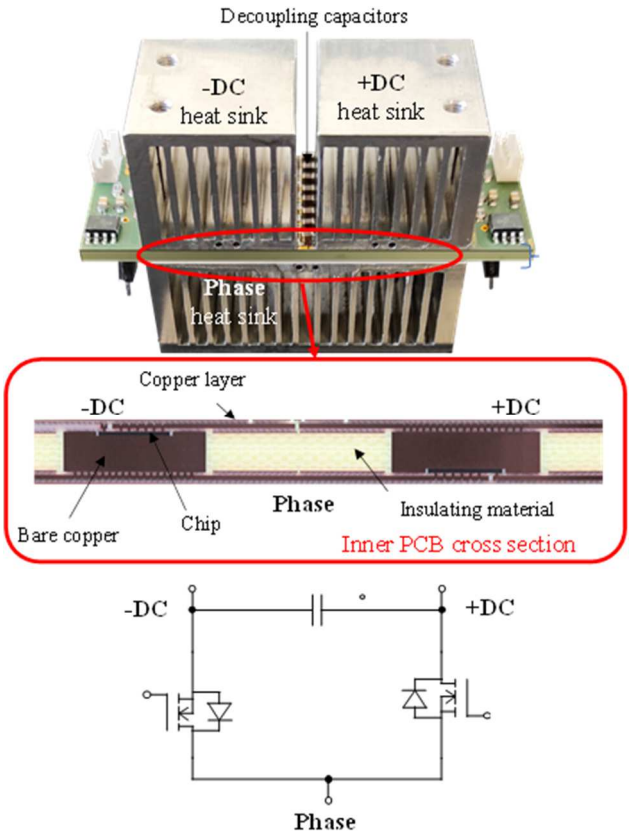
a. Classical 2D implementation



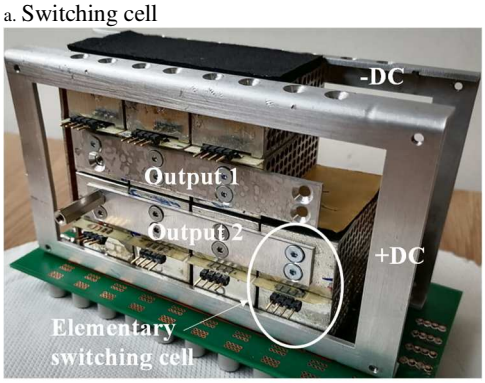
b. Full 3D integration

Figure 1 Classical implementation of power modules on heat sinks vs 3D integration of dies inside the volume of the system

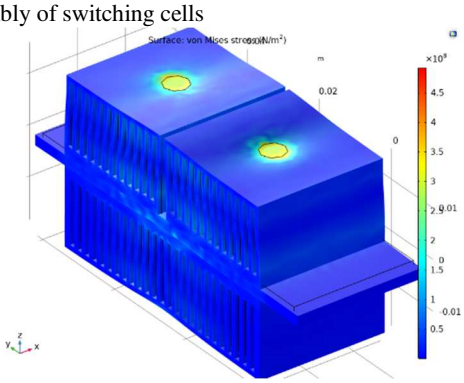
As seen in Fig. 2, the TAPIR assembly is based on a modular arrangement of 3D switching cells. An example of one switching cell is presented in Fig. 2a: the power electrical connections are achieved by the heat sinks and the power devices are embedded in a PCB between them. Thus, there is no insulating material between the heat sinks and the devices which are cooled on their both sides. As a consequence, the thermal resistance can be quite low and reach values comparable to thermal resistances obtained with water cooling as shown in [8]. Also, decoupling capacitors can be integrated between +DC and -DC heat sinks. It is demonstrated in [9] by an experimental setup that the stray inductance of this switching cell is close to 1.5 nH which makes it compatible with the use of fast switching devices. At system level, the switching cells are assembled each other in a 3D structure to make the global power module with integrated cooling. Fig. 2b proposes a possible implementation technique where the switching cells are screwed on massive metal parts which act as power connections inside the converter.



a. Switching cell



b. Assembly of switching cells



c. Illustration of deformations and mechanical constraints during thermal cycling due to the non-symmetrical arrangement

Figure 2 Modular arrangement of 3D switching cells

Despite its advantages, the initial design presents a few challenges, namely:
- high thermo-mechanical constraints due to large solder surfaces and switching cell attachment on massive metal

parts; deformations during thermal cycle due the non-symmetrical arrangement (Fig. 2c),
- thermal disequilibrium exists between switching cells due to the air flow direction,
- the embedded die technology used as a prepackage for the inverter leg involves two flipped chips, which is a technical challenge in itself,
- the global assembly of the switching cell on the PCB embedded dies necessitates several synchronous soldering: decoupling capacitors, connectors, heat sinks, with various requirements due to different sizes,
- having two dies embedded in the same PCB is suitable to build inverter legs, but the whole process must be modified if other topologies should be obtained (for instance multi-level converters),
- if one die fails during manufacturing or operation, the full switching cell must be discarded. This is a serious problem in terms of electronic waste, and will become major issue in the near future [10].

In order to mitigate all these issues, another technique to implement the TAPIR solution is proposed and presented in the next section.

3 TAPIR: Architecture of 2nd Generation

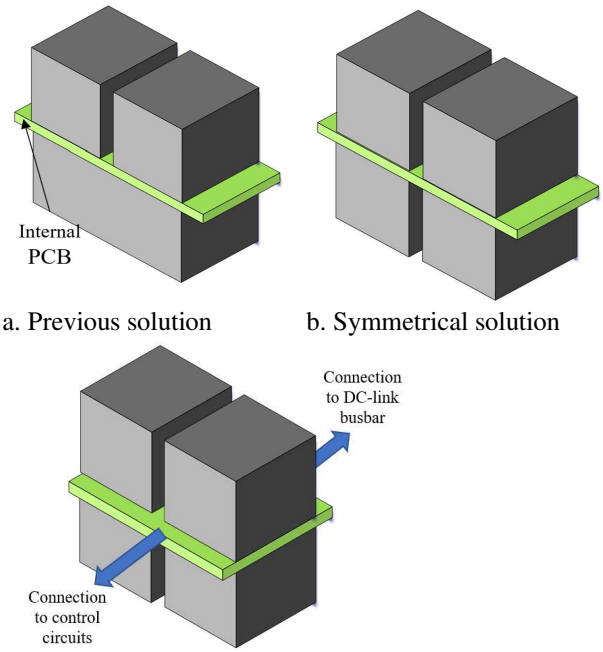
3.1 Reduction of thermo-mechanical constraints

Fig. 3a presents roughly the previous switching cell arrangement where heat sinks are represented by massive grey parts. To reduce deformations during thermal cycling, it is proposed to implement a symmetrical configuration of heat sinks as shown in Fig. 3b. Also, it is decided to not make the electrical connections via the heat sinks in order to reduce mechanical constraints inside the structure as it was done in Fig. 2b. The electrical connection between the switching cells and their environment is now done via the internal PCB. The shape of this PCB is therefore modified (Fig. 3c): one side is used for electrical connection to the DC-link busbar and the other is used for connection to control circuits. Fig. 4a shows how these new switching cells could be assembled.

3.2 Thermal management constraints

As explained before, one issue related to previous TAPIR implementation is thermal unbalance between cells. It is especially the case if the air flow direction is the same in all heat sinks as shown in Fig. 4b. To solve this problem, it is possible to use an alternate air direction on both sides of internal PCBs as shown in Fig. 4c. However, it can be noted that the increase of heat sink number is one drawback of this solution which could have a negative impact on global reliability.

In Fig. 4b, 9 switching cells are represented. It could be for example the implementation of a 3-phase inverter with 3 switching cells in parallel by leg. In this configuration, the air flow crosses 6 heat sinks successively that could induce very high pressure drops. Therefore, a modification of the heat sink shape is also proposed in Fig 4c for reducing pressure drops with constant heat sink volume. This new rectangular shape also allows reducing the parasitic inductance of switching cells because dies are closer to each other. Fig. 4c presents a more realistic implementation of this assembly.



a. Previous solution b. Symmetrical solution

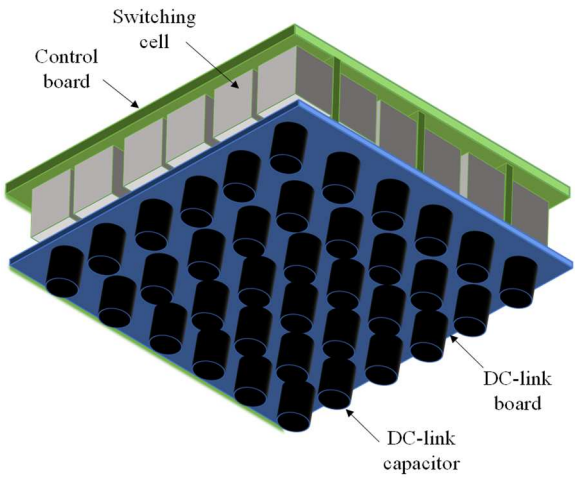
c. Modification of the internal PCB

Figure 3 Evolution of the switching cell geometry

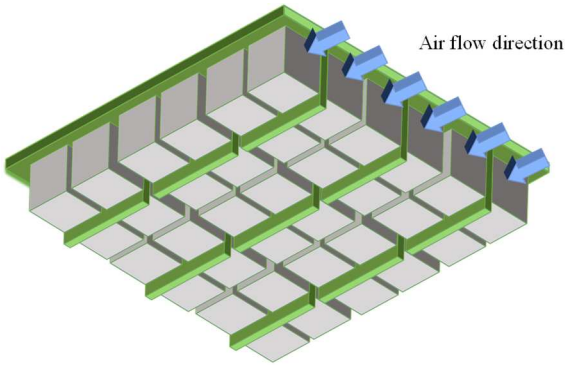
3.3 Switching cell implementation

Fig. 5 compares the former integrated switching cell cross section (Fig. 5a) with the new proposed implementation (Fig. 5b). In the first one, both semiconductor devices of the switching cell are integrated in the same internal PCB. In the second, each semiconductor device is embedded in a prepackage composed of an individual internal PCB with two heat sinks soldered on its both faces. Each prepackage is maintained by pressure between two PCBs called “mother boards”. These boards include the electrical connections to the DC link busbar and the control board. It also includes decoupling capacitors. Holes are made in mother boards to allow the heat sinks to pass through.

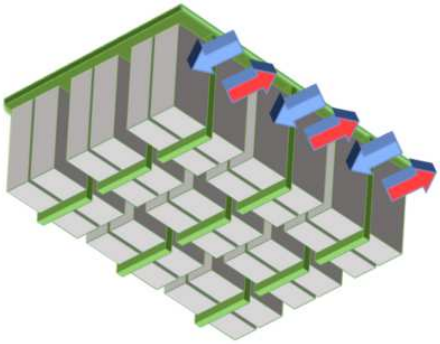
The electrical contact between each individual PCB and the mother boards is done with electrical interface materials (EIM). They could be for example metal foams or other massive or deformable materials. A sealing gasket is used to limit air leaks and help voltage withstand in the system. With this new configuration, the soldering process is easier because the heat sinks are not soldered on the same PCB than electrical connectors and decoupling capacitors. Also, it allows more flexibility concerning the converter topology since this arrangement makes it possible to fabricate other switching cell types. The use of external pressure to assemble prepackages and motherboards is used to facilitate the disassembly process. However, due to this choice, the surface of the switching loop is increased which induces a necessary stray inductance increase. Thus, next sections of the paper aim to evaluate the impact of this choice by comparing the stray inductances of the previous TAPIR structure with the new one.



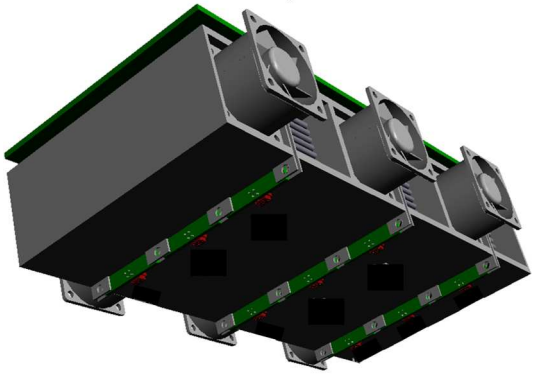
a. Assembly of switching cells



b. Same air flow direction



c. Alternate air flow direction and modification of heat sink shape



d. Possible physical implementation

Figure 4 Power module architecture to reduce thermomechanical constraints and thermal unbalance

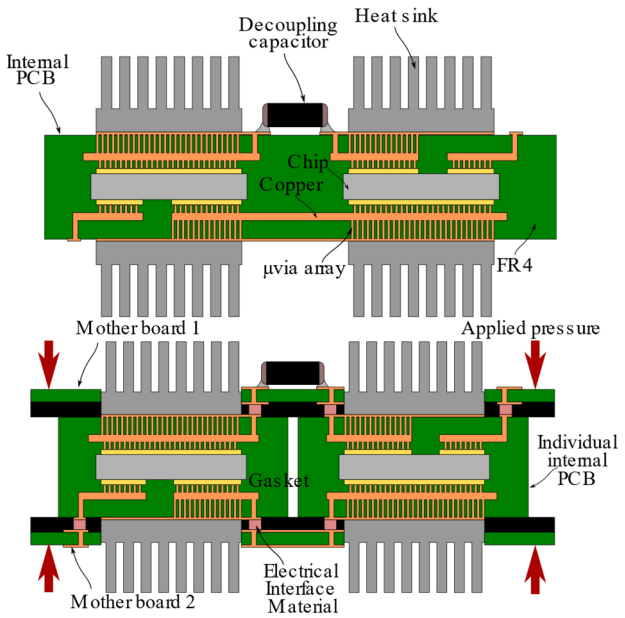


Figure 5 Cross section of TAPIR switching cells (Top: Gen 1, Bottom Gen 2)

4 Numerical Modelling

The geometries of the TAPIR generation 1 and 2 are presented in Figure 6, where the main components are set apart in the z-axis merely to clarify the structure. Generation 1 is the integrated solution and thus only Fig. 6(a) is needed to represent the whole power module, with two semiconductors. Fig. 6(b) presents the TAPIR Gen. 2 module with a single semiconductor whereas Fig. 6(c) presents the whole TAPIR Gen. 2 solution, with two modules and two motherboards.

In Fig. 6(a), four geometrical variables, namely the inner PCB thickness, the microvia thickness, the microvia width and the semiconductors spacing, are highlighted. More details about these variables are given in later subsections. The geometry of the model used for the electromagnetic simulation is further simplified by removing the heatsinks. This rather large conductor volume does not alter significantly the numerical results since high frequency currents do not flow throw it, as verified in previous work [7]. PCB power tracks and control circuitry are not precisely represented as their impact on the stray inductance is negligible. Finally, the semiconductors and decoupling capacitors are modelled as massive copper conductors with a very fine cut (100µm) along the main current flowing direction. This cut allows the introduction of lumped circuit elements between the confronting surfaces, such as capacitors and resistors, and impedance probe for capturing the relevant behaviour in a large frequency range.

Fig. 6(b) presents the TAPIR Gen. 2 module where the EIM can be clearly seen in red.

In Fig. 6(c), two TAPIR Gen. 2 modules are combined with two motherboards through external pressure to create the complete system. Two additional geometrical variables are underlined, namely the decoupling capacitor width and the EIM thickness. The same aforementioned simplifications related to the heatsinks, the fine cuts and PCB tracks are adopted in this electromagnetic model.

The simplified geometries of TAPIR Gen. 1 and Gen. 2 are meshed using Flux3D [13] and solved by MIPSE, an in-house software based on volume integral method [11,12]. The software computes the electromagnetic fields assuming a magneto-harmonic regime and neglecting capacitive effects between the massive conductors. The main advantage of the volume integral method when compared to the typical finite element method is that the air does not need to be meshed, which greatly reduces the size of the problem.

The goal is to compute the stray inductance of the switching loop at an appropriate frequency. The frequency must be high enough to avoid undesired influence from resonant effects of the decoupling capacitors and low enough to be coherent with the magneto-harmonic regime considered and not affect computational performance. Moreover, the phenomenon of overvoltage in the semiconductors is closely related to the rising time of the semiconductor. In the SiC case, it lies in the dozens of MHz range. Thus, the frequency of 100 MHz was found to be appropriate, even though any value between 10 MHz and 500 MHz would produce similar results.

At this frequency, currents are assumed to flow mainly at the surface of the conductors and further computational performance gains can be obtained by considering the surface impedance boundary condition [11]. Once the electromagnetic fields are computed, the inductance is calculated as the imaginary part of the voltage across a unity current source placed inside a fine cut of one of the semiconductors (this corresponds to an impedance probe).

Figure 7 presents a 2D view of the power module with its corresponding circuit schematics for inductance measurement. It highlights the insertion of lumped components in the fine cuts as well as the approximate electric current path.

5 Results

The results of the stray inductance relative to the variation of geometrical parameters are presented in subsections 5.1 to 5.6. In each scenario, the variations are carried out for all identical components to keep the problem's symmetry. Table I presents the nominal values from which the variations are based (parameter names refer to Figure 6).

5.1 Inner PCB thickness

The inner PCB thickness is an important parameter for the module designer. It consists of not only the semiconductor thickness but also all the eventual copper vias necessary for electrical circuitry and thermal dissipation path.

Figure 8 presents the variation of the inductance due to an increase in inner PCB thickness, from 500µm to 2000µm. It is clear that the global behaviour of the inductance is linear in both TAPIR generations, at least in the range considered, with a very close nH/mm ratio. Since the structure of TAPIR Gen. 2 is more complex than Gen. 1, with extra conductor plates, microvias and EIM, it was expected a higher stray inductance. The results show that this additional inductance is on the order of 0.4nH for each point computed.

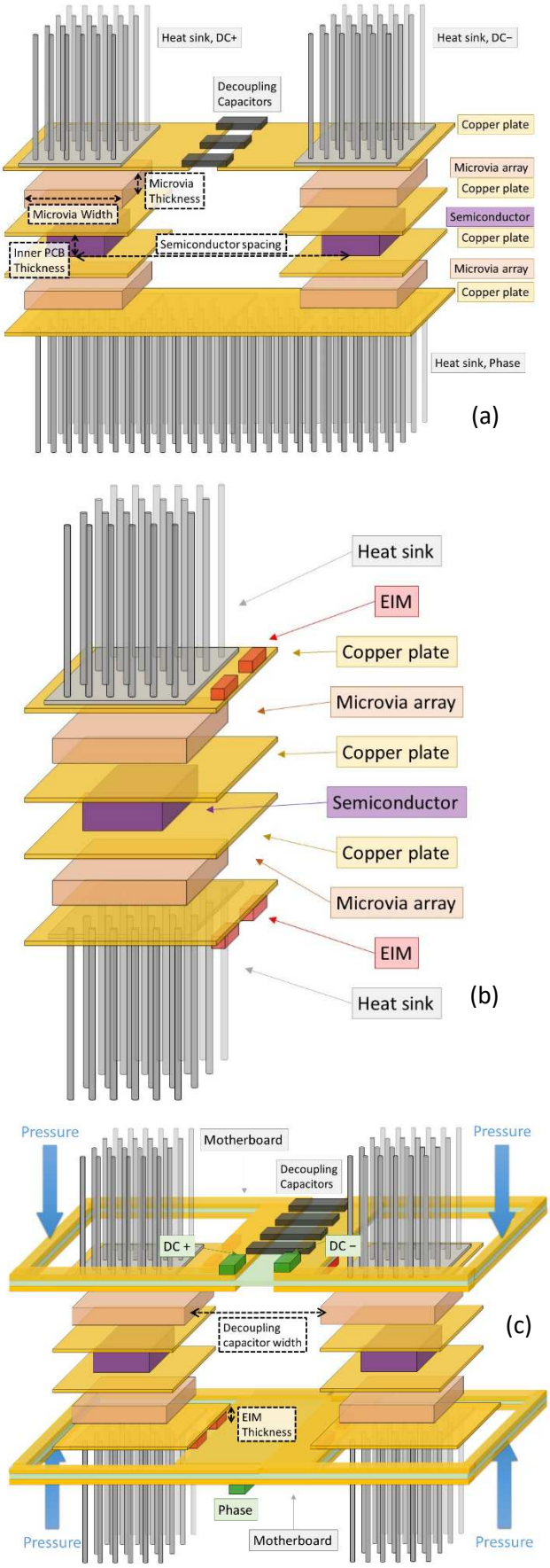


Figure 6 (a) TAPIR Gen. 1, (b) TAPIR Gen. 2 (module) and (c) TAPIR Gen. 2 (module and motherboard)

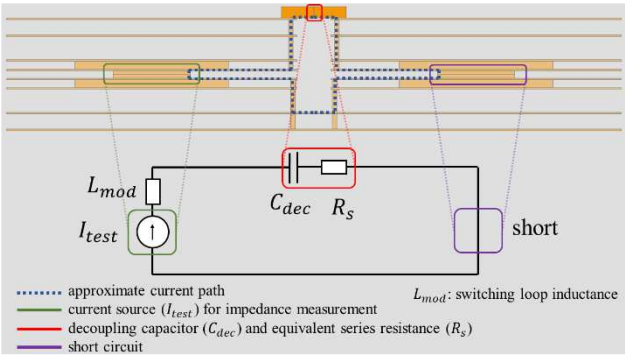


Figure 7 2D view and schematics of the power module

Table I Nominal values of geometrical parameters

Parameter	Nominal value
Inner PCB thickness	1000 µm
Microvia thickness	500 µm
Semiconductors spacing	40000 µm
Microvia width and length	10000 µm
Decoupling capacitor width	600 µm
EIM thickness	1000 µm

5.2 Microvia thickness

The microvias above and below the semiconductors serve mainly two purposes: provide the required electrical path for power and control, and provide a low thermal resistance path to the heat sinks for the heat generated by the semiconductors. Their width can be adjusted by the power module designer based on the electrical and thermal requirements and thus an evaluation of this parameter is necessary. Figure 9 presents the variation of the inductance due to an increase in microvias (below and above) thicknesses, from 300µm to 1100µm. Again, the global behaviour is linear in both cases, however the ratio nH/mm is considerably higher in the TAPIR Gen. 2. This is clearly not a concern, since the stray inductance in all cases is lower than 1nH. The sensitivity of the inductance to the microvia thickness is much lower when compared to the inner PCB thickness. Finally, the results show that TAPIR Gen. 2 presents on average a 0.42nH increase on the stray inductance.

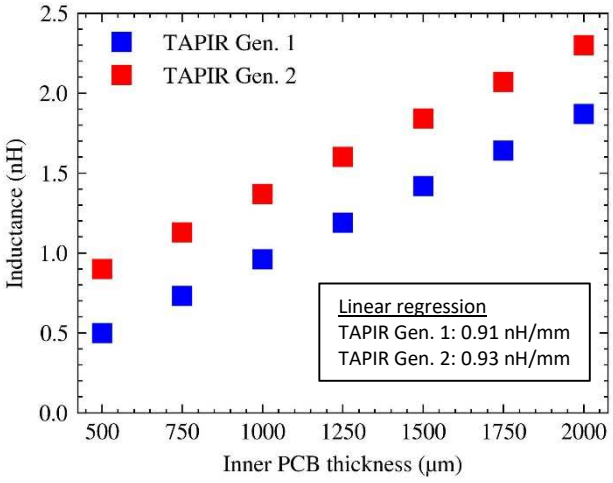


Figure 8 Inner PCB thickness – stray inductance variation

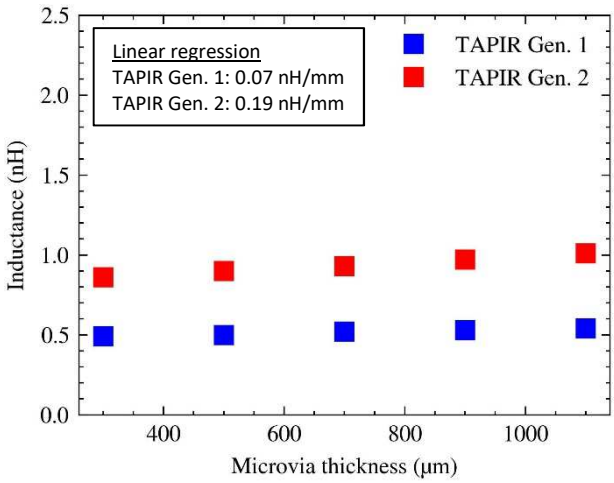


Figure 9 Microvia thickness – stray inductance variation

5.3 Semiconductors spacing

The semiconductors spacing is a critical geometrical parameter. Ideally, the semiconductors would be placed as close as possible to each other in order to minimize the stray inductance. However, mechanical, thermal and electrical constraints prevent this parameter from being arbitrarily small. The semiconductors spacing determines directly the whole system size and the allowed heat sink size. Figure 10 presents the variation of the inductance due to an increase in semiconductors spacing, from 40mm to 100mm. Once more a linear behaviour is observed in both TAPIR generations, with both nH/mm ratios being similar. The average increment in inductance from Gen. 1 to Gen. 2 along the range considered is 0.45nH.

5.4 Microvia width and length

The microvia width and length may be varied by the power module designer in order to accommodate all the necessary electrical connections and to achieve a desired thermal resistance. Therefore, the effect of this parameter value on the stray inductance must be considered.
It was found that there is no correlation between the microvia width and length, and the stray inductance.

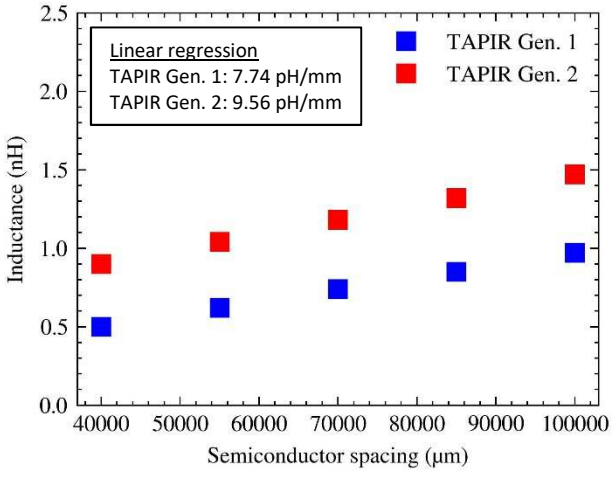


Figure 10 Semiconductors spacing – stray inductance variation

5.5 Decoupling Capacitor width

The decoupling capacitor width is a parameter related to the capacitor packaging. Depending on the results of the decoupling capacitor sizing, it may be necessary to employ smaller or larger components. Consequently, the power module designer must know in advance the effect of increasing the available space for decoupling capacitors.
Figure 11 presents the variation of the inductance due to an increase in decoupling capacitor width, from 600µm to 6600µm, for the TAPIR Gen. 2 only. A linear behaviour is observed with a 0.08nH/mm ratio.

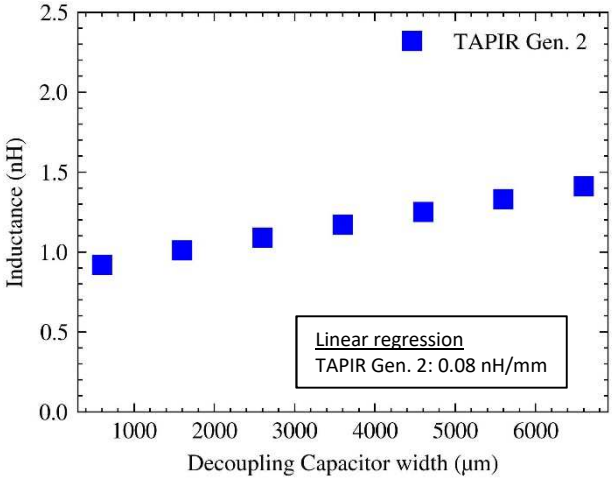


Figure 11 Decoupling capacitor width – stray inductance variation

5.6 EIM Thickness

The electrical interface material thickness is a crucial geometrical parameter. Many different solutions for pressed contact exist, such as spring or copper foam. For that reason, the thickness of the EIM cannot be determined before the choice of technology.
Figure 12 presents the variation of the inductance due to an increase in EIM thickness, from 100µm to 1500µm, for the TAPIR Gen. 2 only. Once again, a linear behaviour is observed. Moreover, in this range, a minor impact of 0.2nH per additional millimeter on the stray inductance is noticed.

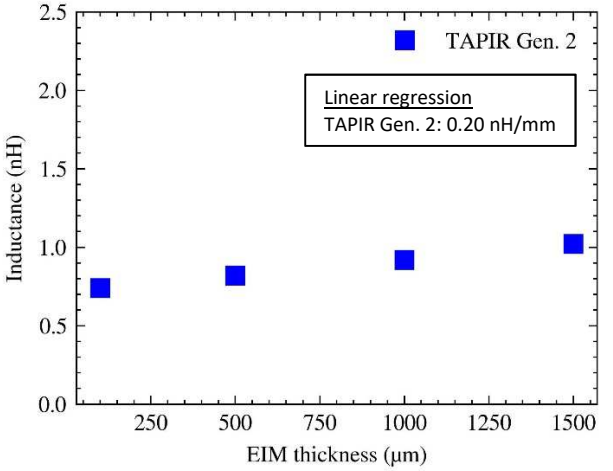


Figure 12 EIM thickness – stray inductance variation

6 Conclusion

This paper presented a new power module concept, denominated TAPIR generation 2, which was conceived to improve modularity and reduce fabrication complexity when compared to generation 1.
These two advantages of TAPIR generation 2 were achieved through the addition of two extra PCB layers and EIM pressed contacts, which increase the switching loop stray inductance. These parameters play a major role on the semiconductors overvoltage and thus requires to be assessed on this new structure.
This work, in particular, drew attention to the computation of the stray inductance of TAPIR Gen. 2 and the comparison to Gen. 1. The results showed that indeed the stray inductance of Gen. 2 is higher than Gen. 1 but not excessively i.e. not more than 0.4 nH. Therefore, TAPIR Gen. 2 seems a realistic concept, with the great advantage of being modular and easier to fabricate compared to Gen. 1.
A sensibility analysis was presented and allows the power module designer to carefully size the proposed power module geometry, minimizing overvoltage. On a final note, the EIM pressed contacts not only allow easier assembly but also easier disassembly. This feature enables the replacement of a single module in case of failure, extending the system's lifetime, and reduces recycling effort and cost. TAPIR Gen. 2 is therefore not only more modular but also eco-friendlier.

Acknowledgment

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