# Design and experimental validation of a SoC-FPGA based compact NQR Spectrometer

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***Abstract*—Nuclear Quadrupolar Resonance (NQR) is a radio frequency spectroscopy technique providing high resolution molecular analysis of solid materials containing quadrupolar atomic nuclei. The NQR technique does not necessitate an external magnetic field and, therefore, permits a large number of applications; it nevertheless suffers from relatively low sensitivity. The challenges of NQR instrumentation are therefore to increase its portability and sensitivity, and to limit interference from various noise sources (e.g., radio frequency interference) in order to perform field applications outside the laboratory. To address these challenges, we present a System-on-Chip Field-Programmable Gate Array (SoC-FPGA) based portable spectrometer integrating the major hardware elements of NQR instrumentation. These include : a high pulse width resolution pulse programmer, a fully controllable pulse transmitter, an acquisition module that performs detection, digital signal processing and storage of the acquired signal in an external memory, in addition to a hardware debugger. Pulser and acquisition Linux applications are embedded on the SoC-FPGA. While many recent compact spectrometers still have crucial radio frequency (RF) parts in the analog domain and lack performance optimization, most of our hardware and software modules are digitally implemented on SoC-FPGA. The designed portable spectrometer was successfully tested by detecting the expected frequencies of several samples such as $NaNO_2$, $HMT$ or $1,3,5-TCB$ covering hence the typical $^{14}N$ and $^{35}Cl$ NQR frequency ranges.**

***Index Terms*—NQR instrumentation, Sensitivity, SoC-FPGA, RTL design, Experimental validation.**

## I. Introduction

NQR is a spectroscopy technique that was discovered in the year 1949 by H. Dehmelt and H. Krueger when studying nuclei with a spin superior to 1/2, like $^{127}I$, $^{35}Cl$, and $^{14}N$. In NQR, the quadrupolar interaction is responsible for the nuclear spin polarization, as opposed to Nuclear Magnetic Resonance (NMR), where the quadrupolar interaction is treated as a perturbation of the Zeeman interaction. The two techniques are, therefore, complementary, since NQR is sometimes more suited for the study of systems containing nuclei with strong quadrupolar interactions [1]. When the nuclear quadrupolar moment interacts with the surrounding electric gradient, the nuclear energy splits into degenerate energy levels, which can be populated by the absorption or emission of RF signals at the characteristic NQR frequencies (Fig. 1). If the energy of an electromagnetic wave is equal to the difference between two levels, the wave can be absorbed by the nuclei. The return of the spin to the equilibrium state liberates an electromagnetic wave whose frequency is characterized by the energy level difference. This wave, when detected by a probe, corresponds to the NQR signal or Free Induction Decay (FID). As indicated in Fig. 1, the signal frequencies depend on the quadrupolar coupling constant $C_Q$ and the asymmetry parameter $\eta$, which define the Electric field gradient (EFG) around the nucleus. Hence, the frequency of the received signal returns the information about the structure of the studied molecule. The NQR technique offers a wide range of applications, such as the detection of explosives (especially landmines), illicit materials like narcotics, medicine counterfeits, and the structural analysis of functional materials that would greatly benefit from compact portable characterization tools [2], [3]. For these specific applications, NQR is particularly well-suited due to the fact that its instrumentation is less bulky than that of NMR, as it doesn't necessitate an external intense magnetic field. However, because the targeted frequencies of these applications are very low compared to NMR (typically less than 60 $MHz$), the NQR signal is very weak and susceptible to noise and radio-frequency interference, which makes its instrumentation very challenging, especially for portable NQR spectrometers.

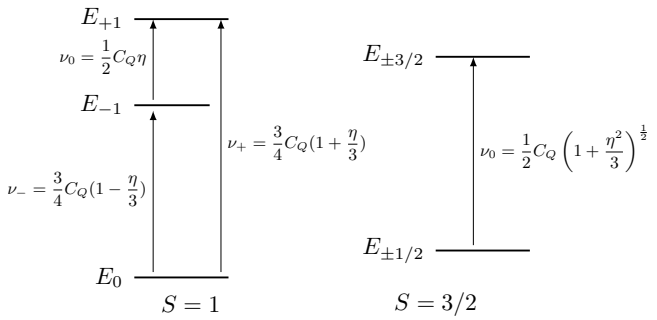


Fig. 1: Splitting of the quadrupolar energy levels of a spin 1 nucleus (left) and spin 3/2 nucleus (right), with allowed transitions and corresponding resonant frequencies $\nu_0, \nu_+, \nu_-$ (e.g. $^{14}N$ and $^{35}Cl$)

The literature describes several portable and miniature spectrometers, many of which were developed using ASIC technology to achieve high levels of miniaturization [4]–[21]. These ASIC-based NQR spectrometers offer advantages in terms of miniaturization and delivering acceptable sensitivity. However, their limitations include reduced flexibility, longer time-to-market due to development challenges, and higher costs associated with their specialized design and production processes. Of particular interest among portable spectrometers

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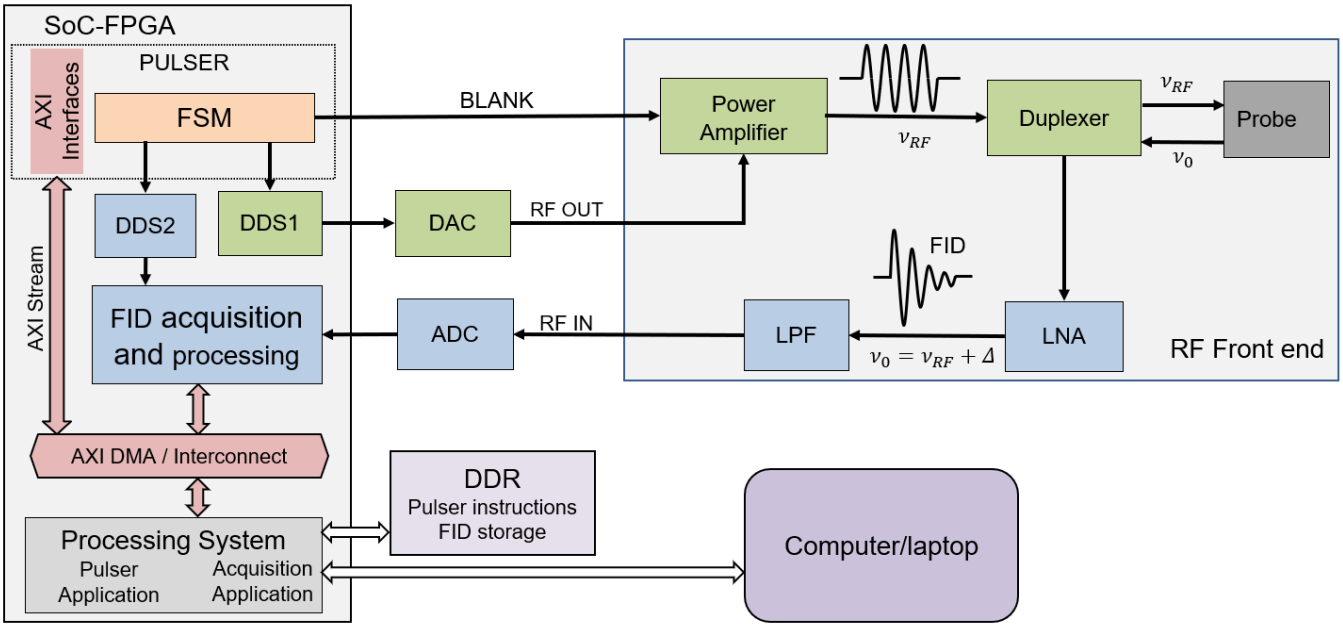


Fig. 2: The NQR compact spectrometer is structured with a system-level architecture, including key components such as the analog front-end, analog to digital and digital to analog interfaces, a SoC-FPGA managing hardware digital signal processing, along with embedded software applications for received FID. The details of the content of SoC-FPGA are given in Fig. 3. The communication with the host PC is performed using Ethernet. The host PC is used for running post-processing and GUI software. The post-processing software includes typical NQR signal treatment like apodisation, baseline correction, FFT and phase correction.

are those that integrate all main functionalities inside the digital domain on FPGA with high levels of integration and miniaturization. Some portable spectrometers use FPGA as the basis for integration of almost all functionalities [22]–[25]. Other portable and miniature spectrometers were developed using existing standard development platforms, such as Terasic DE0-nano, LMS7002M, and Ettus N200 [26]–[29]. A SoC-based approach was also used in some cases, where the FPGA embeds a hybrid system containing programmable logic and a processor subsystem [30]–[32]. Some researchers developed portable FPGA based NQR spectrometers and simulated real-time post-processing denoising algorithms [33], [34], and incorporated denoising algorithms on FPGA embedded processor [35]. Others designed autonomous self-tuning and adapting FPGA-based spectrometers [30].

Many of the portable spectrometers previously mentioned were designed for portable NMR applications. However, those designed for NQR applications still retained some crucial RF components in the analog domain, which caused problems like noise and artifacts. Even those modules that were designed in digital domain had some limitations (e.g. pulse width resolution) [24], [36]. The primary contributions of this study can be outlined as follows:

- SoC-FPGA solution for enhanced shielding and immunity to external RF noise.
- FPGA-based frequency translation, replacing traditional analog methods.
- Exceptional performance, including an 8 ns pulse width and ultra-broadband readiness.
- Complete digital domain processing pipeline with the capability to embed denoising algorithms, including On-The-Fly accumulation and phase cycling on FPGA.

The structure of the paper is organized as follows : section II provides the details of the proposed portable spectrometer while the results and experimental validation are presented in section III. In Section IV the characteristics and performances of the proposed spectrometer are discussed before the concluding remarks of section V.

## II. Proposed Spectrometer

During an NQR experiment, the nuclear spins are stimulated by RF pulse sequences controlled by a pulse programmer. The excitation RF signal, centered at a frequency of $\nu_{RF}$, is produced by the transmitter and then sent to the probe for irradiating the sample after amplification. As a result, the excited nuclei generates a FID signal containing characteristic frequencies $\nu$, shown in Fig. 1, which are typically in proximity to $\nu_{RF}$. After being pre-amplified by a low noise amplifier (LNA), the FID is acquired by the acquisition module and then post-processed by software. In the proposed compact NQR spectrometer (Fig. 2), many of the traditional analog parts (pulse programmer, excitation module, acquisition module) are replaced by digital blocks implemented on FPGA.

### A. System architecture overview

The transmitter channel is composed of a power amplifier and a phase-cycled RF excitation generated by a digital

module inside the FPGA which contains an internal Direct Digital Synthesis (DDS1) that delivers the frequency $\nu_{RF}$ of the excitation pulse. The DDS1 is phase and frequency-controlled either by the software or by the pulser IP (Intellectual Property) outputs. The pulser IP delivers pulse sequence control signals that can be used also externally via GPIO outputs to drive, if desired, an external acquisition board. The acquisition channel is made up of an LNA (MITEQ AU-1525 [37]) and an anti-aliasing low-pass analog filter before entering the STEMlab 125-14 board [38]. On the STEMlab 125-14 board, the FID signal is digitized by a 14-bit ADC at a sampling rate of 125 MS/s. The signal frequency is then shifted digitally inside the SoC-FPGA and demodulated digitally to generate a 32-bit complex digital I/Q signal via a Digital Down Converter (DDC). The signal is then filtered and decimated by the two cascaded integrator–comb filters (CIC). At the output of the CICs, the FID point is clock-domain converted and stored in the DDR as a 64-bit word, with the imaginary part of the FID point in the 32 MSB bits and the real part in the 32 LSB bits. This storage in the DDR is accomplished using a 64-bit stream width to a 64-bit memory width AXI DMA write channel. The FID is then accumulated and optionally phase-cycled on the SoC-FPGA, read back from the DDR, and sent to the PC through the Ethernet interface.

In addition to the digital hardware components, this compact spectrometer embeds an important software part on SoC-FPGA. It consists of the pulser and the acquisition applications developed to drive the functions of the spectrometer (Fig. 2). It also exploits a previously developed socket-based communication. The user interacts with the spectrometer embedded system by a home-made software [39], [40] that performs all NQR signal post-processing through an upgraded graphical user interface (GUI). Through the graphical menu of the interfacing software, the user can define the desired sequence for his NQR experiment as well as other various parameters of the experiment such as the frequency of the carrier, the number of acquisition points, etc. The proposed compact NQR spectrometer (Fig. 3) is composed of three main modules and an auxiliary hardware detailed in the following subsections.

### B. The pulse programmer

In the proposed NQR spectrometer, the pulser is a home-made digital Intellectual Property (IP) designed in Register Transfer Level (RTL) Language. This module functions as the ”bandmaster” of the spectrometer, receiving pre-generated instructions specific to experiments, already stored in the external DDR. By decoding these instructions, it generates the pulse sequence control signals that drive the RF excitation and acquisition modules. The pulser comprises a Finite State Machine (FSM), a configuration register interface, and an instructions FIFO.

*1) The FSM :* For each experiment, the pulser state machine starts to execute the various 128-bits coded instructions of an experiment and generates the control outputs like the RF modulating pulse signal, blanking, trigger, and phase signals. The control signals are transmitted through the 8-bit output bus TTL_out[7:0] of the pulser. The FSM is a Moore state machine that has 11 states (IDLE, START, BLANK, PULSE, DAMP, DELAI, TRIGGER, ACQUI, SYN1, STOP, ERR-STATE). The output of each state determines the values of the 8-bits TTL_out[7:0] bus that constitutes the outputs of the pulse programmer. The details of Pulser FSM States, Control Signals, and Actions are given in table I.

The inputs of the FSM are the values of the 8-bits opcode word which is derived from the instruction and the values of the counters of the different durations (delay duration, acquisition duration, pulse width duration,...). When the FSM finishes executing a given instruction it anticipates the demand of a new instruction by issuing a request signal to the instructions FIFO (Signal ’Req’ on Fig. 3).

*2) Instructions FIFO :* The pulse programmer instructions are coded on 128-bits words that encompass, the duration value of the state, the opcode, the amplitude, the phase of the pulse and the frequency tuning word. The size of the instructions could be smaller than 128-bits, but for backward compatibility with our internal standard of NMR spectrometers instructions we decided to keep some fields and states (SYN1, amplitude, and FTW fields) even though they are not used in the current NQR spectrometer version. Moreover, in order to balance instructions management task distribution between software and firmware, it was decided that software generates the very low level 128-bits instructions set. The design follows then a straightforward and high performance approach, eliminating the need for a decoder that may cause potential timing issues. This architecture leverages the AXI stream bus width which is 128-bits, the big storage permitted by the DDR and the high throughput afforded by the AXI DMAs usage.

This FIFO is used as a buffer to store temporarily the 128-bits instructions that were fetched by bursts via the DMA from DDR before sending them sequentially to the pulse programmer FSM. The FIFO is designed as an AXI stream with a width of 128 bits and a depth of 128 words. It operates using double synchronous clocks. Each instruction word is composed of fields coded in the way showed in table II.

*3) Registers interface :* The registers interface is used to configure or read the pulse programmer 32-bits registers.

It is a read only register that gives the information about the most crucial signals and events inside the pulse programmer during the execution of a given experiment (start of experiment, end of experiment, error flag, value of the output bus TTL_out[7:0], current scan number). The pulser Linux application performs the writing of the pulser instructions inside DDR at the beginning of the experiment and the programming of the AXI DMA in order to fetch these instructions by the pulser from DDR. It also performs all relevant register and frequency settings of the two DDSs.

When the user launches an NQR experiment, the Linux pulser application begins by fetching the instructions in the DDR via the AXI DMA and stores a part of these instructions in the FIFO.

The pulser IP has an AXI-Lite interface for registers programming and a 128-bits AXI-Stream interface for fetching the pulser 128-bits instructions words that were previously generated by a software and stored in the DDR at the beginning of each NQR experiment. The memory to stream channel

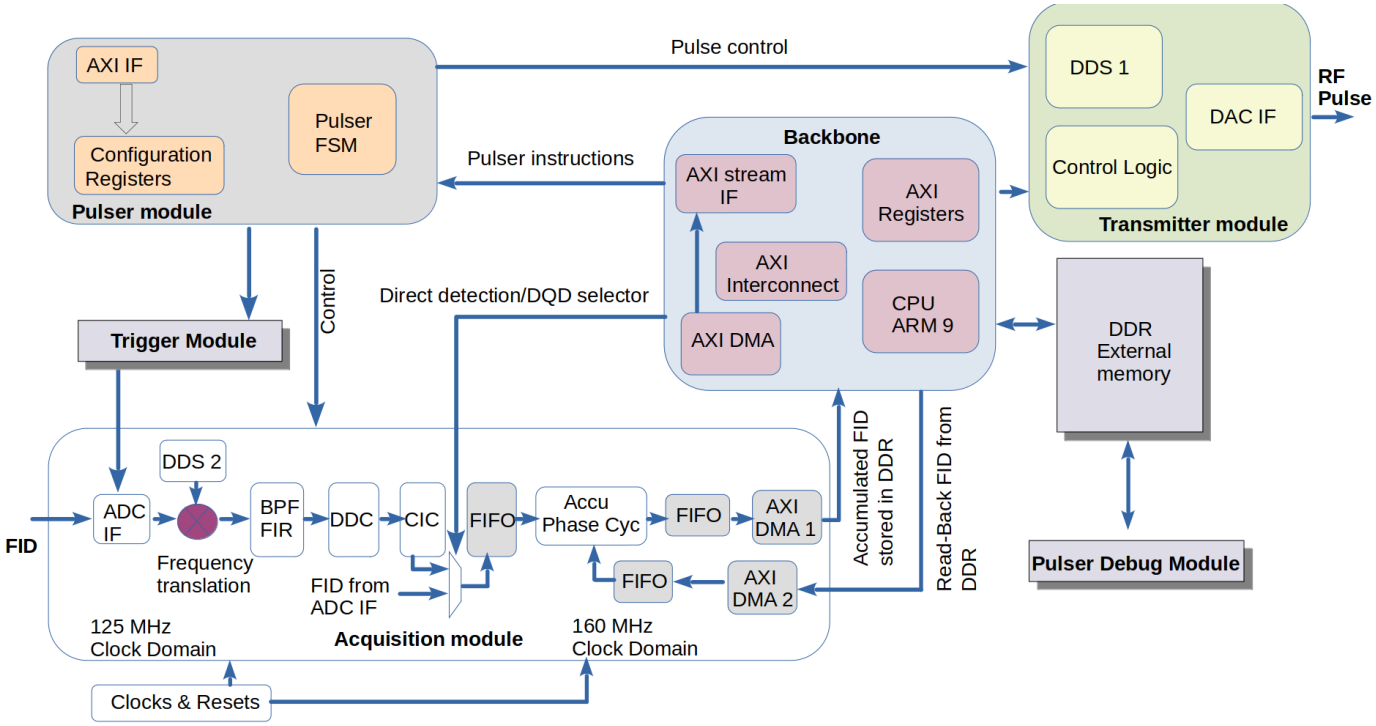


Fig. 3: The figure illustrates the detailed internal micro-architecture of the SoC-FPGA. The top part shows the excitation pulse generation path from the pulser module to the transmitter output. The central backbone module facilitates System On Chip interactions, featuring the ARM9 dual-core and AXI interconnect. The bottom segment depicts the hardware processing path for a received 14-bit digitized Free Induction Decay (FID) until storage in DDR. The acquisition module, incorporating an ADC interface, operates in two clock-domain blocks : a 125 $MHz$ clock-domain with frequency translation, band-pass decimator filter, digital down converter (DDC), and CIC decimator; and a 160 $MHz$ clock-domain for output processing. The transmitter module generates RF pulses, and the trigger module initiates acquisition, while the pulser module controls acquisition duration during each scan.

of the read DMA (AXI DMA 0 on Fig. 3) is used for reading the pulser instructions from the DDR. After writing the size of the transfer into the DMA register that holds the memory to stream transfer size, the pulser starts executing the instructions one by one until the end of the experience. For the integrity of the NQR experience, no dead time is permitted between the execution of instructions. This is enabled by using a DMA-based architecture and a FIFO located inside the pulser AXI-Stream interface.

The first advantage of this pulser (Fig. 3) is that it stores instructions inside the external DDR3 memory. The memory zone for instructions storage can reach 256 MB, which enables a number of up to 16 million 128-bits instructions. This greatly increases the possibility to support complex NQR experiments especially for samples that necessitate a large number of accumulations. For example if we consider only a simple 2D nutation with 100 experiments and 10000 scans each, it would require almost 3 million 128-bits instructions which is equal to a 48 MB memory size. This feature also enhances the portability of the NQR spectrometer by improving its autonomy for storing a very large number of instructions without depending on an external host PC or storage device. This is an additional advantage compared to the state of the art where the storage is done in the internal memory (memory blocks) of the FPGA which limits considerably the number of possible instructions.

The other advantage of this pulser is the high pulse width resolution (8 ns as the minimum pulse width) supplied for pulse sequence programming. Indeed, the minimum pulse width is equal to a clock cycle of the pulser's clock which is 125 $MHz$. This performance is reached thanks to the explained architecture above and especially to the FSM of the pulse programmer. This aspect is not crucial for NQR experiments where pulses typically last several tens of microseconds; nevertheless, achieving high pulse resolution is of interest if the pulser is intended for use in NMR applications where short phase and frequency-shifted pulses are combined in complex sequences.

### C. *Transmitter module*

The transmitter module is based on a Xilinx DDS that is controlled in phase and frequency either directly by the pulse programmer outputs by using the Frequency Tuning Word (FTW on table II) or by software. Indeed the pulse programmer picks up the phase information from the pulse sequence instructions. The phase signals of the pulser are then directly connected to the DDS to control the phase of the output RF pulse. The DDS is also controlled by software by setting the registers that contain the frequency and amplitude

TABLE I: Pulse Programmer Finite State Machine (FSM) States, Control Signals, and Actions.

| Current state | Input (Opcode and counters) | Next State | Outputs(TTL_out[7:0]) | Explanation |
|---|---|---|---|---|
| **IDLE** | Global reset | IDLE or START or SYN1 or BLANK or DELAI or TRIGGER | 0x08 | Initial state. |
| **START** | START counter | SYN1 or BLANK or DELAI or TRIGGER or STOP or ERR_STATE | 0x08 | Waiting state. No action is performed. Delimits the beginning of instructions inside memory. |
| **SYN1** | SYN1 counter | BLANK or SYN1 or DELAI or TRIGGER or STOP or ERR_STATE | 0x08 | Waiting state. No action is performed. Could be used to set RF pulse frequency using FTW. |
| **DELAI** | DELAI counter | BLANK or SYN1 or DELAI or TRIGGER or STOP or ERR_STATE | 0x08 | Waiting state. No action is performed. |
| **BLANK** | Blanking period counter | PULSE or BLANK | 0x28/0x29/0x2A/0x2B | Blanking signal of the PA is active. The LSB bits depend on phase. |
| **PULSE** | PULSE width counter | DAMP or PULSE | 0x20/0x21/0x22/0x23 | Pulse signal is active on low level. The LSB bits depend on phase. |
| **DAMP** | Damping period counter | DAMP or BLANK or SYN1 or DELAI or TRIGGER or STOP or ERR_STATE | 0x48 | Damping signal is active. Issues also internal DDS reset. |
| **TRIGGER** | Lasts one cycle or more until acknowledged | ACQUI | 0x18/0x19/0x1A/0x1B | Trigger flag is active. Increments the scan counter. |
| **ACQUI** | Acquisition delay counter | BLANK or SYN1 or DELAI or TRIGGER or STOP or ERR_STATE | 0x08/0x09/0x0A/0x0B | Acquisition is performed. The LSB bits depend on phase. |
| **STOP** | Lasts one cycle | IDLE | 0x08 | Waiting state. No action is performed. Delimits the end of instructions inside memory. |
| **ERR_STATE** | Lasts one cycle or more until acknowledged | IDLE | 0x08 | Gives flag about a pulser internal error. |

TABLE II: Instructions format

| **State** | **Instruction bits[127:64]** | **Instruction bits[63:56] (opcode)** | **Instruction bits[55:48]** | **Instruction bits[47:40]** | **Instruction bits[39:32]** | **Instruction bits[31:0]** |
|---|---|---|---|---|---|---|
| **IDLE** | Unused | Unused | Unused | Unused | Unused | Unused |
| **PULSE** | Pulse width value | Unused | **Amplitude** | **Amplitude** | **phase** | Unused |
| **START** | Unused | 10101011 | Unused | Unused | Unused | Unused |
| **SYN1** | SYN1 cycles number value | 00000101 | Unused | **FTW** | **FTW** | **FTW** |
| **TRIGGER** | Unused | 00000111 | Unused | Unused | **phase** | Unused |
| **ACQUI** | Acquisition cycles number value | Unused | Unused | Unused | **phase** | Unused |
| **BLANK** | Blanking cycles number value | 00000001 | Unused | Unused | **phase** | Unused |
| **DAMP** | Damping cycles number value | Unused | Unused | Unused | Unused | Unused |
| **DELAI** | Delay cycles number value | 00010000 | Unused | Unused | Unused | Unused |
| **STOP** | Unused | 10111010 | Unused | Unused | Unused | Unused |
| **ERR_STATE** | Unused | Unused | Unused | Unused | Unused | Unused |

information. The amplitude of the RF signal is then adapted by a DAC interface (updated from the Red Pitaya project and P. Demin work [41], [42]) before being sent to the STEMlab 125-14 DAC to generate the RF output excitation signal.

When the user enters a carrier frequency, this value is translated by the pulse programmer application to set the frequency output of the DDS. The user can program frequencies up to $62.5\ MHz$. The DAC interface converts the output digital value of the RF output signals from the 16-bits signed two's complement format to the 14-bits two's complement offset binary format that is required by the DAC used on board. This block serves also to change the amplitude of the RF output pulse by digitally dividing the signal amplitude by powers of two according to the value of the divider set by the user through the GUI.

The first output channel (dac_data_a) is used to transmit the RF output pulse, the second channel (dac_data_b) is used to transmit the blanking signal in analog format to drive the blanking input of the power amplifier.

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### *D. Acquisition module*

The acquisition module detects the digitized incoming FID and performs digital signal processing, including frequency translation, filtering, digital quadrature demodulation, and decimation. The processed FID is then stored inside the DDR using the first AXI DMA, referred to as DMA 1 in Fig. 3. For surface optimization purposes and to achieve a 32-bits

data width for FID instead of 16 bits, we utilized only one acquisition channel, namely channel A. This channel can be easily duplicated to create a dual acquisition pipeline with two channels, A and B. The acquisition module can be programmed to bypass filtering, digital quadrature demodulation, and decimation in the case of direct detection, or to bypass only decimation. In these two scenarios, a very broad-band detection frequency range (up to 62.5 $MHz$) is achieved, allowing for the acquisition of long FIDs, up to several million points.

*1) Frequency translation :* After exiting the excitation phase, the system transitions into the acquisition phase, coinciding with the return of the nuclei spins to equilibrium. During this process, a NQR FID is emitted. The frequency of the FID, denoted as $\nu_0$, slightly deviates from the carrier frequency $\nu_{RF}$ by an offset represented by $\Delta$. Fig. 2 illustrates the relationship between the NQR received signal frequency and $\nu_0$ = $\nu_{RF}$ + $\Delta$.

Once the signal is digitized, it is sent to the FPGA (Fig. 3), where its frequency will be shifted by multiplying by a second DDS output of frequency $\nu_{RF}$ + IF so as to obtain a signal whose frequency is centered around a fixed intermediate frequency (IF) with an offset equal to $\Delta$. The objective is to always bring back the acquired signal, whose frequency is variable, around a chosen fixed carrier intermediate frequency which is the quarter of the sampling frequency. This will fulfill the necessary condition for simplified quadrature digital demodulation and simplifies the design of the band-pass filter as we will explain further in this section.

*2) Filtering :* Before being demodulated by the Digital Down Converter (DDC) (Fig. 3), the multiplier output is filtered by a digital band-pass decimator-FIR with a decimation ratio equal to 4 and a center frequency IF. The objective of this filtering is to eliminate all undesired frequencies and to enable the usage of a low intermediate frequency (less than 10 $MHz$) in order to enhance selectivity. The sampling frequency is reduced so that it is exactly equal to 4 times the intermediate frequency ($IF = 7.8125\ MHz$).

*3) Demodulation :* The DDC is a home-made IP designed in VHDL that generates from the translated and filtered signal of frequency $IF - \Delta$ an $I/Q$ complex signal. The digital Quadrature Demodulation (DQD), performed inside the DDC, after the translation and filtering steps, reproduces the same mechanism used by the traditional analog $I/Q$ demodulators. Indeed, the output of the digital $I/Q$ demodulator is an in-phase signal $I$ and a quadrature signal $Q$ :

$$\begin{aligned} \mathrm{I} &= \cos\{2\pi \cdot (IF - \Delta) \cdot t\} \cdot \cos(2\pi \cdot IF \cdot t) \\ \mathrm{Q} &= \cos\{2\pi \cdot (IF - \Delta) \cdot t)\} \cdot \sin(2\pi \cdot IF \cdot t) \end{aligned} \quad (1)$$

Each of the these complex components contains two frequencies, one of interest which is the offset $\Delta$ and one non desired, $2 \cdot IF - \Delta$, that will be removed by low-pass filtering.

To simplify the VHDL code of the DDC for digital multiplication by $cos(2\pi \cdot IF \cdot t)$ and $sin(2\pi \cdot IF \cdot t)$, we choose the intermediate frequency IF to be exactly one-fourth of the sampling rate. This choice ensures that the values of $cos(2\pi \cdot IF \cdot t)$ and $sin(2\pi \cdot IF \cdot t)$ at the sampling moments become simple integer values, specifically $1, 0, -1, 0$ for $cos(2\pi \cdot IF \cdot t)$ and $0, 1, 0, -1$ for $sin(2\pi \cdot IF \cdot t)$. By utilizing this approach, the generation of the digital $I$ and $Q$ signals can be simplified to a straightforward multiplexing mechanism. The digital incoming sample, which is represented as $\cos\{2\pi \cdot (IF - \Delta) \cdot t\}$, is sent alternately to the $I$ and $Q$ outputs with sign inversion. This multiplexing scheme, as described in [22], [43], is equivalent to the conventional analog $I/Q$ demodulation method.

After crossing the band-pass filter and DDC, the total decimation ratio is 8 and the spectral window is hence reduced by a factor of 8.

*4) Decimation :* To further reduce the spectral window and decrease the number of acquisition points, the complex demodulated NQR signal whose frequency is $-\Delta$ passes through CIC filtering to undergo a decimation with a variable ratio ranging from 4 to 1024 (eg., 128) programmable by the Linux application of the acquisition. The final spectral window obtained, in this example, is equal to the initial value (125 $MHz$) divided by a ratio of 1024 which is $8 \times 128$. The final spectral window is therefore $125\ MHz/1024 = 122070\ Hz$, which allows to display offsets $\Delta$ between $-61035\ Hz$ and $+61035\ Hz$.

*5) Accumulation and phase cycling module :* In order to enhance the Signal-to-Noise Ratio (SNR) and remove undesired artifacts, FID accumulation with phase cycling is performed. Instead of performing this operation only by software during post-processing, it is possible for this spectrometer to execute it on-the-fly in the FPGA. The objective is to optimize the operation when very big FIDs are used or when the allocated time between two consecutive scans is not sufficient for FID transfer after each scan. The accumulation and phase cycling module uses handshake mechanism signals (Ready and Valid) of the FIFOs and DMAs (AXI DMA 1 and AXI DMA 2) (Fig. 3 ) to guarantee the perfect synchronization between the new FID and the accumulated one that is read back from the DDR. Thanks to this solution, the two FIDs (the previously accumulated and the new one) are summed point by point at the FIFOs' outputs in perfect synchronization, without using any DDR addressing mechanism.

*6) Memory transfer :* At the output of the CIC, the decimated $I/Q$ data are sent to a double asynchronous-clock (125 $MHz$ clock for write and 160 $MHz$ clock for read) FIFO and then to the accumulator. The result of the accumulation is sent to the DMA which writes this decimated FID in a DDR memory zone dedicated to the written FID. The acquisition Linux application reads the FID corresponding to the current scan from the DDR zone dedicated to the read FID and performs, if desired, accumulation and user-defined phase cycling. The acquisition Linux application copies the content of the DDR zone dedicated to written FID into the DDR zone dedicated to read FID after each scan. Indeed, in the case we choose to not perform accumulation on FPGA, the acquisition application performs phase-cycling and accumulates the current scan with the previous accumulated scans. In the case where accumulation is performed on the FPGA, the current read FID, as it is already accumulated, can be sent directly after each scan to the PC. This can be achieved by transmitting it through sockets to the PC via Ethernet, where

it can be displayed in real-time using the interfacing/post-processing software. At the end of the experiment, and after performing the number of accumulations programmed by the user, the FID is stored in the form of a binary file which contains the two I and Q channels of the NQR signal.

### E. Auxiliary hardware

*1) Trigger module :* The initiation of the acquisition process relies on the trigger mechanism. Within this trigger module, its primary responsibility is to produce the trigger flag, a crucial determinant defined by the chosen source in the configuration settings. The trigger can originate from various sources : it may respond to the rising or falling edge of external RF inputs 1 or 2, be generated by the pulser IP (when the trigger signal is set during the TRIGGER state), or be triggered via software commands.

*2) Top level interface registers :* This block manages the primary configuration settings for the spectrometer, which are adjusted by the user through a graphical interface. These settings determine how the spectrometer operates during a specific experiment. The pulser and acquisition applications translate the user's inputs, such as RF pulse frequency, number of points, dwell time, number of scans, and pulse width, into configurations that are applied to the system. These configurations are then programmed into the system through the CPU. The configuration settings are controlled through registers, which handle aspects like reset, acquisition mode, triggering, thresholds, scan numbers, frequency settings, power levels, and operational modes. Additionally, there are specific settings within the configuration registers, such as options for phase cycling and debug modes, which are used for specialized purposes during experiments. Lastly, there is a register that keeps track of the number of points effectively sampled during an acquisition scan. This value is determined based on the user's preferences for display points and the system's decimation rate.

*3) Backbone :* The FPGA_SoC backbone is composed of an ARM9 dual core, and AXI interconnect and a DDR interface.

*4) Clocks and reset generator :* Normally, the SoC-FPGA needs to work with four clocks, a 125 $MHz$ clock for the pulser, a 31.25 $MHz$ clock for the DDC, a 15.625 $MHz$ for the CIC and a 160 $MHz$ clock for the system. Nevertheless, an optimization of the SOC-FPGA architecture was performed in order to use only two clocks, the 125 $MHz$ and the 160 $MHz$. Indeed, by using the handshake mechanism signals "READY" and "VALID" of the AXI stream protocol between the different IPs (FIR, DDC, CIC, FIFOs, DMAs), and using an asynchronous double-clock FIFO for clock-domain crossing (Fig. 3), the same functionality was achieved with only two clocks. At the output of the asynchronous FIFO, the read clock which is the system clock (160 $MHz$), is higher that the write clock (125 $MHz$) in order to prevent data write overflow for FID acquisition. The 2 clocks are generated by the Xilinx IP clock wizards. The related resets are generated by the Xilinx reset modules.

*5) ILA :* The SoC-FPGA contains also an ILA (Integrated Logic Analyzer) in order to debug the Hardware on the target using Vivado Hardware Manager and a Jtag cable. It is a Xilinx configurable built-in probe that enables the user to observe and analyze, during the real execution on target, the values of certain signals chosen in advance.

## III. Experimental validation

### A. Experimental details

*1) Material details:* The proposed system architecture of the NQR spectrometer is implemented on a Zynq 7000 device family FPGA from Xilinx [44] located on the STEMlab 125-14 board. The validation environment of the compact NQR spectrometer (Fig. 4) is composed of an analog front-end and the STEMlab 125-14 board that includes an ADC, a DAC, a DDR3 memory, and other electronic parts. The analog Front-end is composed of a set of changeable duplexers, an NQR probehead with changeable solenoids from NMR service [45], an LNA (AU-1525) from Narda-MITEQ with a noise figure of 1.3 $dB$ and a gain of 61 $dB$. The changeable devices allow covering the studied spectral ranges. The results presented here have been acquired with a high power NMR amplifier (TOMCO BT00250 BETA 250 $W$ ) by dividing the RF signal amplitude down to about 2 $W$ using the FPGA DAC IF interface located in the transmitter module (Fig. 3). Since NQR experiments are usually best performed using weaker RF pulses than for NMR [46], the compact low-power amplifier pictured in Fig. 4 (Walfront $1-930$ $MHz$, 2 $W$) has also been successfully tested.

*2) Experimental parameters:* $^{14}N$ NQR Spectra of $NaNO_2$ and HMT, as well as $^{35}Cl$ NQR Spectra of $1,3,5-TCB$ (T = 295 K) were acquired with single pulse excitation experiments. Spin excitation was performed with an amplification of about 2 $W$ (by performing digital amplitude division inside the FPGA on the input signal of the 250 $W$ power amplifier), resulting in optimal excitation pulse durations of 50 $\mu$s to 100 $\mu$s depending on the signal resonance frequency. Optimal pulse durations were determined by taking the first maximum of each spin nutation profile. Interscan recovery delays of 1 $s$ and 0.5 $s$ were used for $^{14}N$ and $^{35}Cl$, respectively, during the signal accumulation procedure. $^{14}N$ $NaNO_2$ spectra were acquired for $\nu_0$ (128 scans), $\nu_-$ (4 scans) and $\nu_+$ (4 scans) respectively, and HMT spectra with 64 scans. $^{35}Cl$ $1,3,5-TCB$ spectra were acquired for 32 scans using a Bruker BBO 10 mm NMR probehead. For all experiments, the spectra were acquired over a frequency window of 122 $kHz$ for $2k$ complex points, resulting in an acquisition time of 8.4 $ms$.

*3) Signal post-processing:* Signal post-processing was performed independently from acquisition on an external PC laptop (Fig. 4) via our constantly upgraded homemade processing software written in Java code [40] or alternatively by the GSim NMR signal processing program developed by V. Zorin [47]. The usual post-processing sequence was performed, including zero filling up to 8k points, a 50 $Hz$ Lorentzian apodisation, a complex Fourier transformation to the frequency domain, and final phase and baseline correction. In order to assess the

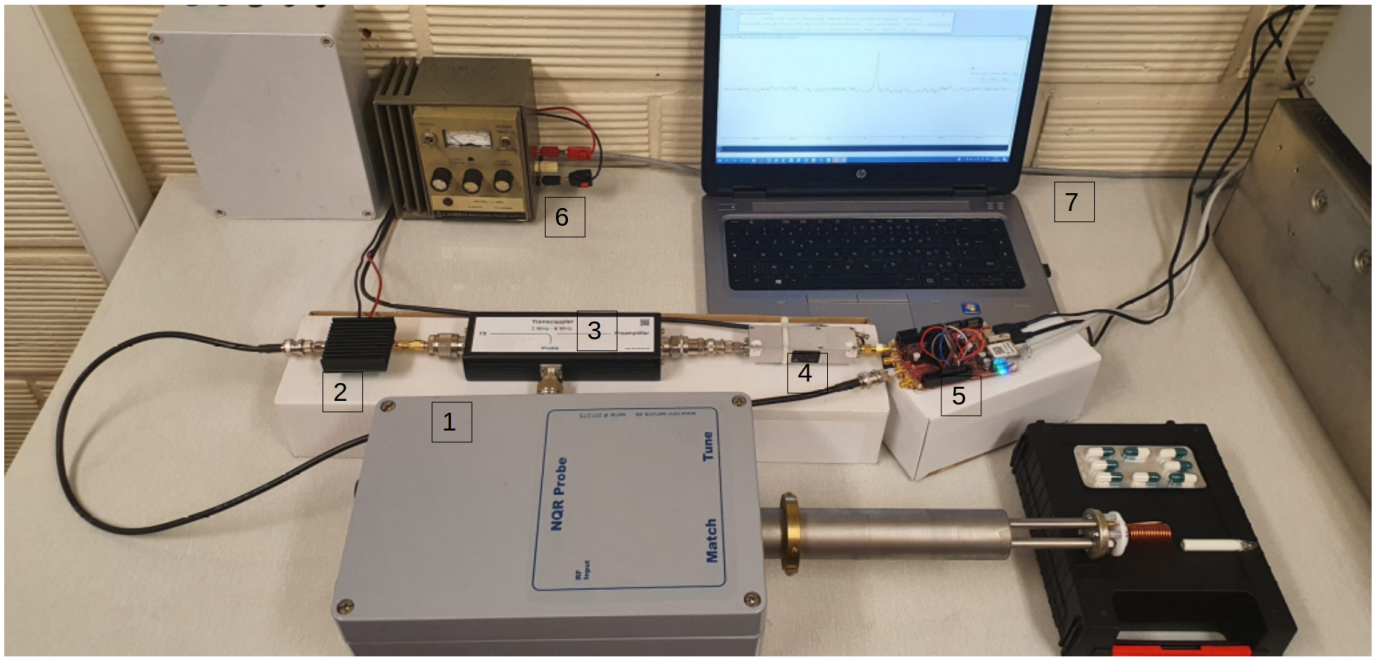


Fig. 4: Validation environment of the NQR compact spectrometer : 1 : The probe, 2 : PA, 3 : The changeable duplexer, 4 : The LNA 5 : The STEMlab 125-14 board containing the SoC-FPGA , 6 : The DC power source for the PA, 7 : The PC for NQR post-processing

sensitivity improvements induced by the subsequent upgrades of our equipment, we calculated SNR by taking the ratio between the signal amplitude and the noise of a signal-free region corresponding to 10 percent of the spectral frequency window. The noise was estimated by calculating the Root Mean Square Deviation (RMSD) in the signal-free region. The approximate sensitivity comparison presented in table III relies on the average SNR increase factor (expressed in dB) with respect to the reference v 2007 obtained for a series of experiments acquired on the same sample (Sodium Nitrite $m_{NaNO_2}$ = 5 g, $\nu_+$ = 4.646 $MHz$ for different accumulation numbers (16, 32, 64, and 128 scans).

### B. Results

To validate its applicability in NQR spectroscopy, we conducted tests using the presented spectrometer on three distinct reference samples. These samples consisted of Sodium Nitrite ($NaNO_2$) and hexamethylenetetramine (HMT) to cover the complete $^{14}N$ NQR frequency range, as well as 1,3,5-Trichlorobenzene ($1,3,5-TCB$) to access the higher frequency range of $^{35}Cl$. In the crystalline Sodium Nitrite sample, only one crystallographic nonequivalent $^{14}N$ nucleus with a non-zero asymmetry parameter ($\eta = 0.379$) exists. Consequently, our expectations, as depicted in Fig. 1, are for three distinct NQR resonance frequencies : $\nu_+ = 4.646\ MHz$, $\nu_- = 3.607\ MHz$, and $\nu_0 = 1.040\ MHz$ [48]. In the case of HMT, the crystal structure also contains a single nonequivalent $^{14}N$ site, but with an asymmetry parameter $\eta = 0$. Therefore, we anticipate a single resonance at $\nu = 3.311\ MHz$ [49]. Regarding $^{35}Cl$ NQR measurements, we expect only one frequency per site due to the degeneracy of the +/- energy levels, as shown in Fig. 1. For 1,3,5-Trichlorobenzene ($1,3,5-TCB$), this implies three distinct NQR resonance frequencies : $\nu_1 = 35.555\ MHz$, $\nu_2 = 35.303\ MHz$, and $\nu_3 = 35.027\ MHz$ [50].

As shown in Fig. 5, the spectrometer successfully detected all expected resonances, even when using relatively small sample quantities ($m_{NaNO_2} = 5\ g$, $m_{HMT} = 4.5\ g$, and $m_{1,3,5-TCB} = 4.8\ g$). Notably, these spectra were obtained through straightforward "one-pulse" experiments, and the data collection required very short experimental times, ranging from nearly 2 minutes to just a few seconds. This remarkable performance underscores the high sensitivity of the proposed spectrometer, which offers approximately 25 times sensitivity improvement (+28 dB) compared to the first spectrometer developed within our research group [40].

## IV. Discussions

The primary objective behind developing this new compact NQR spectrometer was to enhance sensitivity, usability, portability, and overall performance with respect to the initial NQR spectrometer developed by our team in 2007 [40]. This is performed here by integrating a maximum of hardware and software functionalities into an SoC-FPGA with an optimized architecture. A first step was achieved in 2016, where several upgrades implying a new probe (+ 1 dB), sample temperature control (+ 1 dB) and a new LNA (+ 4 dB) lead to SNR improvement. Nevertheless the most significant improvements of this upgrade (+ 14 dB) came from the integration of a new high speed acquisition board (ADQ 214 SP-Devices) and a customized decimation software allowing signal oversampling (400 MS/s sampling frequency). This provided a total collective SNR enhancement of about an order of magnitude

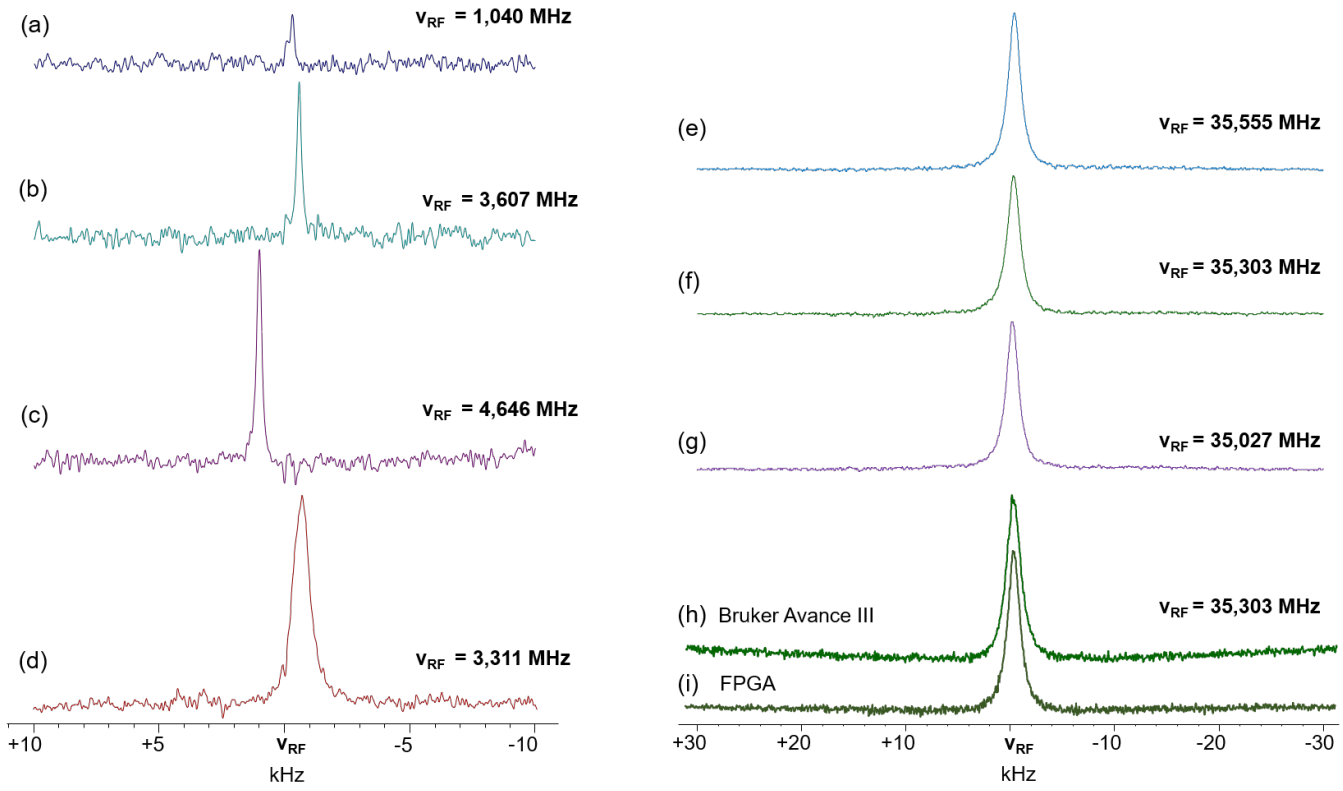


Fig. 5: $^{14}N$ NQR Spectra of $NaNO_2$ and HMT acquired at $T = 295\ K$ (left) and $^{35}Cl$ NQR Spectra of 1,3,5-TCB acquired at $T = 298\ K$ (right). Spectra (a), (b) and (c) are acquired on $NaNO_2$ for $\nu_0$ (128 scans), $\nu_-$ (4 scans) and $\nu_+$ (4 scans) respectively. Spectrum (d) is acquired on HMT with 64 scans. Spectra (e), (f) and (g) are acquired on 1,3,5-TCB and correspond to the 3 nonequivalent $^{35}Cl$ sites in the crystal structure. Each spectrum was acquired with 32 scans. For all experiments, the central pulse excitation frequency is highlighted in bold. Spectra (h), (i) compare respectively the acquisition on a Bruker Avance III 600 $MHz$ NMR spectrometer with the presented FPGA spectrometer (no apodization processing has been performed on these two spectra).

(+ 20 dB) with respect to the first published version. The new version presented here builds upon this experience by applying these oversampling and decimation concepts. It additionally implements the I/Q demodulation digitally, and also enhances RF immunity by integrating more functions on FPGA (table III). These new developments improved even more the sensitivity compared to the initial spectrometer (about +28 dB) and also brought portability and usability improvements. Several concomitant factors related to the digital integration can explain this additional (+8 dB) improvement. These factors include the elimination of typical problems linked to the analog signal treatment (e.g., unbalanced channels related artifacts), as well as the increase of the dynamic range by using 32-bits I/Q digital demodulation, and the reduced exposure to radio frequency noise.

The final performance is visually illustrated in Fig. 5 (h) and (i), where we compare one of the $^{35}Cl$ spectra acquired using our SoC-FPGA spectrometer with that acquired using a commercial Bruker Avance III 600 $MHz$ NMR spectrometer. Both spectra were obtained using the same sample, probe-head, experimental parameters, and processing parameters (no apodization was applied here to ensure an accurate Signal to Noise comparison). As evident in the spectra, the sensitivity of the compact spectrometer matches that of the Bruker spectrometer.

The ADC sampling rate of the STEMlab 125-14 board used here provides a detection frequency range up to 62.5 $MHz$. Since this covers the whole $^{14}N$, $^{17}O$, $^{35,37}Cl$ and $^{169,171}Ga$ frequency ranges, it is indeed sufficient for most applications including the detection of drugs, mines, plastic explosives and pharmaceuticals. Nevertheless if other nuclei (e.g. $^{79}Br$, $^{127}I$ or $^{121,123}Sb$) need to be studied, the maximum frequency can be increased by implementing several solutions like migrating the SoC-FPGA design to a board with faster ADC (e.g., Redpitaya SIGNALlab 250-12 [51] or a board from the Zynq UltraScale+ RFSoC family [52]) or/and using additional external analog up-conversion/down-conversion modules. If one wishes to keep the same STEMlab 125-14 board, under-sampling technique with changeable band pass filters (bandwidth B less than $F_s/2$) can be applied in order to screen the total spectrum. Adding an external dedicated high frequency DDS board would be necessary for the latter case.

With respect to the state of the art, we used the best-in-class available platforms. Our system is a compact digital spec-

TABLE III: Features comparison between the proposed SoC-FPGA spectrometer and the previous versions of the NQR spectrometer developed in the team (v 2007 [40] and v 2016)

| Parameters | Reference spectrometer v 2007 [40] | Upgraded reference spectrometer (v 2016) | Proposed SoC-FPGA spectrometer |
|---|---|---|---|
| I/Q demodulation | Analogue, separate element | Analogue, separate element | Digital, integrated on FPGA |
| Direct detection | NO | NO | YES |
| Broad band acquisition | NO | NO | YES |
| Accumulation on FPGA | NO | NO | Available |
| Over-sampling and decimation | NO | YES | YES |
| Pulse programmer | Separate equipment (Spincore) | Separate equipment (Spincore) | Integrated on FPGA |
| Emission unit | Separate element (Home-made) | Separate element (Home-made) | Integrated on FPGA |
| Acquisition unit | Separate element (Home-made) | Separate equipment (ADQ 214 SP-Devices) | Integrated on FPGA |
| Acquisition SW | On PC | On PC | Embedded on FPGA |
| LNA | Anzac AM-110 30dB LNA in series with a 24dB ZFL-500LN LNA | MITEQ AU-1525 | MITEQ AU-1525 |
| Probe | Home made | Commercial(NMRService, Bruker) | Commercial(NMR Service, Bruker) |
| Temperature control | YES | YES | YES |
| Timing resolution | 10 ns | 10 ns | 8 ns |
| Minimum pulse width | 50 ns | 50 ns | 8 ns |
| Relative sensitivity (SNR) | Reference | +20 dB | +28 dB |
| Instructions memory | 4k of 80-bit instructions | 4k of 80-bit instructions | Up to 32 million 128-bit instructions |

trometer built on the STEMlab 125-14 AP-SoC of the Zynq 7000 device family hybrid system that contains programmable logic and processing sub-system. This technology provides the developer with an outstanding HW and SW development platform and high-end flows and methodologies for embedded systems design and makes it possible to integrate the major spectrometer Hardware and Software parts on a single FPGA. The optimized architecture of this spectrometer increases the immunity of the system to external noise and enables to perform all the relevant signal processing in the digital domain, especially frequency translation, quadrature demodulation and filtering. Moreover, the embedded software for the acquisition module and pulser drivers is designed to run on the dual-ARM9 core. Indeed, this SoC-FPGA is composed of a fully custom VHDL pulse programmer driven by a dedicated home-made software instead of an external equipment. It uses AXI DMA and external DDR for storing and retrieving the experiment instructions which guarantees a very high pulse width resolution (8 ns) and enables a very large number of instructions without introducing any delay between their execution. In addition to the high performance pulse programmer, this SoC-FPGA based spectrometer integrates a pulse transmitter that is controlled in frequency, phase and amplitude which enables the user to launch typical phase cycled NQR experiments. With respect to standard available commercial spectrometers, the main advantages of the proposed spectrometer are summarized in Table IV.

The third major spectrometer part is the acquisition module, which is a complete receiver, fully integrated inside the digital domain, performing either a direct digital detection for ultra-broad band acquisition, or a frequency translation and $I/Q$ demodulation for digital quadrature detection scheme. The architecture of the acquisition module is based on DMA for optimized transfer throughput and on external DDR3 memory for storing the FID, rather than using internal FPGA RAM blocks. This advantage makes it possible to store a very large number of FID points, thus enabling a long acquisition time (up to one million points), broad band detection, and performing accumulation directly on the FPGA for a maximum repetition rate and standalone operating mode. Moreover, using FPGA makes this spectrometer fully flexible and configurable even remotely.

For portability considerations, this compact spectrometer was also successfully tested using a compact $2\ W$ amplifier (Fig. 4) which can be battery operated. This enlarges the field of portability and miniaturization, thus facilitating outdoor applications like anti-personnel landmines detection.

In estimating the power consumption, we have considered the specifications for each component. The STEMlab 125-14, with a voltage of $5\ V$ and a maximum current of $2\ A$ (equating to a maximum power consumption of $10\ W$, including the FPGA), contributes to the overall power budget. The Low-Noise Amplifier (LNA), specified by MITEQ AU1525 with a voltage of $15\ V$ and a current of $225\ mA$, adds an additional power consumption of $3.5\ W$. The power amplifier (Walfront $1-930\ MHz$, $2\ W$), boasting a power rating of $2\ W$, further contributes to the estimated power usage. Thus, collectively, our conservative estimate suggests a maximum power consumption of $15.5\ W$ for the entire system. It's important to note that this figure is considered an overestimate, providing a safety margin for the actual power requirements of the system.

This SoC-FPGA spectrometer, which already constitutes a high quality proof of concept, is still able to evolve. Indeed, it is perfectly capable of interfacing with other boards which may embed the remaining spectrometer hardware functionalities, especially Front-End parts (probehead, impedance matching, duplexers) and pulse power amplification part. Also, additional

TABLE IV: Performances comparison between the proposed spectrometer and the other commercial solutions

| Parameters | Proposed spectrometer | Magritek Kea [53] | Tecmag Redstone [54] |
|---|---|---|---|
| Application | NQR | NQR/NMR | NQR/NMR/MRI |
| Features | DQD/Direct detection/Broad band | - | - |
| Receiver architecture | Full digital superheterodyne and low IF | - | - |
| Frequency range | $0 - 62.5\ MHz$ | $0 - 400\ MHz$ | $0 - 500\ MHz$ |
| Timing resolution | 8 ns | 100 ns | 10 ns |
| Minimum pulse width | 8 ns | 100 ns | 10 ns |
| Memory | 64 million of 2x32-bit samples | 256 k of 24-bit samples | 2x64 M of 24-bit samples |

signal denoising algorithms can be further implemented on the FPGA.

## V. Conclusion

In this work we present a compact SoC-FPGA based spectrometer and illustrate its performances by presenting $^{14}N$ and $^{35}Cl$ multi-nuclear NQR spectra acquired for representative samples including $NaNO_2$, $HMT$ and $1,3,5 - TCB$. The proposed SoC-FPGA spectrometer contains a high performance acquisition and signal processing pipe, a high resolution pulse programmer and a fully controllable transmitter. Although we focus in this work on NQR applications, the presented spectrometer can also be used as a sensitive low field NMR spectrometer. Comparison with a commercial state of the art NMR spectrometer, shows that we obtain equivalent sensitivity performances with our low cost compact spectrometer. Additional signal denoising algorithms will be further implemented on the FPGA module in order to enhance the spectrometer sensitivity.

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