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Abstract

The objective of this paper is to study Metal-Air-FR4 triple point management for the development of three-dimensions (3D) power modules based on printed circuit boards (PCB). Capacitive field grading structure is introduced to shift the high electrical field area from the triple point in the air to the FR4 PCB resin. The concept is firstly exposed with finite element simulations, and different field plate architectures are compared. Experiments are then carried out. They show that the Partial Discharge Inception Voltage and Breakdown Voltage can be increased at least by +248% and +8.2% respectively compared to PCB without field plates.

1 Introduction

Currently, many power electronics developments focus on high power density converters with massive integration of Wide Band-Gap (WBG) semiconductors. Indeed, the management of high switching speed combined with higher efficiency and compacity lead researchers to find better integration solutions than the classical two-dimensions (2D) power module architecture [1]. Solutions based on three-dimensions (3D) structures and Printed Circuit Board (PCB) with embedded dies allow to alleviate 2D weaknesses by reducing stray inductance of switching loops [2]. Also, they make it possible to cool the dies on their both sides [3]. For instance, Fig. 1 presents a structure with a PCB embedded switching cell made of two flip-chipped WBG dies, leading to massive inductance loop reduction as described in [3], [4]. In this figure, the cooling is done by heatsinks attached to DC+, DC- and Phase electrodes. Thus, several electrical triple points are present with a possible high electric field in the air area.

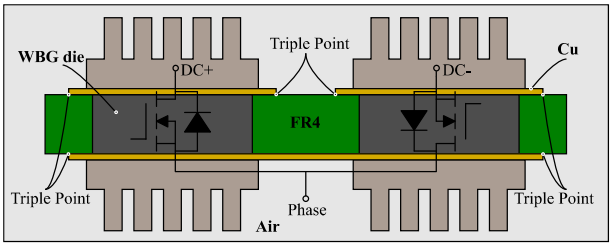


Fig. 1: PCB embedding switching cell made of two flip-chipped WBG dies

The literature presents several techniques to manage the electrical field reinforcement at triple point [5]. For instance, Waltrich et al. [6] propose to apply a dielectric coating to reduce the electric field at this location. Other solutions lie on geometric modifications: Reynes et al. [7] propose to modify the shape of the metallization (i.e. sharp to round edge) to submit triple point at lower field area, and Hourdequin et al. [8] present a structure with a gap between two surface metallizations to improve electrical field distribution. Although these techniques have proved their abilities, material modifications require control process and chemical dependency, while surface geometric modifications like in [7] seem to be more complicated for PCB applications compared to bulk materials classically used in 2D power modules.

A solution developed in [9] for high voltage DC-link busbars lies in modifying the electrical field configuration thanks to a capacitive field grading inside the PCB structure. With this technique, the electrical field reinforcement located at the triple point is reduced and transferred to another material with better dielectric rigidity than air, i.e. FR4 resin.

The present paper aims to study capacitive field grading structures, i.e. field plate designs, dedicated to PCB embedding assemblies as shown in Fig. 1 with a high voltage applied across the thickness of the PCB. For this study it is assumed that the off-state of the power chips is well managed, meaning that the voltage drop is fully transferred to the PCB. For a given applied voltage, the electric field mapping inside and outside the PCB will be determined solely by its design. In Fig. 2 is depicted a possible PCB architecture inspired by the capacitive field grading method adapted to the PCB embedding assemblies. The dotted rectangle represents the area concerned by the present work, while power chips are not considered in the study.

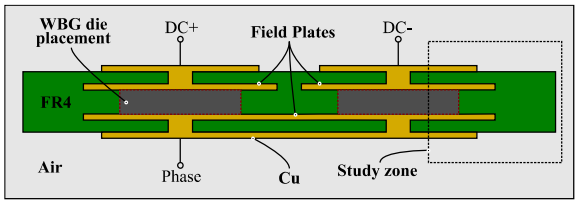


Fig. 2: Field plate concept

The next section presents a preliminary study of the concept based on numerical simulations. Then different PCB assemblies and the experimental setup are depicted. Eventually, Partial Discharge (PD) and Breakdown Voltage (BDV) experimental results are shown and analyzed.

2 Preliminary Study of the Concept Based on Numerical Simulations

This section compares different PCB geometries representative of the assembly of Fig. 2, with and without capacitive field grading structure. The objectives of these simulations are: i) identify the weaknesses areas of the structures based on the electrical field reinforcement, ii) evaluate the electrical field, despite that this criteria does not represent exactly the physicals phenomena, in various zones of interest for different field plate configurations. This study is based on finite element numerical simulations developed with COMSOL Multiphysics V6.0 software and electrostatic physics resolution. The reference case, i.e. without field plate, is studied in the next subsection. Then, configurations with field plates are evaluated in the second subsection.

2.1 PCB without Field Plates

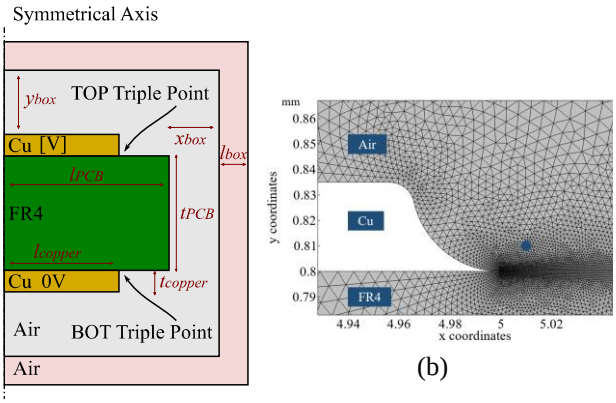
The reference geometry without embedded dies is shown in Fig. 3a with geometrical dimensions representative of the desired application. A 2D geometry is simulated with an axial symmetry and all geometrical dimensions are depicted in Table 1. Considering the hypothesis that space charges do not influence the electrical field behavior, Poisson equation can accordingly be reduced to Laplace equation.

For the boundary conditions, an infinite box is mandatory to represent the air domain around the PCB. Outer boundaries of this domain, defined far enough (x_{box} and y_{box} parameters) of the potentials, are defined as Dirichlet boundary condition where inductive field $\vec{D}$ is set to zero. The high-voltage value is defined to 15kV while the other metallization is set to ground potential.

The presence of three materials of different permittivities in the simulated geometry entails to consider some numerical simulations limitations in regards of triple point effect [10]. Therefore, the edges of metallizations were simplified and the mesh accordingly refined around the triple point (Fig. 3b). Moreover, to bypass singularities of numerical simulation calculations, the electrical field is measured at 10µm (point represented in Fig. 3b) from the triple point location as suggested by [10].

Table 1: Geometrical dimensions and physical parameters of numerical simulations

Parameter	Value	Parameter	Value
l_{PCB}	10 mm	x_{box}	10 mm
t_{PCB}	1.6 mm	y_{box}	6.7 mm
l_{copper}	5 mm	V	15 kV
t_{copper}	35 µm	εr_{FR4}	4.5
t_{FP}	480 µm	εr_{Cu}	1
t_{mid}	570 µm	εr_{Air}	1.0006
l_{box}	1 mm		



(a) (b)

Fig. 3: (a) PCB without field plate geometry and (b) Simulation mesh around triple point with the dot representing electrical field measurement point

Fig. 4 shows simulation results of equipotential lines and electrical field mapping in the air and FR4 without field plates. The colorscale being defined between 0 and 30kV/mm, white area (except for the metallizations) represents electrical field values out of this scale. The electric field enhancement at the triple point is clearly identified by simulation and highlights the copper edge metallization as a weakness point leading potentially to breakdown or partial discharge activity.

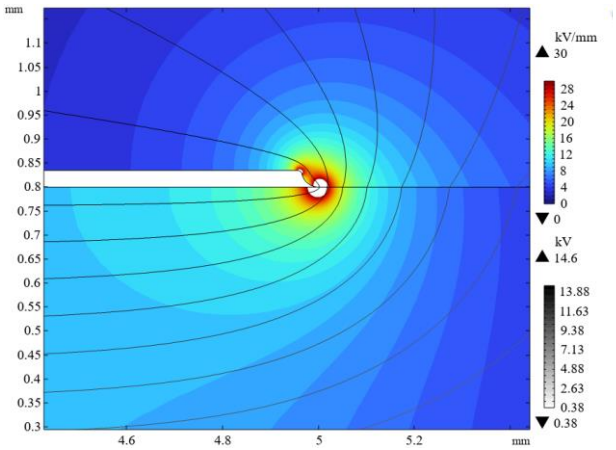


Fig. 4: Equipotential lines and field mapping results of PCB without field plates

Given that voltage withstand issues can lead to destruction of power modules, solutions must be proposed to guarantee that the maximum electrical field is lower than the dielectric rigidity of the weakest material, i.e. the air.

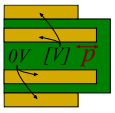
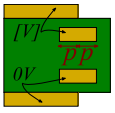
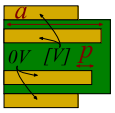
2.2 PCB with Field Plates

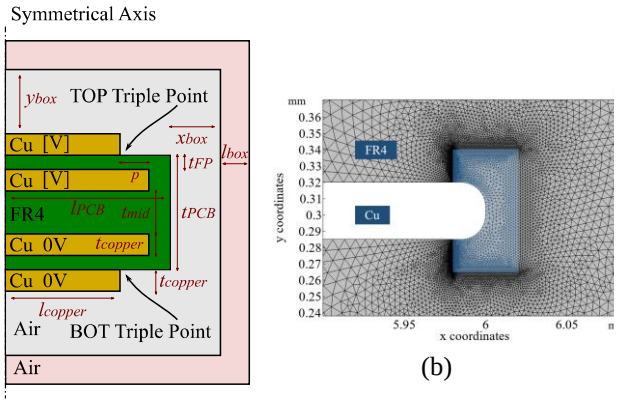
Compared to Direct Bonded Copper (DBC) classically used in 2D power modules architectures, PCBs benefit from lower cost process realization and more degrees of freedom in a design point of view. Indeed, PCB fabrication holds on an iterative process consisting of alternatively stacking conductive and isolating layers. Voltage withstand can therefore be considered during PCB design with proper definition of conductive layers and potentials associated to them.

Different field plates configurations, depicted in Table 2, are proposed in order to study the influence of field plate geometries on electrical field map. The first possibility aims to study the influence of inner copper field plates inside the PCB. This configuration is called “Symmetrical” in the table. In this case, the main parameter is the equipotential prolongation *p*. The second possibility, called “Non continue” in the table, aims to study the effect of short field plates near the triple points. Finally, the last configuration is defined by two field plates with different dimensions. It allows evaluating the influence on non-symmetrical geometries. The field plate at the TOP has a fixed width (*a*=9mm). The variable parameter *p* is defined as the offset between the bottom (BOT) field plate and the BOT outer layer.

A symmetrical configuration is depicted in Fig. 5a and all the geometrical dimensions are given in Table 1. This multilayer PCB is made up two groups of conductive layers. The first one (outer layers) has the same location and dimensions than the case without field plates. The second one (inner layers acting as field plates) has a larger width, *p* being the offset between outer and inner layers and the equipotential prolongation. For all simulated configurations, only the field plates patterns change.

Table 2: Different field plate configurations evaluated with numerical simulations

Field plates variants	Illustration	Studied parameter	Study range (mm)
Symmetrical		*p*	0 – 4
Non continue		*p*	0.5 – 2.5
Asymmetrical		*p* with fixed TOP field plate	0 – 4



(a) (b)

Fig. 5: (a) PCB with field plate geometry and (b) Simulation mesh around field plate edge

2.2.1 Simulation results – general trends

Simulation results of PCB with symmetrical field plates (*p*=1mm) are illustrated in Fig. 6. A comparison of electrical field maps of Fig. 4 and Fig. 6 highlights the effect of the concept with the displacement of the maximum electrical field from the triple point to the field plate edge. The 3kV/mm electrical field at the triple point represents a decrease of 91% compared to the reference case at the same location.

Nevertheless, the presence of inner layers lies in an electrical field reinforcement at the end of the field plates leading to: i) a possible PD inception inside FR4 resin as a result of micro air cavities, ii) a possible BDV through FR4 resin. This reinforcement can be evaluated with the measurement of the maximum electrical field on a defined area represented by the rectangle of Fig. 5b. For example, a maximum electrical field of 88kV/mm can be evaluated in this zone with *p*=1mm. This value represents an increase of 144% compared to the reference case with a maximum electrical field inside FR4 equal to 36kV/mm (Fig. 4). The electrical field decrease observed at the triple point is consequently balanced by an increase inside the FR4. These issues seem necessary to consider for high voltage applications.

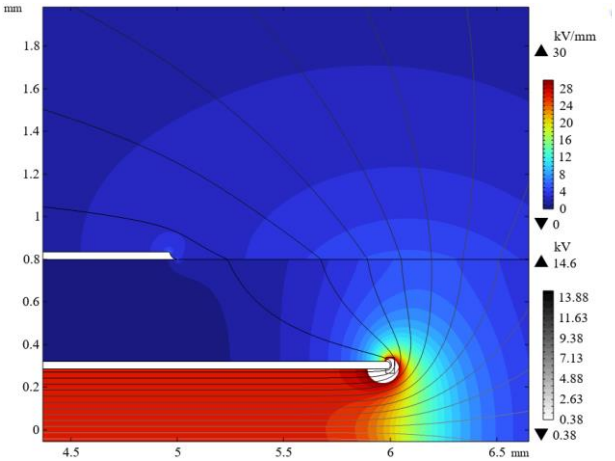


Fig. 6: Equipotential lines and field mapping results of PCB with field plates

2.2.2 Simulation results at the triple point

The behavior of the electrical field at triple point as a function of *p* is evaluated for the different configurations of Table 2. Results are depicted in Fig. 7 where the horizontal dashed-dotted line represents the reference case without field plate. This value is defined to 1pu for this analysis in order to carry on a comparison based on electrical field values for the different field plate configurations. The first and second variants being symmetrical, only the electrical field at TOP triple point (Fig. 5a) is considered while the BOT triple point is also evaluated for the asymmetrical variant.

Except for the asymmetrical TOP, the electric field at the triple point decreases when *p* increases. The quasi-flat evolution of the asymmetrical TOP triple point electrical field below 0.01pu is explained by the fact that the corresponding field plate have a constant length for all these simulations.

The symmetrical configuration shows a decrease of the triple point electric field when *p* increases from 0.63pu to 0.026pu. The non continue variant follows the same trend with values from 0.24pu to 0.034pu.
A higher sensitivity to *p* is observed in the case of the BOT triple point of the asymmetrical configuration, with a decrease of the electric field from 1.04pu to 0.026pu when *p* increases.

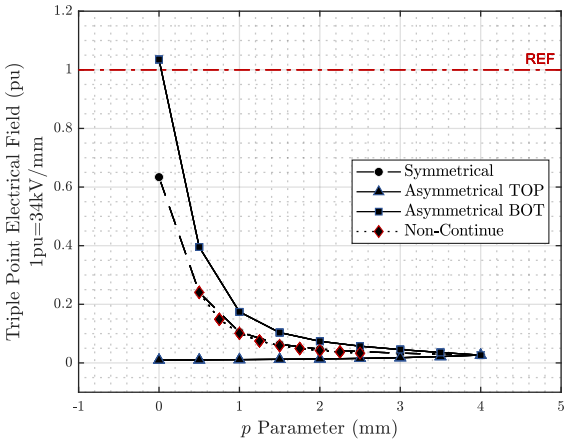


Fig. 7: Triple point simulation results analysis for various field plates configurations

2.2.3 Simulation results in the FR4 resin

The maximum electrical field at the ends of field plates in the FR4 region is also investigated, given that it can represent a possible drawback of the concept. The homogenous electrical field between field plates is defined as the reference (1pu=26kV/mm). The results are illustrated in Fig. 8. The electrical field reinforcement of the symmetrical configuration between 3.3pu and 3.4pu is not very sensitive to *p* in the proposed range. For the non continue configuration, both edges of field plates are analyzed. It can be seen that right and left edges are also not very sensistive to *p* but a dissymmetric constraint can be observed at both ends of the internal plate. Finally, the edges of the asymmetrical configuration admit opposite behaviors with respectively a decrease and an increase of the maximum electrical field at BOT and TOP ends as *p* increases.

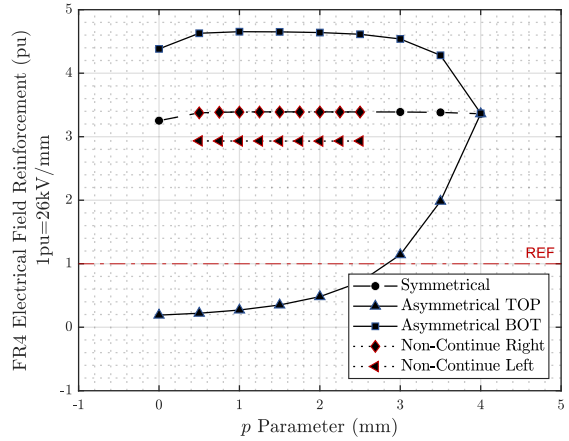


Fig. 8: Field plate termination simulation results analysis for various field plates configurations

2.2.4 Simulation results - conclusions

The analysis of the different field plate configurations leads to the following conclusions:

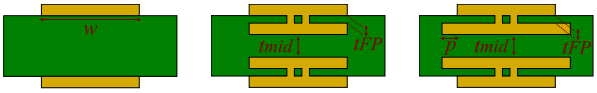
1) The symmetrical configuration allows reducing drastically the electrical field at triple point when *p* increases. It is also observed that the electrical field at the edges is not significantly dependent on this parameter.
2) The non-continue configuration has a behavior close to the symmetrical one as field plates are also *y* axis symetricals with the same equipotential prolongation. The maximum electrical field inside the FR4 is nevertheless dissymmetric between right and left edges.
3) The asymmetrical configuration seems however not suited to electrical field attenuation since its value remains higher than the symmetrical case at the TOP triple point. This comment is also supported by a higher maximum electrical field inside the FR4 compared to the other configurations.

The study of capacitive field grading configurations thanks to numerical simulation tools allowed to expose the pros and cons of the concept. Comparison of PCB geometries without and with field plates indicates a possible reduction of the electrical field at triple point with a shifting of the maximum electrical field constraint from the air to the FR4 PCB resin. Different multilayer PCB configurations have been studied with variant field plate patterns. Based on analysis detailed in this section, symmetrical configuration of the field plates is considered for the rest of this paper.

3 Experimental Characterization

3.1 PCBs Design and Test Vessel

This experimental study aims to focus on the effect of field plates geometry on PD and BDV behaviors of PCB. Different configurations are made for the tests (Fig. 9). Their volume is 20mmx50mmx1.6mm and they include two 10mmx40mmx35µm copper layers on their both sides. Design A is defined as the reference case without field plate. Two other designs (B and C) include field plates, their geometrical dimensions are given in Table 3 where t_{FP} and t_{mid} represent respectively the field plates depth and distance between field plates. In design B, the inner and outer layers have the same width. In design C, the offset between outer and inner layers is *p*=2.5mm. Ten specimens by design are fabricated and characterized.



A) B) C)

Fig. 9: Synoptic patterns of different PCB configurations

Table 3: Geometrical dimensions of the PCB

Design	A	B	C
w [mm]	10	10	10
p [mm]	-	0	2.5
t_{FP} [µm]	-	480	480
t_{mid} [µm]	-	570	570

Fig. 10 represents the experimental test vessel for both PD and BDV tests. The PCB is inserted between two 12.5mm diameter spherical electrodes respectively connected to high voltage and ground potentials.

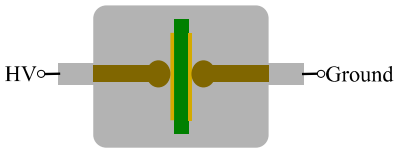


Fig. 10: BDV and PD test vessel

3.2 AC Partial Discharge Measurements

PD measurements in AC are performed in compliance with IEC 60270 standard recommendations using an Omicron commercial system. The setup has been used in previous works of the research group like in [11]. For the PD Inception Voltage (PDIV) measurement, each sample is submitted to a slow 0.4kV/s linearly increasing voltage until the PDIV is reached with a 10pC threshold. As PD events need to be originiate from the tests and not from possible static charges resulting from PCB conditionnement, a few preconditionning tests were considered. The average of the last five results is accordingly considered as the PDIV of the sample.

Fig. 11 depicts mean PDIV values of the ten specimens from each configuration with associated standard deviations. Preliminary analysis of Phase Resolved Partial Discharge (PRDP) diagrams of electrical and optical (FR4 being not electroluminescent) measurements allows to conclude on the area of the PD. Indeed, with a good correlation of both events in respect of voltage phase, it can be concluded that the PDs always take place at the surface of the PCB. Additional tests with some PCB immersed in dielectric fluid and none PDIV measured above 10kV support this conclusion.

Maximum and minimum PDIV results of each design are summarized in Table 4 in order to calculate maximum deviations between specimens. The mean values of all tests on all samples are depicted in Fig. 12 in order to conclude on PDIV results in relation to p parameter. With an increase of +7%, capacitive field grading effect is limited with p equals to 0mm. The third configuration with p equals to 2.5mm points out a 248% increase of global PDIV values compared to the reference case. This increase is allowed by the equipotential prolongation. It supports the trend observed in simulation with a high reduction of the electrical field in the air. Conditions for the apparition of PD events are therefore delayed to a higher voltage value.

Table 4: Maximum and minimum PDIV results of each configuration and associated standard deviations

Design	$PDIV_{min}$ (kV)	σ (kV)	$PDIV_{max}$ (kV)	σ (kV)	Δ_{PDIV} (kV)
A	2.07	0.145	2.85	0.0996	0.78
B	2.18	0.0491	3.02	0.119	0.84
C	8.02	0.215	9.48	0.571	1.5

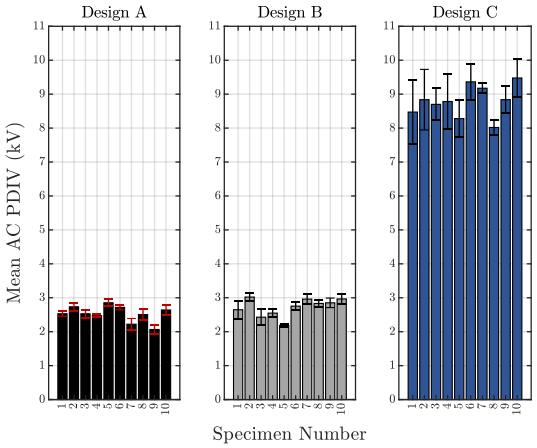


Fig. 11: Mean AC PDIV results of each configuration for all specimens

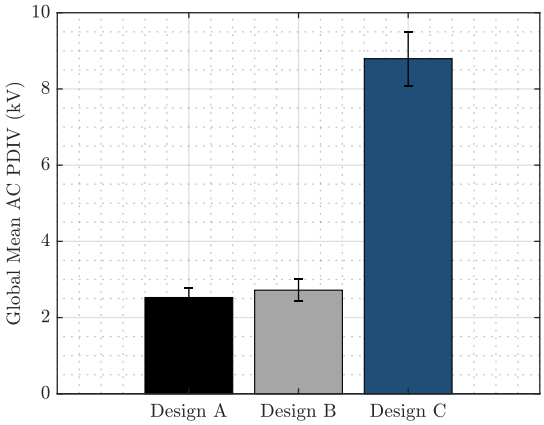


Fig. 12: Global mean PDIV results for each configuration

3.3 AC Breakdown Voltage Measurement

AC BDV measurements are performed with the same PDIV test vessel. A 50MHz 8-bit oscilloscope with high voltage and current probes allows to respectively measure voltage and current through PCB during the tests. The voltage source is manually stopped when breakdown occurs. Each PCB sample is subjected to a series of 20 consecutive BDV measurements with 0.5kV/s RMS voltage rising speed.

AC BDV experimental results of one sample are represented in Fig. 13 for the different PCBs designs of Table 3. It can be seen that no decrease trend is observed on every 20 consecutives BDV measurement. Therefore, it can be stated that the breakdown event always occurs in air with laboratory atmospheric conditions during the experiments.

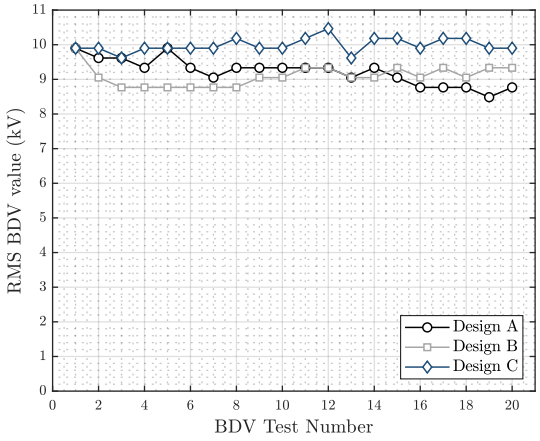


Fig. 13: Consecutive BDV results for one sample of each configuration

To enable comparison, the overall mean values over the 200 BDV measurements per configuration (20 BDV of 10 specimens per configuration) are depicted in Fig. 14. With a decrease of 0.3% and an increase of +8.2% for respectively designs B and C, BDV values seem less sensitive to the presence of field plates.

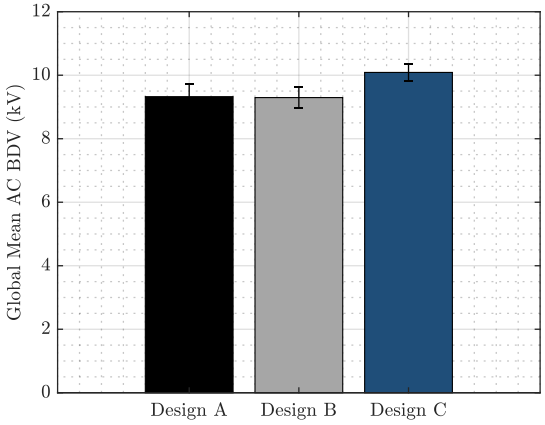


Fig. 14: Global mean BDV results for each configuration

As far as converter design rules are concerned, breakdown must be avoided. Thus, experimental BDV results can be fitted with the Weibull distribution to obtain BDV values especially at low probability levels [11]. Fig. 15 represents the Weibull fit results for all designs.

From the results, it can be noticed that BDV value of design B is weakly lower than design A at 63.2% risk level, while the contrary can be observed at 0.1% risk level. This paradigm must be carefully analyzed on the statistical point of view. Indeed, as can be seen on Fig. 15, BDV values are organized in clusters as a result of the voltage measurement which induce a 400V resolution with 8-bit on 10kV/div channel setting. The validation of Weibull distribution is therefore limited, as can be seen by the rejection of the null hypothesis of the Anderson-Darling statistical test [12]. Despite that, the high value of the slopes underlines the relatively small difference in the BDV between all risk levels. Decreases between 63.2% and 0.1% are respectively equals to -24%, -14% and -12% for designs A, B and C.

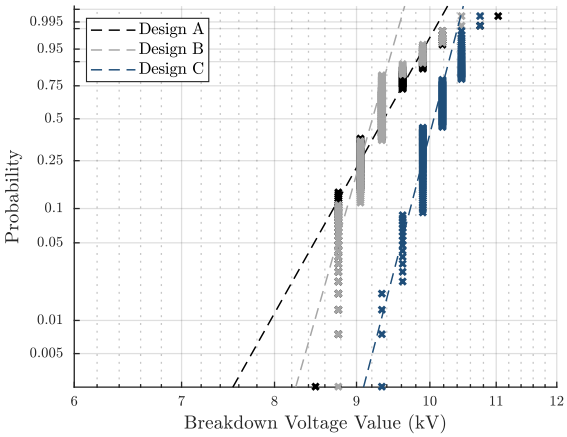


Fig. 15: Weibull distribution of all PCB designs BDV measurements

4 Discussion - Conclusion

In this paper, the management of the electrical field at triple point of 3D power modules isolated with air was studied. More specifically, a capacitive field grading solution dedicated to PCB embedding technology was evaluated.

Numerical simulation results of different field plate configurations inserted in the PCB allow to conclude on an attenuation of the electrical field at triple point. This observation is linked to the flattened behaviour of the equipotential lines around the triple point. The electrical field reinforcement at the edges of field plates, refered as a drawback in the case of present simulations (dimensions of Table 1), is more a consequence of the field plate disposition than a supplementary issue. The electrical field reinforcement observed must be therefore considered and the design of internal layers of PCB must be as symmetrical as possible with sufficient equipotential prolongation to decrease the electrical field at triple point and limit field reinforcement inside the FR4.

From experimental characterizations, it can be observed a high PD dependency to field plate configuration with a 248% increase of PDIV with p=2.5mm. However, the 40% electrical field decrease observed in simulation with p=0mm results in only +7% increase of PDIV compared to the reference case. These results highlight that the equipotential prolongation needs to be well chosen and optimized to really improve the design on the PD point of view.

On the contrary, BDV are less sensitive to the concept. Indeed, as breakdown always occurs in air, BDV results are more related to creepage distance (i.e. pad to pad distance) than triple point electrical field. PCB configurations presented in this paper holding on the same PCB size, BDV evolution is therefore limited. Note however that breakdown mechanisms depend on the electrical field at triple point given that this is the source of air ionization. Therefore, with a 96% decrease of triple point electrical field with p=2.5mm in simulations (Fig. 7), BDV values are nevertheless increased by 8.2% compared to the reference case.

Other works currently in development aims to study a possible optimized configuration in regards of PD and BDV states. The final objective is to define a trade-off between PCB size and *p* parameter in order to guarantee both a safe operating margin compare to desired application, and the best compacity for 3D power modules.

Acknowledgment

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