Multiple Shapes Micro-LEDs with Defect Free Sidewalls and Simple Liftoff and Transfer Using Selective Area Growth on Hexagonal Boron Nitride Template

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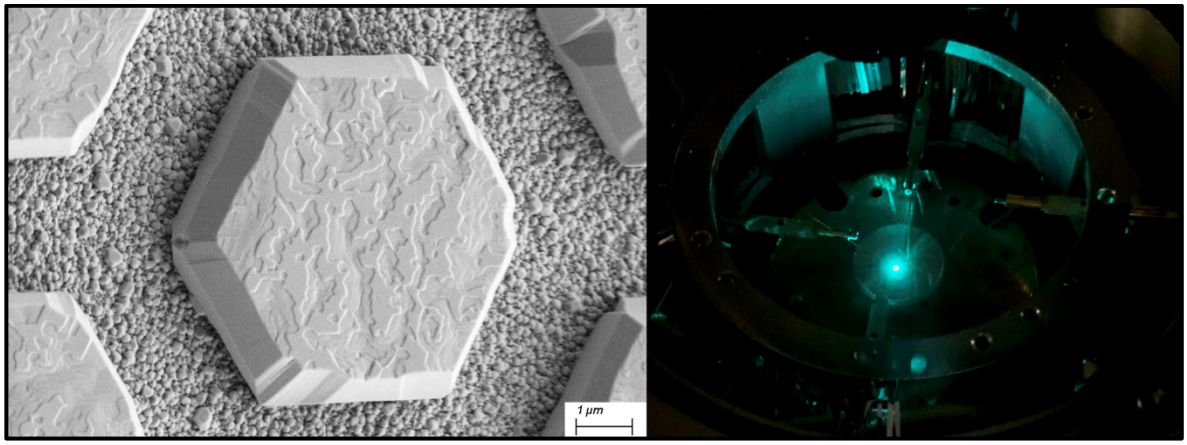
Abstract: Several technological challenges have prevented GaN-based micro-LEDs from finding application in mass market displays, despite their unique properties such as very high brightness and the very fast response time of GaN-based materials. The primary challenges have been the cost and complexity of lifting-off and transfer of LEDs from sapphire substrates to suitable supports as well as the lowered performance for tiny micro-LEDs caused by chemical etching that defines individual LEDs. Here we report demonstration of a complete process that solves these challenges with epitaxy and cleanroom technologies that are commercially available. The process begins with van der Waals epitaxy of 2D h-BN on silica masks with square, triangular and hexagonal patterns on sapphire substrates which define the micro-LED regions, then selective area growth of MQWs LED heterostructures. Ultra smooth crystalline sidewalls are obtained and because of the lack of vertical chemical bonds in the h-BN layer, simple mechanical lift-off and transfer is performed on an array of LEDs heterostructures down to ultra tiny size of 1.4 µm. Finally, transparent ITO p-contacts are deposited on LEDs with uniform lift-off, resulting in high brightness LEDs with size down to 8 µm.



1. Introduction

Micro-light emitting diodes (micro-LEDs) are a key display technology undergoing intense interest from research groups because of their importance to mass market technologies of the future such as virtual reality and augmented reality displays, as well as applications in large video displays. For micro-LEDs, gallium nitride-based (GaN-based) materials have advantageous properties that include high brightness, wide color range, excellent stability, long lifetime, and very fast refresh rate, which have the possibility of overcoming limitations of other materials systems such as liquid crystal and OLED displays.

The two main existing approaches for fabrication of micro-LEDs use top-down methods or bottom-up methods. In a top-down approach, after epitaxy, a dry-etch is used to define the size of the micro-LEDs. This approach unfortunately induces crystallographic defects, impurities, and dangling bonds that introduce trap states within the bandgap which act as nonradiative recombination centers [1]. This damage on the sidewalls leads to substantial reduction in performance and a significant challenge to viability at a high injection current density, which is particularly relevant for small chips [2]. On the other hand, reported bottom up approaches overcome the sidewalls damages but involve challenging processing steps and/or several steps of epi growth in different epi-systems [3][4].

For use in applications, GaN-based micro-LEDs are best removed from their sapphire substrate and placed on transparent supports or placed on reflective backings to increase light extraction efficiency. Options that remove epilayers from substrates that have been demonstrated include laser lift-off (where high cost excimer lasers are used to melt the bottom of the GaN epilayers through the sapphire) [5], chemical lift-off (which has been proven too slow to be practical and not environmental friendly) [6], and use of multi-sapphire nano-membranes (which require a complex process) [7]. An attractive alternative technology for lift-off that has attracted much attention is the epitaxy or deposition of 2D materials such as graphene or hexagonal boron nitride (h-BN) as a release layer with subsequent epitaxy of GaN-based 3D materials. The use of graphene as a release layer has been reported [8]. For commercial production, the graphene deposition processes require specific growth conditions and post-growth backing or extra epitaxy equipment. The advantages of 2D / 3D van der Waals (vdWs) epitaxy with h-BN are that the same epitaxy equipment and ultimately the same epitaxial run can be used for growth of the h-BN and the GaN-based epilayers and there are fewer processing steps. After a first demonstration in 2012 [9] for LEDs , h-BN / GaN vdWs epitaxy has been performed by our research group at the wafer scale [10], with demonstrations of solar cells [11], gas sensors [12], and LEDs [13]. In addition to devices, lift-off has been studied, establishing control of whether or not lift-off will occur [14] and a technique called self-lift-off and transfer (SLOT) has been demonstrated for transfer to copper supports [15].

In addition to lift-off, display technologies require that distinct addressable diodes must be separated physically. This is usually done by chemical etching, which has the drawback of generating nonradiative recombination centers in the sidewalls around defects due to etching damages. As a result the external quantum efficiency (EQE) decreases with decreasing size especially for ultra-small micro-LEDs that have large surface area-to-volume ratio [16].

Typically, a passivation layer is needed to reduce the effect of sidewalls, but it's not enough for complete recovery of LED performance.

To improve the crystal quality of the sidewalls and hence the device performances, selective area growth (SAG) techniques have also been explored [3]. Our research group has proposed a novel approach using conventional silica or other amorphous dielectric patterns such as silicon nitride. h-BN growth is then performed, which covers the sapphire surface with several nanometers of 2D h-BN and covers the dielectric mask with several nanometers of disordered BN. As a result, a single LED or array of LEDs can be detached easily from their substrate while no contamination from silica occurs since it is covered by h-BN.

One would not expect that 2D h-BN could be used in SAG due to boron readily bonding to silica glasses. Indeed, our previously reported results show that boron nitride deposited on silica is highly disordered under growth conditions favorable for h-BN epitaxy on sapphire [17]. Surprisingly, our group discovered [13] that subsequent to h-BN deposition, SAG of GaN alloys occurs only on the h-BN/sapphire surface, with few polycrystals on the disordered BN on silica masks. This resulted in LEDs with minimum size of 500 µm [18].

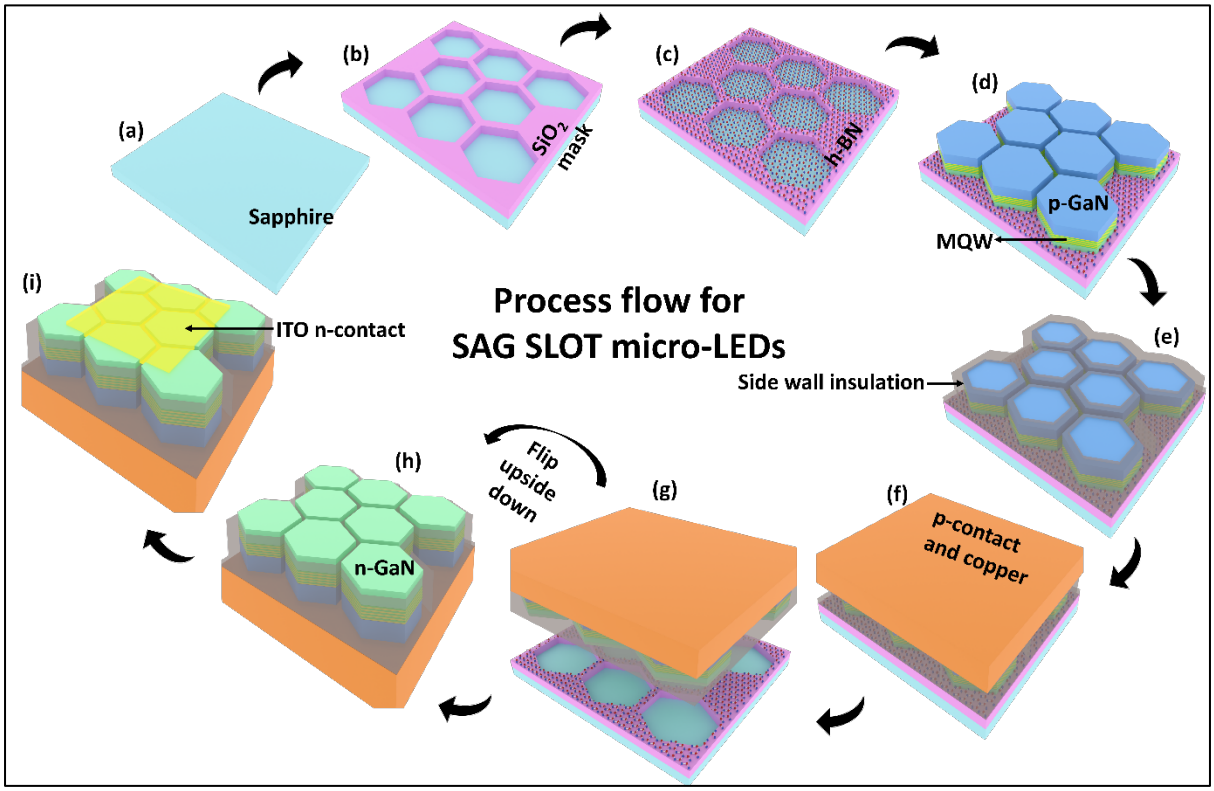


Figure 1. Process flow for the micro-LED fabrication. Figures showing (a) epi-ready sapphire substrate, (b) SiO_2 mask deposition by PECVD and patterning for growth, (c) non-selective growth of h-BN growth by MOCVD, (d) selective area growth of LED heterostructure by MOCVD, (e) LED's sidewall insulation by SiO_2 deposition and opening the top surface for p-contact (f) deposition of p-contact, seed layer and copper electroplating for SLOT process (g) lift-off and transfer to copper substrate, (h) micro-LEDs on copper, (i) deposition of top n-contact ITO on array of micro-LEDs.

In this paper, we apply this process to micro-LEDs of from 32 µm in diameter down to 1.4 µm, for three different mask opening shapes: square, hexagonal and triangular (Fig. 1). The

challenges that are studied and solved in this paper are (a) the selectivity and the quality of the micro-LED heterostructures in small selective openings and the smoothness of the sidewalls even for 1.4 μm micro-LED heterostructures, (b) demonstration of SiO_2 mask widths between 2 to 5 μm which provide perfect separation between the micro-LEDs, and where the high opening area to masked area ratio is favorable for reduction of the cost per chip, (c) the fabrication process for ultra-small micro-LEDs down to 1.4 μm, and (d) the liftoff and transfer of a range of shapes and sizes down to 1.4 μm.

The technology reported here offers advantages that can address some of important challenges associated with fabrication of micro-LEDs. After h-BN growth, the AlGaN/GaN buffer is ~600nm thick, leading to substantial reduction of the micro-LED total thickness (less than 1 μm) and hence the cost of the epi growth compared to GaN on sapphire. Next, thousands of micro-LED chips can be processed simultaneously since the liftoff can be done over a large surface (whole wafer). Additionally, the substrate can be reused after liftoff without any heavy CMP process. This approach is scalable as GaN-based wafer size increases, the only limitation is the growth chamber size and the handling capability of clean room equipment. Further benefits of this approach include vertical contacting, which eliminates current crowding in existing n-type side contacted devices. The simplicity of the process can reduce capital expenditure. Finally, the geometry of SAG micro-LEDs and transfer to metallic supports can also result in significantly improved thermal management as compared to GaN-on-sapphire and GaN-on-GaN.

2. Results and Discussion

2.1 Materials Growth and Characterization

Prior to the micro-LEDs growth, patterned SiO_2 substrate with openings of square, hexagonal, and triangular shapes were prepared. As shown by optical micrographs in Fig. 2, opening sizes ranged from 32 μm down to 1.4 μm separated by different SiO_2 mask widths (2 μm to 5 μm). For comparison of square, hexagonal, and triangular pattern sizes, the reported linear micro-LED size is the square root of the area of each opening.

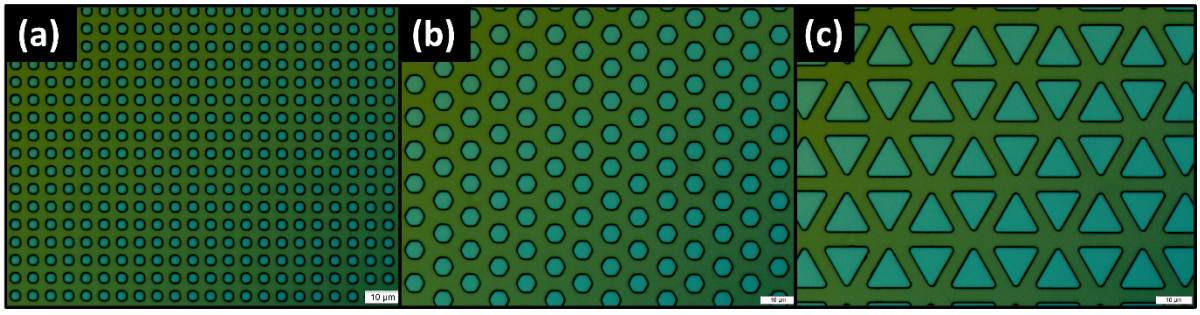


Figure 2. Optical micrographs of the SiO_2 mask with openings of different shapes (a) square (b) hexagon (c) triangle. The sea green color indicates openings while yellowish green color corresponds to the SiO_2 mask.

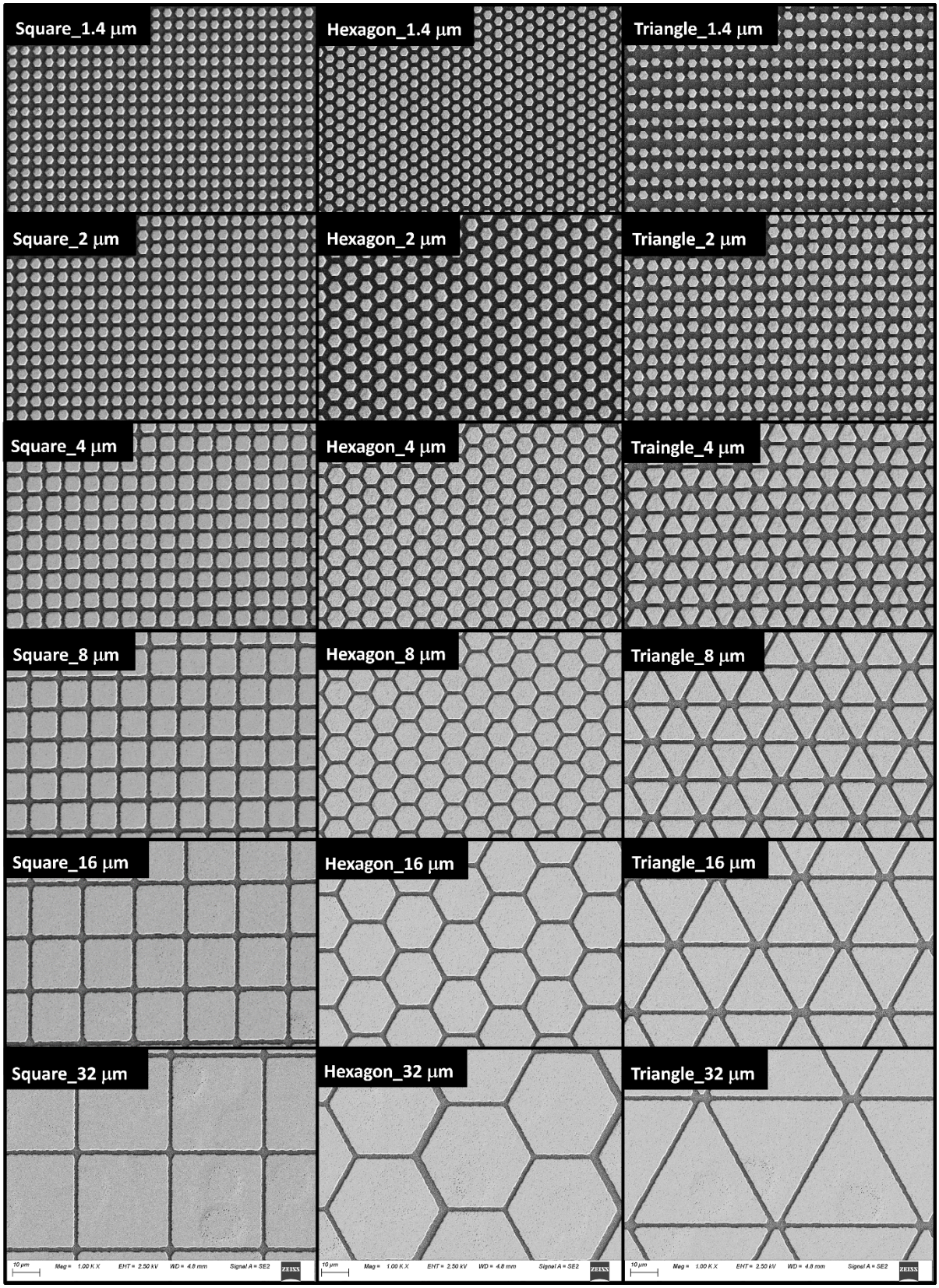


Figure 3. SE micrographs of SAG for square, hexagon and triangular LEDs of six sizes. For comparison of square, hexagonal, and triangular pattern sizes, the reported linear micro-LED size is the square root of the area of each opening All the images are shown at same magnification (1kX) and same beam column conditions.

Fig. 3 shows scanning electron micrographs (SEM) of SAG for square, hexagonal and triangle LEDs on different sizes from 1.4 μm to 32 μm. LEDs have grown selectively in the opening areas where layered h-BN is deposited and do not grow on randomly oriented BN on SiO_2. The LED structures show high quality selective area growth for mask widths as low as 2 μm. For each shape the micro-LED heterostructures are well-aligned with no sign of tilt or twist. It is worth noting that for opening size below 4 μm, the micro-LEDs heterostructures have hexagonal shape no matter the shape of the mask. The hexagonal shape is the most stable shape formation of the GaN based crystal. For easy use of photolithography in our case all the LEDs presented in this study are separated with a mask of 3 μm width.

Fig. 4(a) shows magnified SEM micrograph of 1.4 μm micro-LEDs, the top surface morphology of these LEDs heterostructures is smooth with no observable V-pits. This suggests the possibility of uniform current injections to individual LEDs, that could result in good electrical and optical performance. The small granular deposition on the mask are AlGaN deposits, as shown in Fig. 4(a), is related to the short surface migration of the adatoms on SiO_2, however on gas phase the D/K (D is the diffusion coefficient of the active species, k is the reaction constant) insure good selectivity for indium, gallium and aluminum active species [20]. In addition to that, the sidewalls of these LED structures (Fig. 4(b)) maintain well defined crystallographic facets and a smooth surface, irrespective of the mask width, evidence of high quality of selective area growth.

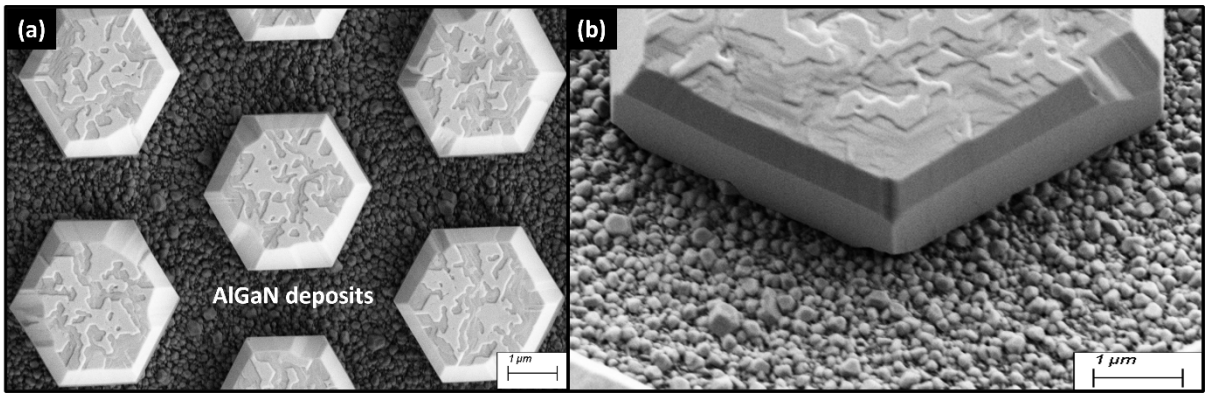


Figure 4. (a) SE micrograph of hexagonal shaped LED heterostructures of size 1.4 μm. (b) SE micrograph of the tiled sample showing smooth growth sidewalls .

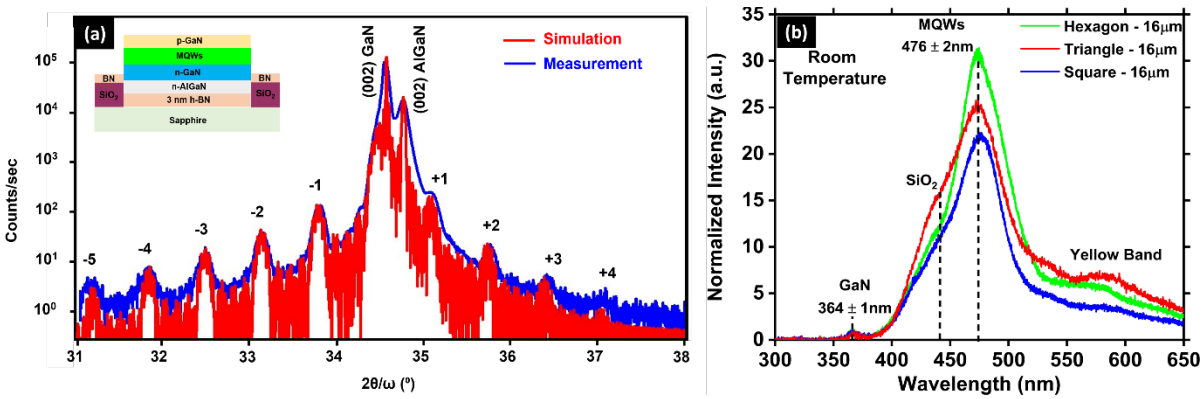


Figure 5. (a) XRD of the LED heterostructure with inset of device structure, (b) Cathodoluminescence spectrum of 16μm micro-LED of hexagon, square and triangle shape.

HR-XRD $2\theta - \omega$ scans, are shown in Fig. 5(a) which have InGaN satellite peaks up to fourth order as well as the peaks corresponding to the GaN and AlGaN layers. The 5 QW structure consists of a 11.5-nm-thick GaN barrier layer and a 2.4-nm-thick InGaN quantum well layer with an In mole fraction of 15% (as extracted from X-ray simulation). To understand if the number of facets and the angle between two facets affect the growth rate and variation in content of In incorporation in the MQWs, depth resolved cathodoluminescence (CL) spectra for the LEDs structures of the same area (corresponding to size 16 μm) were recorded. The results shown in Fig. 5(b) were obtained after removing the background noise and normalizing the resulting spectrum with respect to GaN peak. As shown the LEDs structures exhibit a GaN near band edge emission peak at 364 nm and yellow band peak near 575 nm. A small shoulder in the spectrum obtained near 450 nm corresponds to the signal from SiO_2 mask [21]. InGaN MQW emission peak at 477±2 nm is observed which corresponds to little over 15% In content in the quantum wells, as predicted by XRD measurements. However, for all the three shapes same MQW emission wavelength is obtained i.e., the MQW peak wavelength doesn't depend upon shape of the LED. Interestingly, the LEDs shape do affect the peak intensity, hexagonal LEDs show highest intensity followed by triangle and then square LEDs. This originates due the highest and lowest photon extraction efficiency of hexagonal and square shape respectively [22,23].

2.2 Self Lift-off and Transfer Process

Our group has reported [15] that wafer scale lift off can be achieved for GaN epi-layers grown on 2D h-BN. This process of self lift-off and transfer (SLOT process) involves deposition of a Ti (10 nm)/Au (15 nm) seed layer followed by 30 μm copper deposition via electroplating. The self lift-off of the GaN epi-layers and its transfer to copper substrate upon heating stems from thermal stress generated at the h-BN/epilayer interface introduced due to high thermal expansion coefficient of copper. This causes epilayers to break the weak van der Waals force adhesion at h-BN/epilayer interface and transfer to copper substrate.

For our grown micro-LED heterostructures, bottom n-AlGaN/n-GaN layer thickness (~600 nm) exceeds the SiO_2 mask thickness (~450 nm). Ti/Au p-contact layer deposition for SLOT process on this structure would risk in short circuiting of LEDs heterostructures. Thus, SLOT process was modified to mitigate this risk by adding a silica electrical insulation step as shown in a schematic of the process flow in Fig. 1. Fig. 6 (a to d) shows SE micrograph of the complete process cycle of the device fabrication. Figure 6 (e) and (f) show the images of back side and front side of 1cm*1cm lifted-off membrane. Back side corresponds to the copper and front side corresponds to face containing nearly 1 million micro-LEDs of different shapes and sizes.

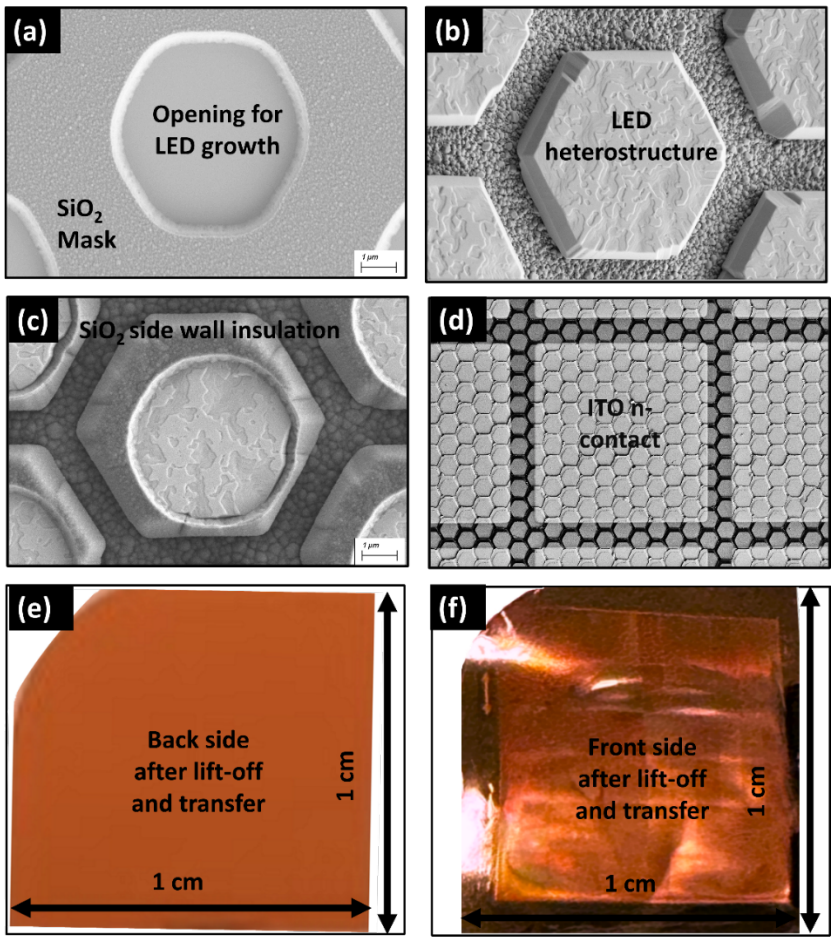


Figure 6. Images of sample at different stages of fabrication process. SE micrograph showing (a) the SiO_2 mask and opening for LED growth. (b) micro-LED heterostructure after growth, (c) deposition of SiO_2 side wall insulation layer (d) deposition of ITO n-contact after lift-off on an array of micro-LEDs. All these SE micrographs corresponds to LED of size 8μm. Photographs showing (e) back side (copper) and (f) front side (LEDs) of 1cm*1cm lifted-off membrane containing approximately 1 million micro-LEDs of different shapes and sizes.

The SiO_2 deposition step on the sidewalls of each device adds a mechanical resistance to lift off which is proportional to the circumference of the micro-LED. The bonding of the micro-LEDs to the copper above them is proportional to the area of the LEDs. Therefore, one could anticipate that lift-off would be easier for larger micro-LEDs. We found that the liftoff was 100% successful for 100 μm down to 8 μm micro-LEDs. However, many micro-LEDs of size 4 μm and below did not lift off. In addition, the current mask design is not optimal for pads deposition on ultra-small LEDs. For these reasons our device performances presented below are for micro-LEDs down to only 8 μm diameter. To increase the lift-off yield of micro-LEDs 4 μm to 1.4 μm, thick SiO_2 mask will be deposited and a new mask design for process fabrication is under investigation.

2.3 Optical and Electrical Device Characterization

For electrical characterization of micro-LEDs from size 32 μm down to 8 μm, arrays of micro-LEDs have been covered with ITO as common n-contact . The size of square ITO contacts was 100 μm, which covered several devices (9 device of size 32 μm , 32 devices of size 16 μm and

90 devices of size 8 μm), therefore reported current densities are averages over many devices.

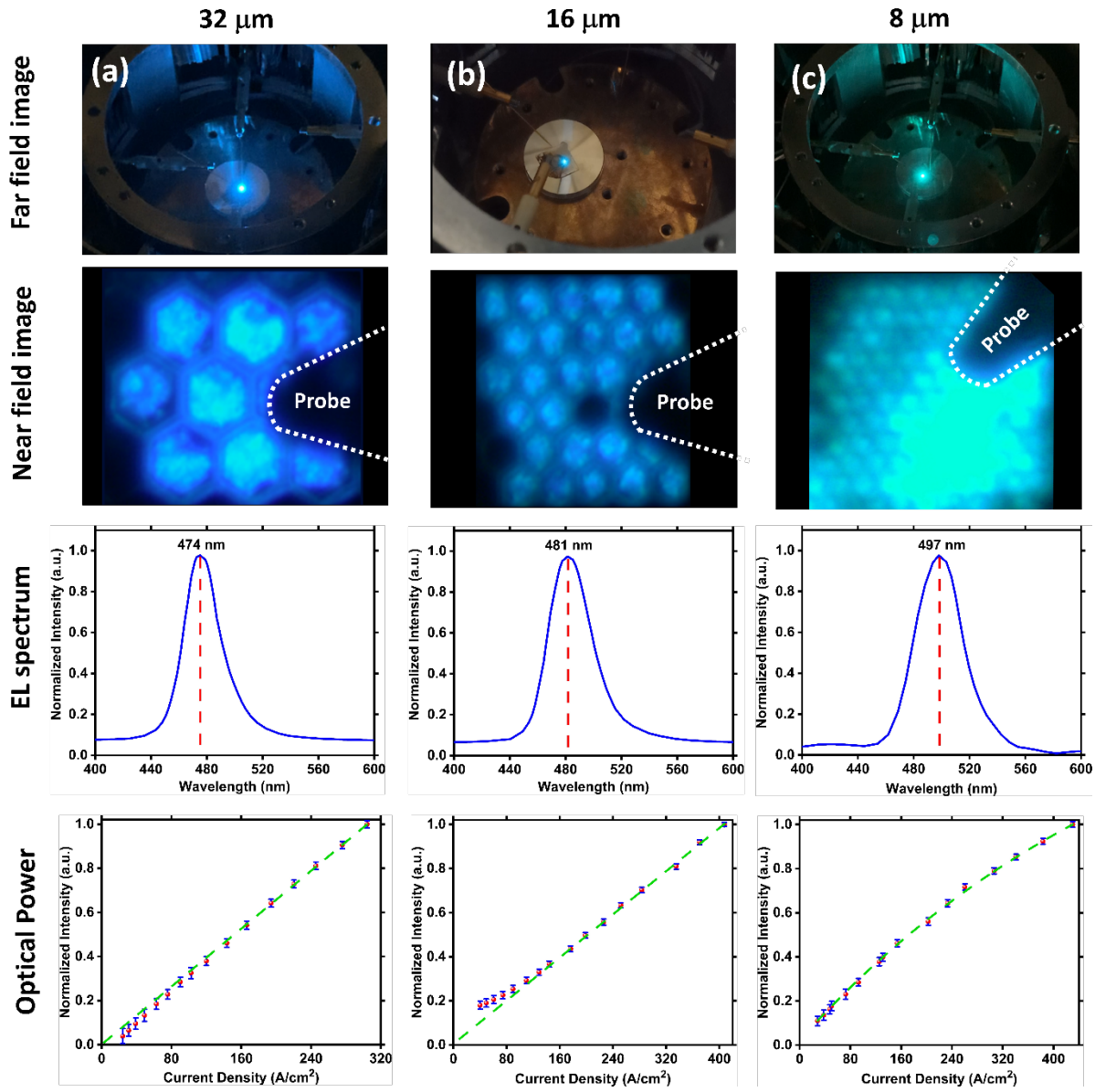


Figure 7. Far field image, near field (near threshold voltage), electroluminescence spectrum, and normalized optical power output vs current density characteristics of (a) 32μm, (b) 16 μm and (c) 8 μm micro-LED.

Fig. 7(a) are camera images, showing far-field non-saturated LED emission from 32 μm , 16 μm and 8 μm size micro-LEDs. There is a noticeable color difference in micro-LED color. It is likely that the color difference is primarily related to the SAG effect which creates a slight thickness enhancement by decreasing the opening sizes and keeping the same mask width. As a result, the quantum well thickness increases and leads to the red shift. This interesting result shows that SAG can generate LEDs heterostructures emitting at different colors within the same wafer or on different wafers within the same epitaxial run by adjusting the size of the openings as in our case or the size of the mask width that we believe would have the same effect. Fig. 6(b) shows near field microscope images of LED emission near threshold so as to produce a non-saturated image. Note that the dark area in each picture is due to the electrical probe blocking light from the micro-LEDs below it. Fig. 7(c) shows electroluminescence

spectra quantifying the wavelength shift evident from different sizes. For the 4 μm, 2 μm and 1.4 μm size micro-LED, the MQW peak emission wavelength obtained from photoluminescence are 500nm, 510nm and 520nm respectively. Fig. 7(d) shows normalized optical power output with increasing current density. From these figures we see that the for 32 μm and 16 μm optical power output linearly increases with increasing current densities. However, for 8 μm micro-LEDs we observe droop in optical power output beyond current density of 350 A/cm^2. Absence of optical power droop for 32 mm and 16 mm LEDs could be attributed to better thermal management due to high thermal conductivity of copper. However, as the LED size decreases, LED contact area to copper (via p-contact and seed layer) decreases due to increase in passivation area, which act as deterrent to thermal conduction, this could explain the observed droop in optical power for 8μm LEDs.

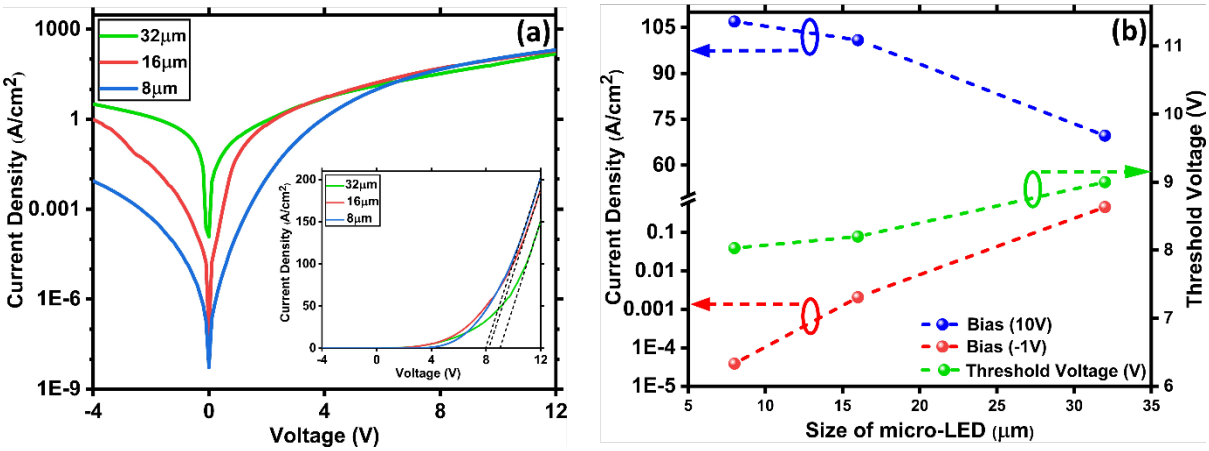


Figure 8 (a) Graph showing variation of current density with voltage for 32, 16, and 8 μm width micro-LEDs on log scale (with inset of the same graph on linear scale) (b) Graph showing variation of current density (at 10V and -1V bias) and threshold voltage with size of micro-LED.

Fabricated micro-LEDs were finally tested for their electrical performance and corresponding results are shown in Fig. 8. Fig. 8(a) show the current density variation for 32 μm, 16 μm and 8 μm micro-LEDs with the applied bias on log scale (inset linear scale). Clearly these LEDs show expected diodic behavior.

As expected, when the size of micro-LEDs is reduced from 32 μm to 8 μm, the overall spreading resistance for current injection decreases due to the decrease in cross-sectional area. This leads to an increase in current density in smaller size micro-LEDs [16]. This phenomenon also explains the reduction in threshold voltage from 9V for 32um micro-LED to 8V for 8um micro-LED as shown in Fig. 8(a). This threshold voltage of 8V is much higher than the typical value of around 4V for GaN/InGaN blue LEDs. The reason to almost double threshold voltage is attributed to the presence of highly resistive AlGaN buffer layer [15] as well as the high mismatch between the work-function of ITO n-contact and electron affinity of AlGaN layer. This leads to formation of Schottky barrier for electrons (between 1.7eV - 2.2eV) at the metal semiconductor interface.

Interestingly, as evidenced in Fig. 8(b), the reverse current density, at reverse bias of 1V, continuously decreases by ~4 order of magnitudes as micro-LED size decreases from 32 μm

to 8 μm. This behavior is opposite to what has been reported on micro-LEDs fabricated by etching [24], i.e. first decrease and then increase in the current density with decreasing size. This could be attributed to a higher crystalline quality of the sidewalls with less nonradiative defects obtained due to SAG as compared to the micro-LEDs prepared by etching process.

3. Conclusions

We have demonstrated epi growth of micro-LEDs heterostructures down to 1.4 μm size on 2" wafers using SAG technique by MOCVD combined with the vdWs epitaxy on h-BN. A complete process fabrication, liftoff and transfer of ultra-small micro-LED arrays has been successfully demonstrated with high brightness. The increasing current density as LED size decreases while the decrease of leakage current with decreasing the size of LEDs down to 8 μm are good evidences of the excellent surface quality of the sidewalls formed by crystallographic planes even for ultra-small micro-LEDs. With h-BN serving as a release layer, devices are simply mechanically removed and can be bonded to foreign substrates, a copper support in our case for better and homogeneous injection of current into the micro-LEDs. This novel approach demonstrates the ability to design micro-LED with different wavelengths on the same wafer or different wafers in the same growth run, by adjusting the size of the opening or the size of the mask width. This novel approach of micro-LEDs fabrication could be an alternative way to produce micro-LEDs with better control, high yield and low cost.

Because the process is done with nearly commercial epitaxy systems with a single epitaxy run and with standard microfabrication equipment, the simple process is highly attractive for application, and demonstrates the utility of 2-D materials for integration into industry compatible processes.

4. Methods.

SiO_2 mask fabrication was done in a two-step process on an epi-ready sapphire substrate. In first step, a 400 nm SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) on a 2-inch sapphire wafer, onto which patterns were defined by photolithography. In a second step, SiO_2 was etched by buffered oxide etchant to open the areas for SAG.

Next, epi growth of 3 nm thick h-BN was performed on patterned sapphire substrates at 1280°C. The growth conditions for h-BN were same as that reported for unpatterned sapphire [19]. Then, a 200 nm thick n-AlGaN layer with an Al mole fraction of 14% was grown at 1100°C for nucleation and as interfacial buffer between the 2D h-BN and the rest of the epitaxial film. Then LED heterostructure was grown which consists of a 300 nm thick Si-doped n-GaN layer, 5-periods of InGaN/GaN multi-quantum wells (MQWs) and a 175 nm thick Mg-doped p-GaN layer. The h-BN, AlGaN interface layer and the LEDs heterostructures were grown in the same run using a Aixtron MOVPE CCS 3x2'' system on (0001) 2-inch sapphire wafers with SiO_2 patterns prepared as described above.

Device fabrication process begins with the insulation step which involves deposition of 600 nm of SiO_2 on the grown LED heterostructure. While this step serves for isolating devices it also ensures sidewall protection from any external contamination of the facets beyond the patterning SiO_2 mask height. SiO_2 was then etched in the center of the micro-LED structure

opening a p-contact region (Fig. 1e & Fig. 6c). Then, a Ni (15 nm)/Au (5 nm) p-contact was deposited and annealed at 600°C in an O_2 environment to form an ohmic contact. Following this, metal seed layer deposition and copper electroplating (Fig. 1f) were performed for the SLOT process. Subsequently, liftoff (Fig. 1g) and transfer to copper substrate was performed (Fig. 1h). Finally, 100 μm*100 μm square, n-contact ITO was deposited on front face of micro-LEDs on copper (Fig. 1(i) & Fig. 6(d)) and final devices with front ITO n-contact and back copper p-contact were obtained.

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Declaration of competing interest

The authors declare that they have no conflict of interest.

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