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A Self-Reconfigurable Highly Linear and Robust X-Band MMIC GaN LNA

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Abstract — In this article, a two-stage reconfigurable X-Band low noise amplifier is presented. This is the first time that an LNA is presented which can be tuned from a high sensitivity (low noise figure) but medium input saturated power configuration, to a slightly degraded noise figure but high input saturated power configuration. This robust LNA, developed with the D01GH technology from OMMIC, meets electronic protection requirements in that it offers a low noise figure, and is still able to operate under elevated RF signal jamming conditions. The proposed system, when configured in a low noise figure mode, achieves an average noise figure ($NF_{50\Omega}$) of 1.5 dB over 40 % bandwidth centered on the X-Band. In its high linearity mode, 10 dB improvement is achieved on the input compression point (IP_{1dB}) measured at 9 dBm, at the price of 0.4 dB increase in noise figure. The small signal gain is greater than 18 dB and the return losses are better than -10 dB in both configurations over the complete frequency band under consideration

Keywords—Low-noise amplifier, LNA, Electronic Protection, Electronic warfare, Gallium Nitride, HEMTs, Linearity, Tunable, Reconfigurable, MMICs.

I. INTRODUCTION

GaN HEMT active devices offer higher linear performance and robustness than their GaAs or SiGe counterparts. Widely used for RF power modules (PAs), GaN HEMTs have also attracted the attention of RF engineers for the design of low noise amplifiers (LNAs). Thanks to the properties of wide bandgap GaN material, this technology meets robust low noise receiver systems requirements, as developed in modern military radar, altimetry detection or space communication front-ends, requiring systems capable of operating at high RF input power. GaN-based receivers are also advantageous for their ability to withstand high jamming powers without being degraded or destroyed. This new approach of utilising a robust LNA design in the front end, negates the requirement for the traditional protection technique of implementing a specific limiter before the LNA: the use of a smaller and therefore less noisy integrated power limiter, or even the absence of a protection device before the LNA becomes possible. The size of the active device is a critical parameter in designing a system that can still operate at high RF power. A compromise must be made between the

number and the width of the gate fingers of the GaN active device. This compromise determines two crucial parameters which are the noise figure ($NF_{50\Omega}$) and the linearity (compression point at 1dB, P_{1dB}) of the LNA [1]. The importance of decreasing the noise figure (NF) to increase the detectivity of the systems is known, but the resulting premature compression (under high RF power at the amplifier input) leads to a very significant increase in NF, making the system blind [2]. Linearity cannot be set aside at the risk of rendering the device inoperative under strong RF input signal conditions.

Hence, for a robust LNA, it is preferable to oversize the active device and its biasing to increase its performance in linearity and survivability [3]. This will be done to the detriment of the noise figure which will be penalized by the oversized choice of the size and the polarization of the transistor. We propose here to reconcile the noise and linearity performances of GaN technology in an original adaptive approach, applied to a two-stage X-band LNA. The principle is to select the transistor of the first stage of the LNA on noise figure and [S] small-signal parameters considerations, but also by considering the possibility of increasing its input 1 dB compression point IP_{1dB} by modifying only the quiescent points with minimal impact on the characteristics of the [S] parameters (gain and return losses). The selection of the transistor is of prime importance to allow such a change in the DC biasing and to reach a low $NF_{50\Omega}$ or high IP_{1dB} . The second stage is implemented in the same way, but now considering the output power of the first stage to maintain a linear mode of operation; $NF_{50\Omega}$ will not be a minimum for this second stage, but according to Friis formula, has less impact on the overall system noise figure for the reception chain.

II. TWO-STAGE LNA DESIGN

The GaN technology used for this original study of adaptive LNA is the OMMIC D01GH MMIC process on silicon substrate. It provides HEMT devices with a transition frequency of 110 GHz, a high breakdown voltage of 36 V, and a power density as high as 4 W/mm. This process is suitable for PAs, robust LNAs as well as transceiver modules.

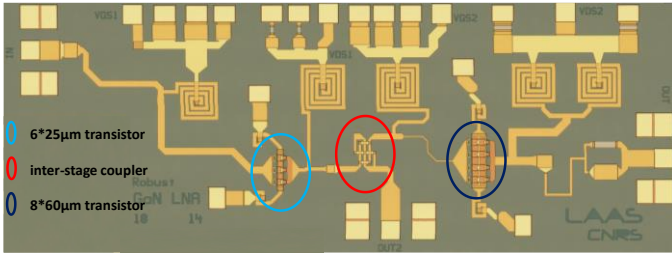


Figure 1 : Layout of the two-stage reconfigurable X-band LNA

In order to achieve the best possible robust LNA, the methodology implemented is to optimize each stage separately.

Therefore, in order to achieve the lowest possible system noise figure ($NF_{50\Omega}$), the transistor selected for each stage is different in size with the first stage having a nominally small transistor ($6 \times 25 \mu\text{m}$) for an X-Band application. According to Friis' formula, the first stage is critical in the LNA design procedure, but it is not necessarily the limiting factor in terms of system linearity. The second and eventually third stages are more constrained by the linearity issue due to the more important RF power level at their input port, because of the gain of the previous stage. A bigger transistor ($8 \times 60 \mu\text{m}$) is then selected for the second stage, with an appropriate DC bias in order to achieve a coherence between the output 1dB compression point (OP_{1dB}) of the first stage and the input 1dB compression point (IP_{1dB}) of the second stage. The input and output matching networks of Figure 1 are achieved so as to obtain a constant small signal gain, and input/output return losses better than -10 dB. The interstage network targets 25Ω load lines instead of 50Ω to achieve better overall gain but also to increase the 1 dB compression point by only tuning the gate DC biasing of each transistor (first and second stage). The interstage coupler is used to sense the RF power level and to change the quiescent points between low NF mode and high IP_{1dB} mode, with a dedicated PCB circuit.

III. RECONFIGURABLE LNA

The electrical circuitry on chip (X-band LNA MMIC) and on PCB is depicted in Figure 2. A coupler is used at the inter-stage of the MMIC LNA. It is connected to an external RF-DC converter on the PCB. It permits the detection of the RF power level for bistable switching between the two states (low NF and high IP_{1dB} biasing modes). Unconditional stability is achieved on the MMIC chip (frequency above 1 GHz), and on the PCB for the lower frequency band.

The proposed LNA is designed to operate under two distinct biasing modes: a nominal low noise mode with $[V_{GS1} = -0.9V \ \& \ I_{DS1} = 26mA] / [V_{GS2} = -1.1V \ \& \ I_{DS2} = 54mA]$ when the input RF signal is at a low or moderate power level, and a high linearity mode with $[V_{GS1} = -0.25V \ \& \ I_{DS1} = 66mA] [V_{GS2} = -0.6V \ \& \ I_{DS2} = 114mA]$ when the RF signal exceeds a set power level. The LNA is then still able to operate in its linear region by increasing its IP_{1dB} . In addition to the ability to operate in a linear mode under high RF input power conditions, the LNA can also withstand very high-power RF signals before destruction occurs without using a limiter.

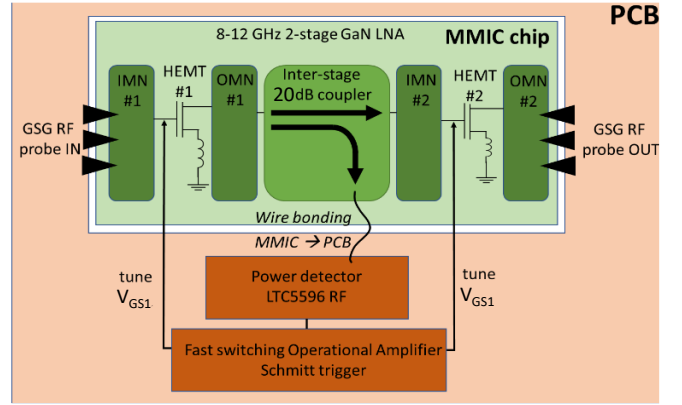


Figure 2 : representation of the MMIC chip (X-band 2-stage LNA) with the PCB circuit for power detection and DC gate bias triggering between the low NF and high IP_{1dB} mode. Drain biasing and electrical topology details are not shown.

Due to the transistor's dimensions and the interstage matching consideration, the drain voltages are each set to a constant value ($V_{DS1} = 6V / V_{DS2} = 15V$). One of the main challenges lies in the choice of the transistor quiescent points conditions which allow invariance of the small-signal parameters (gain and input-output reflexion coefficient within the 8-12 GHz frequency band) during the design steps, independent of the mode of biasing used. Then the matching network topologies are also selected to minimize the impact of the previous choice. Return losses less than -10 dB and small-signal gains greater than 20 dB (with only 0.3 dB variation between the two operating modes) are illustrated in Figure 3 and Figure 4 respectfully. Also, during the self-reconfiguration from a DC quiescent point to the other on, the phase of S_{21} only moves by 7 degrees. This phase shift does not harm BPSK or QPSK modulation schemes.

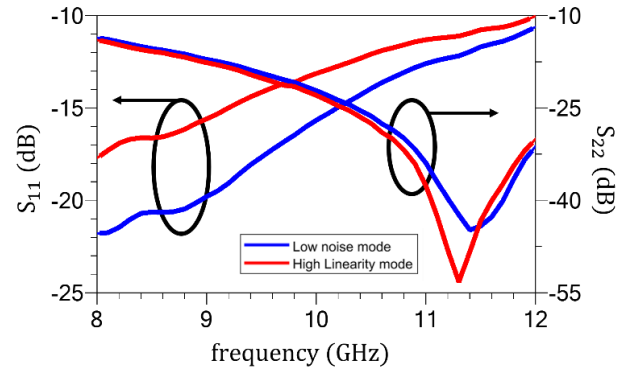


Figure 3 : measured input and output return losses under the two operating modes; low NF (blue) and high IP_{1dB} (red).

As shown in Figure 4, an increase of 10 dB is achieved on the 1 dB compression point (P_{1dB}) between the two selected quiescent points, which is all the more interesting as it operates at constant gain. While an input 1 dB compression (IP_{1dB}) level of -5 dBm in low noise mode is achieved, it reaches +5 dBm in high linearity mode ($IP_{1dB\#A}$). Consequently, and in a way that is irrelevant for the study of these amplifiers in reception, the output compression point (OP_{1dB}) then increases from 15 dBm to 25 dBm.

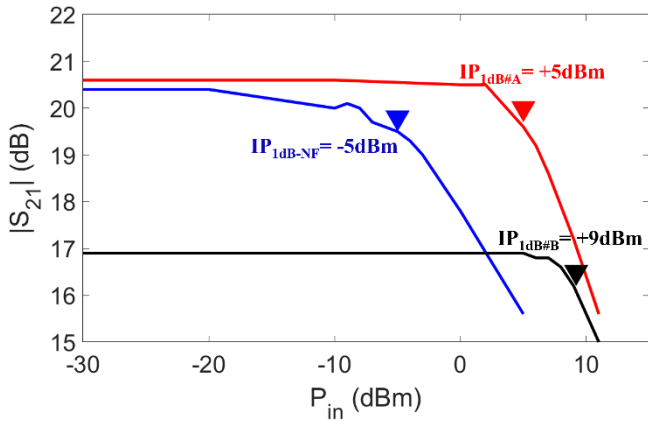


Figure 4 : Measured small-signal gain versus the input power at 10 GHz. IP_{1dB} is extracted for two quiescent points (low NF- blue plot, high $IP_{1dB\#A}$ /constant gain- red plot). Black plot represents the highest $IP_{1dB\#B}$, but with reduced S_{21} .

It should be noted that 14 dB improvement on $IP_{1dB\#B}$ is measured for the ultimate high linearity biasing in Figure 4 (black plot for $V_{GS1} = -0.1V / V_{GS2} = -0.1V$), at the cost of a degraded small-signal gain by 4 dB. The input compression point can reach $IP_{1dB\#B} = 9$ dBm. Surprisingly, the output compression point remains unchanged, a consequence of the sizing of the last stage transistor, and of its capacity to deliver its maximum power.

The noise figure is measured with a PNA-X N5244B, operated with option 029 for accurate noise measurement.

As shown on Figure 5, the noise figure increases by 0.5 dB between the two operating modes, as expected from CAD simulations. This is not excessive if we consider the increase in the power level applied to the input port while the LNA still operating in linear mode. Moreover, the biasing strategy as proposed for the 14 dB improvement on IP_{1dB} only degrades the $NF_{50\Omega}$ by 0.6 dB (+0.1 dB regarding NF associated with high $IP_{1dB\#A}$).

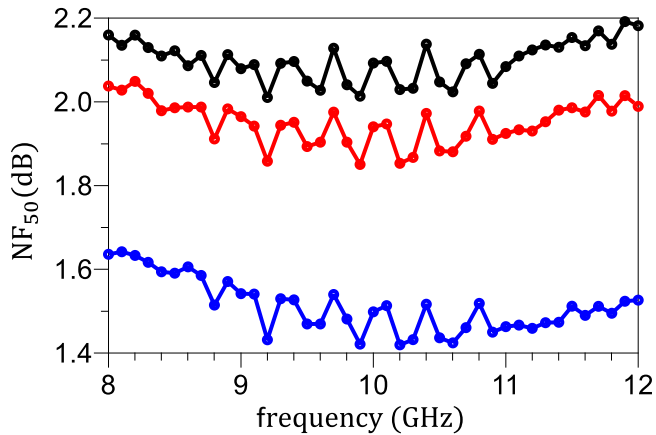


Figure 5: measured Noise Figure over 8-12 GHz for the 2-stage GaN LNA: blue plot is for NF quiescent point, red plot is for high $IP_{1dB\#A}$ quiescent point, and black plot is for high $IP_{1dB\#B}$ quiescent point.

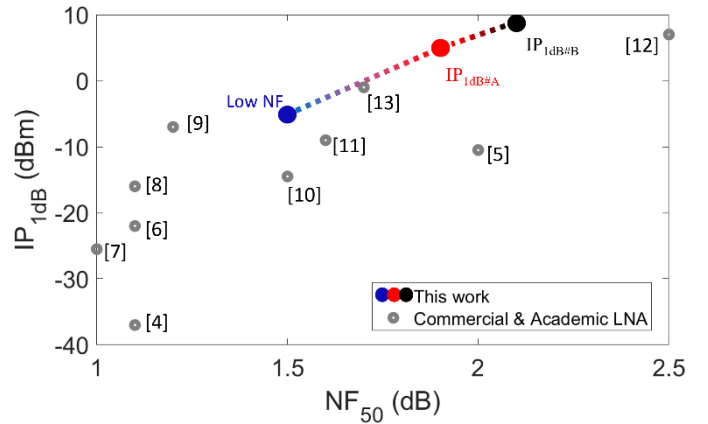


Figure 6 : state of the art for X-band GaN LNAs, considering the noise figure plotted versus IP_{1dB} (at 10 GHz). This work is depicted by the solid lines between the different operating modes; low NF (blue), high $IP_{1dB\#A}$ (red), or ultimate $IP_{1dB\#B}$ (black).

IV. COMPARISON AND DISCUSSION

The proposed strategy for designing a reconfigurable LNA capable switching from a low-noise to a highly linear configuration, while still operating in constant-gain small-signal linear RF mode, is compared in Figure 6 with the state of the art of the commercial or academic conventional GaN-based solutions. The input compression point is plotted versus the noise figure for multi-stage LNAs (small-signal gain greater than 20 dB) operating in the X-band. This work on a 2-stage LNA is positioned as the state-of-the-art of this trend between low NF_{50} and high IP_{1dB} from the investigation carried out on GaN technology. However, beyond this observation, this work takes advantage of being adaptive to the RF conditions under which the receiver operates. This is represented by the solid line between the two situations, low NF (moderate IP_{1dB}) and enhanced linearity $IP_{1dB\#A}$ (slightly degraded NF, but still at the state-of-the-art).

Table 1 : comparison of MMIC GaN multi-stage LNA (2 or above) at 10GHz from literature and from manufacturer portfolios. OP_{1dB} are listed below, instead of IP_{1dB} as computed in Figure 6.

Ref	Frequency Band (GHz)	NF (dB)	OP_{1dB} (dBm)	Gain (dB)	S_{11} & S_{22} (dB)
Proposed LNA	8-12	1.5-2	15-25	20.5	<-13
[4]	8-12	1.1	17	55	<-12,7
[5]	8-12	2	19.5	31	<-10
[6]	6-18	1.1	8	25	<-15
[7]	7-11	1	5.5	32	<-12
[8]	8-12	1.1	10	33	<-12
[9]	7-12	1.2	11	19	<-10
[10]	6-18	1.5	10.5	26	<-10
[11]	8-12	1.6-1.75	13	23	
[12]	7-12	>2.5	20	14	<-10
[13]	8-11	1.6-1.95	23	22-30	<-13

The comparison of LNAs cannot be limited to only two parameters, namely the NF_{50} and the P_{1dB} , and it is also necessary to consider the gain and the return losses: more details are presented in Table 1.

When the initial circuit evaluations were performed, the switching between the two modes was operated manually (tuning the DC biasing of gate voltage for each stage of the LNA). The MMICs chips are implemented on a PCB circuit which manages automatically the switching conditions of the gate voltages of the transistors (Figure 2). According to the power derived from the coupler, and applied to the RF-DC converter, the electrical circuit on the PCB acts as a trigger between two biasing modes as discussed. The RF power level $P_{NF \rightarrow High P_{1DB}}$ switches from low NF mode to high P_{1dB} state. The trigger that brings the LNA back to its low NF state operates at $P_{High P_{1DB} \rightarrow NF}$, which is lower than $P_{NF \rightarrow High P_{1DB}}$ (hysteresis with all levels adjustable on PCB). Tests of robustness versus RF jamming signals have been performed at 10 GHz, using different RF step stress profiles (5 minutes per step). This study was developed on two types of single-stage MMIC LNAs from the same chip, whose design information and performance are given in [14]. One LNA was designed to operate at high IP_{1dB} , with a slightly degraded $NF_{50\Omega}$, while the second LNA was designed according to the proposed strategy of self-reconfiguration versus the incident RF power. It was concluded that the self-reconfiguration of the quiescent point gives the LNA under test better robustness to EM aggression, in addition to the increase in the compression point. Up to 30dBm was applied to the LNA input with only 0.1 dB degradation on $NF_{50\Omega}$, while LNA destruction occurs at 35 dBm input RF power [15]. Further tests on two-stage LNAs are still on-going.

V. CONCLUSION

For the first time, a reconfigurable GaN MMIC 2-stage LNA is presented which allows the electrical and noise performance of the amplifier to be tuned from a low-noise configuration to a rugged highly linear one. This is performed in a reversible manner, according to specific DC gate biasing of the transistors, selected for these two operating modes. This new strategy of design for an LNA permits an increase in the compression point of the amplifier while still maintaining a constant gain and stable return losses. The LNA operates between 8-12 GHz, and features a small-signal gain of 20 dB, a noise figure lower than 1.6 dB over the operating bandwidth of the LNA, and a IP_{1dB} of 5 dBm. The input 1 dB compression point can be improved by 10 dB (and also 14 dB under specific biasing conditions at the expense of a reduced small-signal gain), with only 0.4 dB degradation on the noise figure when the gate bias is switched to the high-linear operating mode. The LNA can thus operate under these two low NF or high IP_{1dB} conditions while still maintaining the system operating in its linear power region. Outside this linear region, the receiver can withstand higher RF input power before destruction (35 dBm), without using an external limiter thus improving the overall noise figure of the receiver.

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