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Flip-Chip Low inductive and EMC optimized PCB Power Module

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Abstract—This paper presents an original power module based on printed circuit board technology. Two designs are compared, one based on flip-chip technology and the other based on conventional technology. The advantages of the flip-chip design are in term of stray inductances (sub nanohenry) and in term of EMC behavior are detailed. This kind of design is particularly adapted for GaN or SiC devices and their very high dv/dt and di/dt values during switching operation.

Keywords—Flip-Chip, MOSFET, Sic, GaN, Power module, EMC.

I. INTRODUCTION

In recent applications and in many specific markets, such as automotive, aerospace, energy and many other technologies, the power required to be delivered by the energy converters is constantly increasing. This demand is accompanied by the need to increase power density. This is made possible by increasing the switching frequency of converters, which mainly minimizes the size of passive elements. The semiconductor materials used in switches remain the heart of power converters. Technological advances in these materials could lead to significant gains in converter compactness, efficiency, and reliability [1]. Silicon (Si) has dominated the semiconductor market for years, and still does. However, Si component technologies now seem to have reached their theoretical limits. This necessitates a switch to other semiconductor materials, to regain potential increments in conventional power electronics performance (efficiency, compactness, power, voltage rise, switching speed rise, etc.). In this context, components based on silicon carbide (SiC) and gallium nitride (GaN) are competing with Si thanks to their advanced properties [2]–[4].

Nevertheless, power switches are in direct interaction with their environment and package. To take full advantage of the excellent performance of wide-bandgap semiconductors, package enhancement has therefore become a necessity [5], [6]. As increasing switching speed stimulates parasitic elements in the package, we will present the various parasitic elements that affect switching and the EMC behavior of the system.

This article presents an original power module based on a printed circuit board (PCB). It features low stray inductance (sub nanohenry) using a flux compensation based on a flip-chip design.

Other power modules, such as the one proposed in [7], [8] offer flux compensation. In the module propose in [8], the power switches are placed in windows in the PCB and soldered to the DBC. Interconnections between chips are made by bonding wires. A plastic case is used to cover the package. A partial elimination of flux will take place since the input and output currents of the module are in opposite directions. Despite the aforementioned advantages enabling a significant reduction in switch loop inductance, the presence of bonding wires results in electrical limitations.

The flip-chip design also allows careful design of parasitic capacitive elements to reduce the common-mode current spectrum. Part II describes the power module and explains flux compensation. Part III focuses on the indicative part and the common-mode current in this power module.

II. LOW INDUCTIVE POWER MODULE

This Power Module consists of a single inverter arm. As shown in Figure 1, flip-chip technology enables the source of the HS transistor to be connected directly to the drain of the LS transistor, with the aim of minimizing the surface area of the switching loop and hence its inductance.

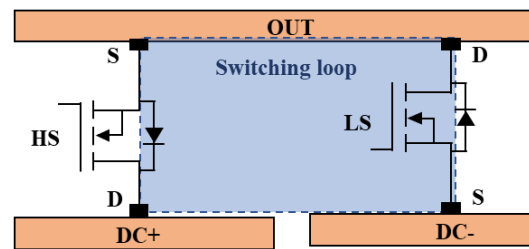


Fig. 1. Power loop using flip-chip design

The circuit diagram in Figure 2, shows that each switch in this switching cell consists of two MOSFETs in parallel (HS1, HS2 for the High Side transistor and LS1, LS2 for the Low Side transistor). This configuration is necessary to demonstrate the importance of magnetic flux compensation in reducing parasitic inductance. We therefore find two loops associated in parallel. A 3D view of the power module is shown in Figure 3.

Figure 4 shows the flux compensation principle used in this module.

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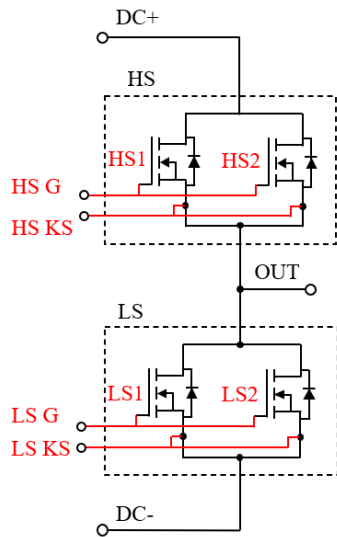


Fig. 2. Electrical scheme of the power module

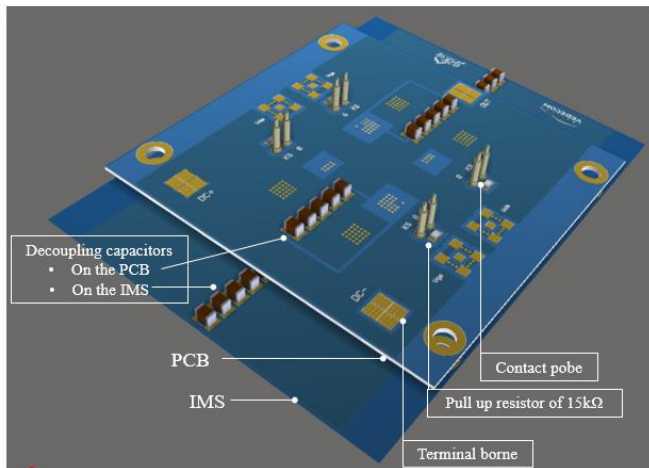


Fig. 3. 3D view of the power module

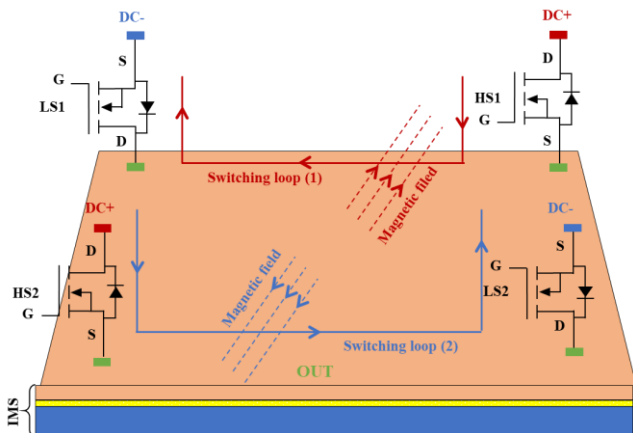


Fig. 4. Flux compensation principle used in this module

III. DESIGN REGARDING EMC, TAKING ADVANTAGES OF PARASITIC

This power module is designed by placing the power switches between a PCB and an IMS (Isolated Metal Substrate). Figure 5 and 6 show the MOSFET used in this power module, we choose this package due to the possibility to connect the drain directly from the top of the package, like a bare die component. Figure 7 and 8 show cross-sections of two version of this power module, with and without flip-chip technology, respectively. As shown in Figure 7 and 8, we observe that components are used instead of copper pads to ensure electrical continuity between the PCB and the IMS. In this case, the gate and source of each MOSFET are short-circuited thanks to their footprints on the IMS. For reasons of economy, and since cooling is only possible via the underside of the SMI, the connections between the various PCB layers are made via vias rather than microvias. The whole assembly is fixed to a heat sink using thermal paste on the IMS side.

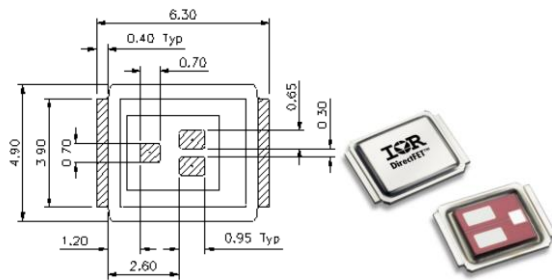


Fig. 5. The DirectFET package used in the power module

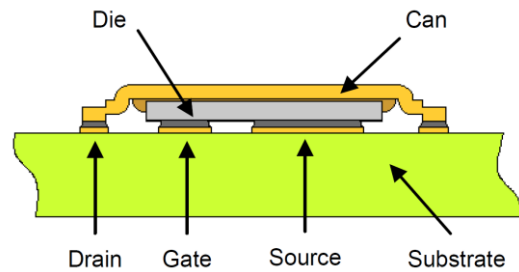


Fig. 6. Section of the MOSFET IRF6775MTRPbF

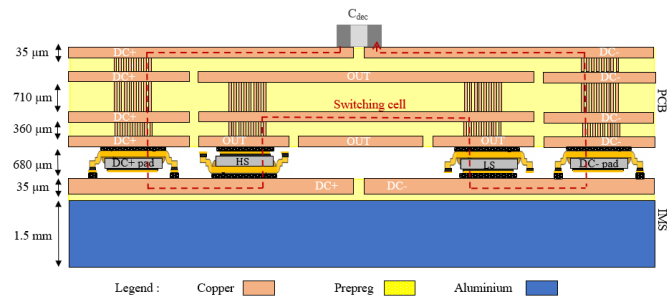


Fig. 7. Side view of power module with the flip-chip design

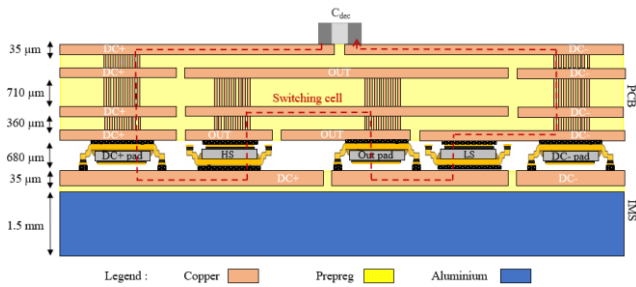


Fig. 8. Side view of power module with the conventional design

The parasitic inductances of the various branches of the power module's switching loop, as well as the mutual inductances between them, are extracted by Ansys Q3D software. This calculation is performed for both flip-chip and conventional designs

Figures 9 and 10 show that in the conventional design, the mutual inductance between the two power loops is positive, whereas it is negative in the flip-chip design due to flux compensation.

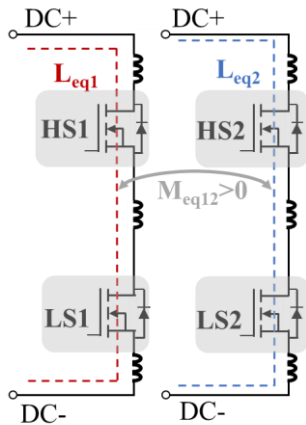


Fig. 9. Selfs and mutual inductances for the conventional design

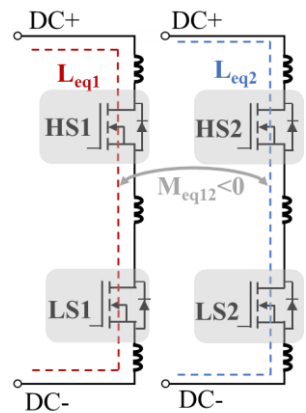


Fig. 10. Selfs and mutual inductances for the flip-chip design

In Tab 1, the inductance matrices obtained, composed of the self-inductances of the two loops of the switching loop and the mutual inductance between them, are presented for each design.

	Flip-Chip Design	Conventional Design
$\begin{bmatrix} L_{eq1} & M_{eq12} \\ M_{eq12} & L_{eq2} \end{bmatrix} (\text{nH})$	$\begin{bmatrix} 1.9 & -0.18 \\ -0.18 & 1.9 \end{bmatrix}$	$\begin{bmatrix} 2.3 & 0.1 \\ 0.1 & 2.3 \end{bmatrix}$
Stray inductance of the power loop	0.8nH	1.3nH

Tab. 1. Q3D results for parasitic inductances of flip-chip and conventional designs

Figure 11 shows the capacitive modelling of the power module including the stray capacitances to the ground. Due to high switching speed, the C_{OUT_GND} is submitted to high dV/dt and generate common mode current. The C_{DC+_GND} and C_{DC-_GND} are connected to the DC bus and can "recycle" internally the common mode current generated by C_{OUT_GND} , as described in [9]. C_{DC+_GND} and C_{DC-_GND} should thus be increased, whereas C_{OUT_GND} should be kept as small as possible.

However, care must be taken to the symmetry of C_{DC+_GND} and C_{DC-_GND} , as clearly explained in [10]. This is a crucial point to avoid Differential Mode \rightarrow Common Mode conversion. Symmetry is a key point; more details are provided in [9].

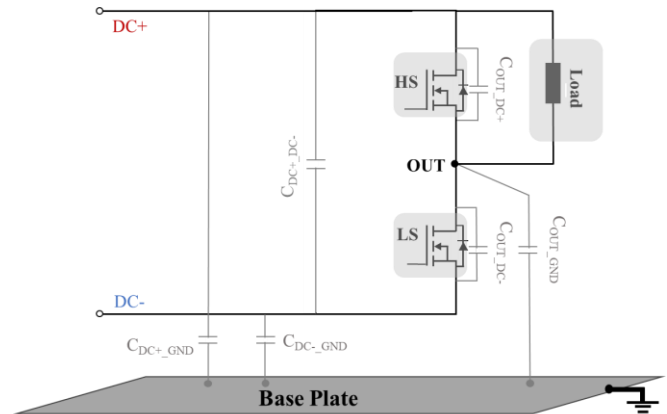


Fig. 11. Parasitic capacitances added by the package

Tab. 2. clearly illustrate that flip-chip design allows a large reduction of the common mode capacitance (3pf vs 270 pf in the conventional design) and a better symmetry of C_{DC+_GND} and C_{DC-_GND} .

[pF]	Flip-Chip Design	Conventional Design
C_{OUT_GND}	3	270
C_{DC+_GND}	1600	1700
C_{DC-_GND}	1500	1400
C_{OUT_DC+}	90	93
C_{OUT_DC-}	86	84

Tab. 2. Q3D results for parasitic capacitances

Figure 12 shows a view of the power module used for EMC test bench. Figure 13 illustrates the setup of the EMC test bench. As the EMC measurements are carried out in steady state, a water heat sink is used to cool the power module. The load consists of a $40\mu\text{H}$ inductor to minimize current ripple, and a 1Ω LPS1100 resistor. The ATS-CP-1004 water heatsink is chosen to remove the heat from the resistive load. The whole unit is mounted on a copper ground plane. Figure 14 shows a large reduction of common mode current in all the spectrum thanks to the use of the flip-chip design. This reduction in disturbance is justified by two main features of the flip-chip design. The first is the huge reduction in parasitic capacitance C_{OUT_GND} between the phase and ground plane, from 270pF for the conventional design to a value of just a few pF for the flip-chip design. The second is the almost balanced values of C_{D+_GND} and C_{D-_GND} . This high values of these two stray capacitances act as part of EMC filter for common-mode currents, and the symmetry of the design prevents coupling between differential and common modes.

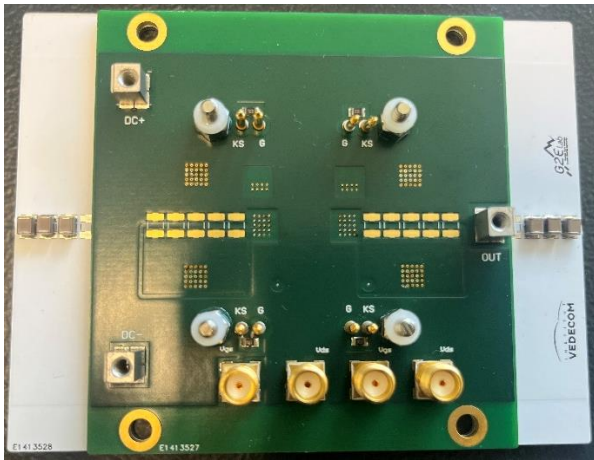


Fig. 12. The power module

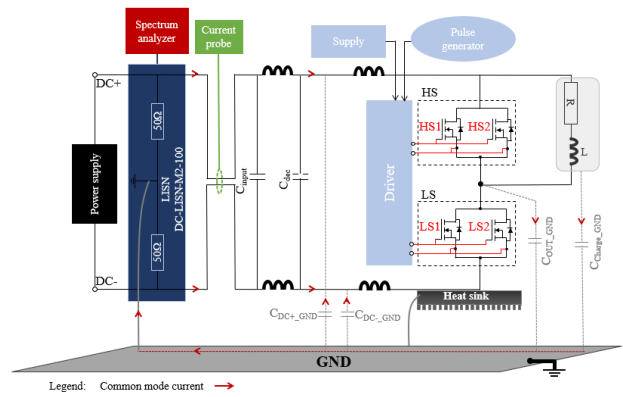


Fig. 13. EMC test bench circuit diagram

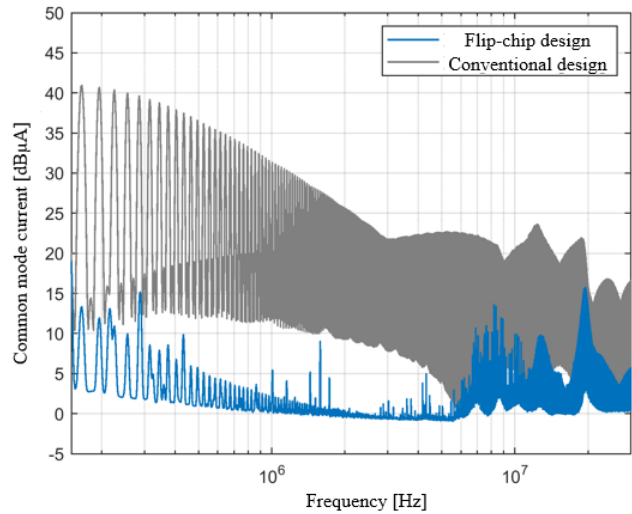


Fig. 14. Common mode current spectrum of flip-chip design and conventional design. Measurements condition: $f_{dec} = 20\text{kHz}$, $V_{GS} = 12\text{V}$, $V_{DC} = 30\text{V}$, $I = 7.5\text{A}$

In the frequency range of the EMC standard for conducted interferences ($150\text{kHz} - 30\text{MHz}$), the flip-chip module offers a gain of between $5\text{dB}\mu\text{A}$ at 20MHz and $32\text{dB}\mu\text{A}$ at 600kHz .

Figure 15 shows experimental waveforms of V_{DS} voltage of LS1 low side MOSFET during turn off operation. The overvoltage is reduced from 27V with the conventional design to 19V with the flip-chip design. This is due to the overall reduction of the loop inductance from 1.3nH to 0.8nH .

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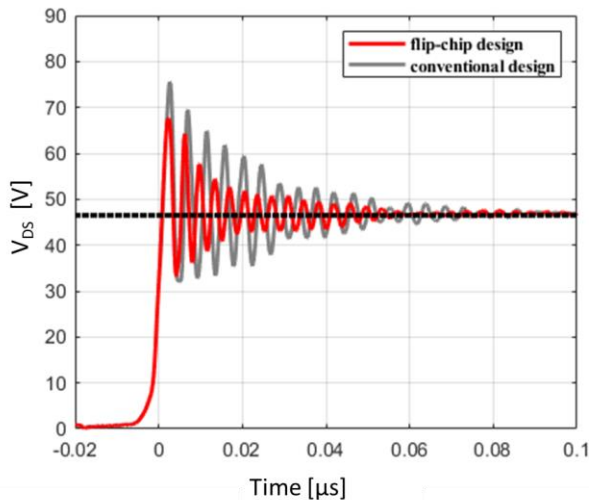


Fig. 15. V_{DS} Voltage during turn off operation for the flip-chip desing (in red) and conventional design (in grey) Mesurement conditions : $V=48V$, $I_a=40A$

IV. CONCLUSIONS

This paper has shown that the use of flip-chip design results in a very low stray inductance power module despite the use of only classical SMD technology. Compare to the classical design with the PCB circuit to connect front side of chips (figure 8), the gain using the flip-chip design with flux compensation is 0.5nH, or almost 40% in our case. Note that we have also simulated a design with PCB embedded chip technology which allows another small reduction in the parasitic inductance loop, reaching a value of 0.7nH.

The flip-chip design also shields the output trace (OUT trace in Figure 7) of the power module between the DC+ and DC- plates. This shielding effect is responsible for the reduction in the current's common-mode spectrum. A further advantage is the improved balance between CD+_GND and CD-_GND, which also reduces the common-mode current by avoiding the conversion of differential mode to common-mode current.

In our power module, the flip-chip design enables a 30% reduction in overvoltage and a gain of 5dB μ A to 32dB μ A in common-mode current with the same level of technology.