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# Programming operations analysis and statistics in 1S1R OTS+PCM Double-Patterned Self-Aligned structure

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This study explores the reliability of a Phase-Change Memory (PCM) co-integrated with an Ovonic Threshold Switching (OTS) selector (1S1R structure) based on an innovative Double-Patterned Self-Aligned (DPISA) architecture. The PCM device is based on a "Wall" structure and on Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> alloy, while the OTS is based of a GeSbSeN alloy. Our analysis focuses on the programming characteristics and SET pulse optimization, with a focus on current control and pulse fall times. The results are based on statistical data obtained from a kb-sized memory array. We examine the variability of the threshold voltage ( $V_{th}$ ) for both the SET and RESET states, comparing different distribution model to validate the use of Mean and Standard Deviation as viable metrics. We also track the dispersion of  $V_{th}$  as the fall time increases during SET operation and provide insight into the evolution of device behavior over endurance cycles and reading cycles. This research sheds light on the DPISA architecture, and on PCM+OTS in general, offering insights into their programming, variability, and reliability targeting Crossbar applications.

## 1 Introduction

Phase Change Memory (PCM) and Ovonic Threshold Switching (OTS) selector in 1S1R configuration demonstrated to be a promising Back-End-of-Line (BEOL) memory technology. PCM is one of the most mature emerging non-volatile memory, renowned for its reliability, scalability, and small aerial footprint[1]. Its performance metrics make it suitable for Storage-Class Memory (SCM) applications[2], [3], DRAM replacement[4], and embedded memory[1]. PCM features as well an analog programming behavior that makes it interesting for exploitation in neuromorphic and in Matrix Vector Multiplications (MVM) computing[5]. The success of Phase-Change Memory is also attributed to its adoption in Crossbar architecture, combining high cell density in a stackable and technological portable solution. PCM-based Crossbar arrays first appeared into the market with the 3D Xpoint™ technology by Intel/Micron [6], [7], which objective was introduce a gap-filler solution into the servers' memory hierarchy. This SCM solution provides intermediate performances between the dynamic main memory (DRAM) and the mass storage (Flash Memory)[8], [9]. The introduction of PCM in Crossbar arrays was possible thanks to the co-integration with OTS selector. OTS offers many advantages, such as low leakage current, an extremely high ON current density ( $>10 \text{ MA cm}^{-2}$ ), fast switching speed with an ON/OFF current ratio of more than two orders of magnitude [10], [11]. PCM and OTS compositions share some common elements, they have similar thermal budget and compatible switching properties. It makes OTS a preferable choice over all the other two-terminals selector device alternatives [12].

The most common 1S1R device is based on a "confined" structure with a minimal footprint of  $4F^2$ , built by the stacking of the electrodes, PCM and OTS in a pillar architecture [13]. This solution offers the

advantages of a relatively simple integration and 3D stacking of multiple memory layers. While this approach is preferred for dense memory applications, it lacks the reliability and the optimization knobs offered by a standard "mushroom" cell [14], that are well suited in embedded applications [15].

In this work we address the programming characteristics of a novel 1S1R Double-Patterned Self-Aligned (DPSA) cell based on "Wall" heater structure [16]. We study 1S1R devices integrating GeSbSeN-based OTS and  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ -based PCM. We show how the SET state can be improved in order to enlarge the memory window up to more than 2 V, analyzing the statistics of the corresponding switching voltage in kb arrays. We compare three different distribution model fitting to validate the use of mean and standard deviation (SD) to describe the collective trends. Moreover, we demonstrate the scalability of the DPSA structure comparing the behavior of large and scaled devices (down to 60 nm). Finally, we track the evolution of the Threshold Voltage ( $V_{\text{th}}$ ) during writing (programming endurance) and reading operations (reading endurance). Therefore, our results provide a first insight into the reliability and intrinsic variability of the programming in 1S1R DPSA PCM+OTS devices.

## 2 DPSA PCM+OTS device structure

The DPSA structure is described in detail in **Figure 1**. It is fabricated through two lithographic steps (i.e. Double-Patterned) that allows to provide the self-alignment (i.e. Self-Aligned) along x-direction of the Wall heater electrode with the rest of the memory stack [16]. We tested devices with a Wall electrode width (i.e. critical dimension) of 60 nm and 100 nm and in the following we address them by their dimension. The OTS device sides are equivalent to the Wall heater width (i.e.  $60 \times 60$  nm and  $100 \times 100$  nm). The phase-change layer is based on standard  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  while the OTS selector on GeSbSeN alloy stacked between two carbon-based layers to avoid intermixing [10]. Both the Top Electrode (TE) and the Intermediate Metal (IM) are based on titanium nitride (TiN).

## 3 DPSA PCM+OTS Electrical Characterization

We performed the electrical characterization of the devices using pulse based (AC) protocols. The  $V_{\text{th}}$  was systematically measured by a staircase-up sequence starting from low voltage up to the detection of the switching of the device (i.e. detection of the current increase). During the reading (and programming) operations, the current is limited by an nMOS transistor (1T) controlling its gate voltage. In the following we will analyze the programming characteristics of DPSA 1S1R devices, the SET programming performance and the statistics of the correspondent threshold voltage  $V_{\text{th}}$ , the reading and programming endurance and the statistical analysis of the programmed SET and RESET states.

### 3.1 Programming Characteristics

The devices were all initialized by a dedicated firing procedure well known in OTS devices [17], controlling the max firing current by the 1T device to avoid some unwanted device damage and to emulate the real behavior once integrated in a Crossbar array. We used a firing current proportional to the size of the PCM and OTS devices tested. We applied a sequence of programming pulses of increasing voltage acquiring the programming current during each pulse. Before each programming pulse, the device was prepared in a SET state (the PCM is programmed to a low resistance state). Therefore, the reading protocol allowed to collect the  $V_{\text{th}}$  of the device as a function of the current during the programming pulse as reported in **Figure 2** ( $V_{\text{vsI}}$ ). Both 60 nm and 100 nm devices exhibit a compatible threshold voltage range, between 3.5 V ( $V_{\text{th,SET}}$ ) and 5 V ( $V_{\text{th,RESET}}$ ), however the 60 nm cells are programmed in the RESET state with a current reduction of about 50% as expected from the reduced Wall heater size. The slightly higher  $V_{\text{th}}$  of the 60 nm population, is likely attributable to the reduced volume of the OTS region implied into the initialization [17], the threshold memory window is however not impacted. Moreover, we think that using a reduced initialization current can reduce the elemental migration phenomena in the material preserving the OTS device from a premature degradation of its leakage current and  $V_{\text{th}}$  [18].

### 3.2 SET programming

The SET current was chosen to minimize the  $V_{th,SET}$  from preliminary  $V_{vsI}$  characteristics (Figure 2). In order to enhance the crystallization into the PCM device, we explored the impact of the pulse fall-time ( $t_{fall}$ ) on the  $V_{th}$  [19] (**Figure 3**). We can observe a reduction of  $V_{th,SET}$  increasing the  $t_{fall}$  value in both device dimensions, compatibly with a better SET programming. Moreover, the programming window ( $V_{th,RESET} - V_{th,SET}$ ) is enhanced to more than 2 V. Remarkably, both 60 and 100 nm devices show a similar evolution, suggesting a negligible impact of the scaling on the device's SET performance. **Figure 4** shows the obtained  $V_{th,SET}$  distributions by selecting a 1  $\mu$ s pulse fall time, and the good separation (at  $1\sigma$ ) of the SET and RESET distributions. The  $V_{th}$  is reported after a short seasoning procedure of about 100 cycles.

#### SET programming statistical analysis

Considering the SET state of 1S1R devices, the  $V_{th}$  is dependent almost only on the OTS switching voltage, being the PCM in its SET state (i.e. highly conductive). On the contrary, in the RESET state, both the OTS selector and the PCM memory switching voltages affects the final  $V_{th,RESET}$  distribution. A Normal distribution is commonly used for the analysis of  $V_{th}$ , reporting the associated mean and variance values. However, the stochastic switching mechanism in chalcogenide-based devices has been suggested to better follow a Weibull distribution or a Generalized Gamma function [20]. We compared the three different distribution models by fitting the SET data from Figure 3 with an iterative Maximum-Likelihood method, in particular focusing on 60 nm devices (**Figure 5**). The mean values overlap with no significant differences, while the SD vary slightly depending on the model. The best fitting is characterized by a greater Likelihood coefficient [21], reported at the bottom of Figure 5 for three different time instants corresponding to a low, medium and high  $t_{fall}$ . The Gamma distribution fits best in all cases, followed by the Normal model, as reported in Figure 5. The Weibull models produces the worst approximation of the data set about most of the times. Based on this results, we can conclude that the best fitting is obtained with the Gamma distribution, while the Normal still provides a good estimate.

All the three models present a minimum SD around 2  $\mu$ s, compatibly with a lower variability of the SET operation in this  $t_{fall}$  range. Indeed, a more reliable SET operation thanks to the  $t_{fall}$  increase can be easily achieved below 2  $\mu$ s with a reduction of  $V_{th,SET}$  from about 3.7 V to 3 V, likely suppressing all the amorphous residuals over the heater electrode. A further improvement of the PCM SET state implies a better crystalline arrangement that could present some higher variability [22].

### 3.3 Reading Endurance

In a 1S1R device the reading operation is performed at an intermediate voltage between  $V_{th,SET}$  and  $V_{th,RESET}$ . If the cell is programmed in the SET state, the reading operations implies a switching of the OTS and a current flow is detected: such switching could affect the programmed state. In order to verify the impact of the reading operation, we applied a sequence of  $10^3$  reading pulses of 3.5 V with a max reading current fixed at 100  $\mu$ A (enough to discriminate SET and RESET states through switching). In **Figure 6** we report the final  $V_{th,SET}$  and  $V_{th,RESET}$  measured after the applied stress sequence. The  $V_{th,SET}$  shows an increase likely due to some possible re-amorphization of part of the devices population, however the mean value remains below the reading voltage. On the contrary,  $V_{th,RESET}$  shows only a slight increase likely due to drift phenomenon [23], [24]. This test shows that the reading operation should be carefully optimized and in our case the chosen reading current revealed to be sufficiently low to ensure at least  $10^3$  reliable reading operations.

### 3.4 Programming Endurance

We studied the programming endurance of our 60 nm 1S1R devices using a RESET current overdrive of about 30% to induce early degradation. The  $V_{th}$  for both RESET and SET states as a function of the

programming cycle number is reported in **Figure 7**. After  $10^3$  cycles the programming window begins to narrow, in particular due to a reduction of  $V_{th,RESET}$ . This is due to a degradation of the PCM device, while the OTS continues to show a switching voltage compatible with the beginning of the test (i.e. equal to  $V_{th,SET}$ ). Indeed, the current density is higher in the PCM device due to the reduced heater surface (dependent on the electrode thickness and on the Wall heater width) with respect to the OTS surface. This confirms that in our DPSA structure, the endurance capability is mainly driven by the PCM cycling performance.

#### Programming endurance statistical analysis

In **Figure 8** we report the SD for the SET and RESET distributions along cycling for the test already presented in Figure 7. While the SD of  $V_{th,SET}$  is quite stable, it sharply increases for the RESET state when the PCM degradation starts. Comparing Normal, Weibull and Gamma models to fit the obtained distributions, all of them show this similar trend. Moreover, starting from  $10^3$  cycles we can observe a reduction of the Likelihood estimates for the three models, and the data can be considered as the result of the convolution of two different populations (i.e. distributions). Indeed, devices still preserving a RESET state for the PCM are mixed with devices presenting a stuck SET state. As for previous results the SET state can be well described by a Gamma distribution, or approximated as Normal. On the contrary, the increased dispersion of the RESET state does not produce a consistent fit with only one model.

## 4 Conclusions

We presented for the first time the programming characteristics of a novel Double-Patterned Self-Aligned (DPSA) 1S1R OTS+PCM device. We evaluated the variability of the programmed states and showed how the SET state can be improved with a reduction of the associated  $V_{th,SET}$  in devices with a "Wall" heater electrode width down to 60 nm. We did not observe an impact from the device size on the SET performance, confirming the scaling potentiality of DPSA structure. Thanks to such improvement, the programming window can be enhanced up to 2 V. We fitted the data using three different distribution models: Normal, Weibull and Gamma. Even if the switching phenomenon is compatible with a Weibull model as previously reported in literature, we show that Gamma (and with lower precision Normal) model can be safely used to describe  $V_{th}$  distributions even along cycling and aging. Moreover, we showed that the DPSA OTS+PCM device endurance mainly depends on the PCM performance. Finally, the  $V_{th}$  evolution in particular of the RESET state under a given stress condition such as a programming current overdrive (i.e. + 30%), should be described using the convolution of several distributions and not just a single one. It means that the report of the  $V_{th}$  mean and SD values, could give an incomplete information about the array failures. We think that this is important for the right estimation of the failure parameters for future reliability assessment of Crossbar arrays based on DPSA 1S1R OTS+PCM.

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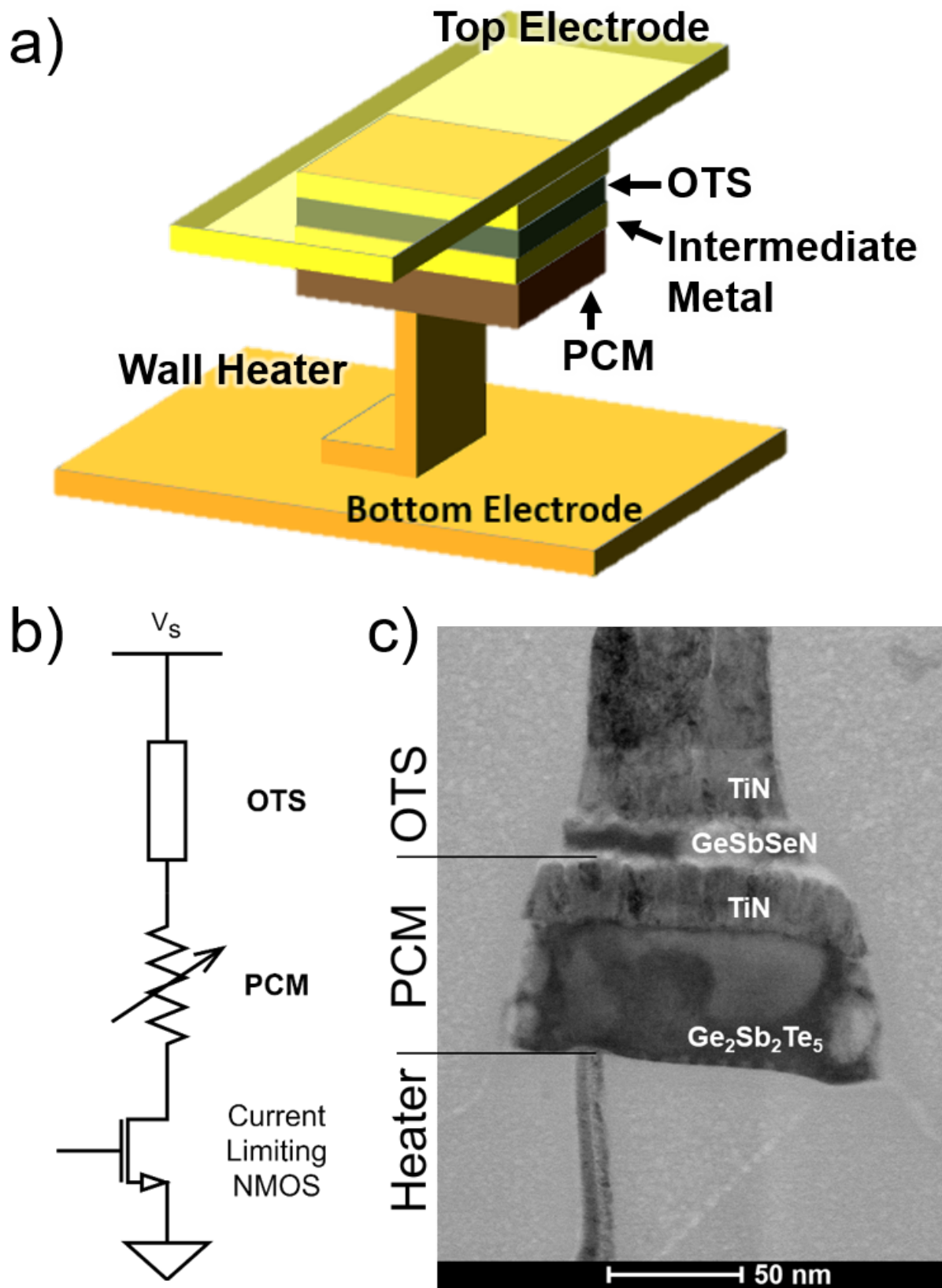


Figure 1: (a) 3D simplified scheme of the DPSA device. (b) Circuit scheme of a single 1S1R device including the nMOS limiting device. (c) Scanning Transmission Electron Microscopy (STEM) image of a 100 nm DPSA 1S1R device, highlighting some of the challenges of the lithographic steps such as the heater alignment.

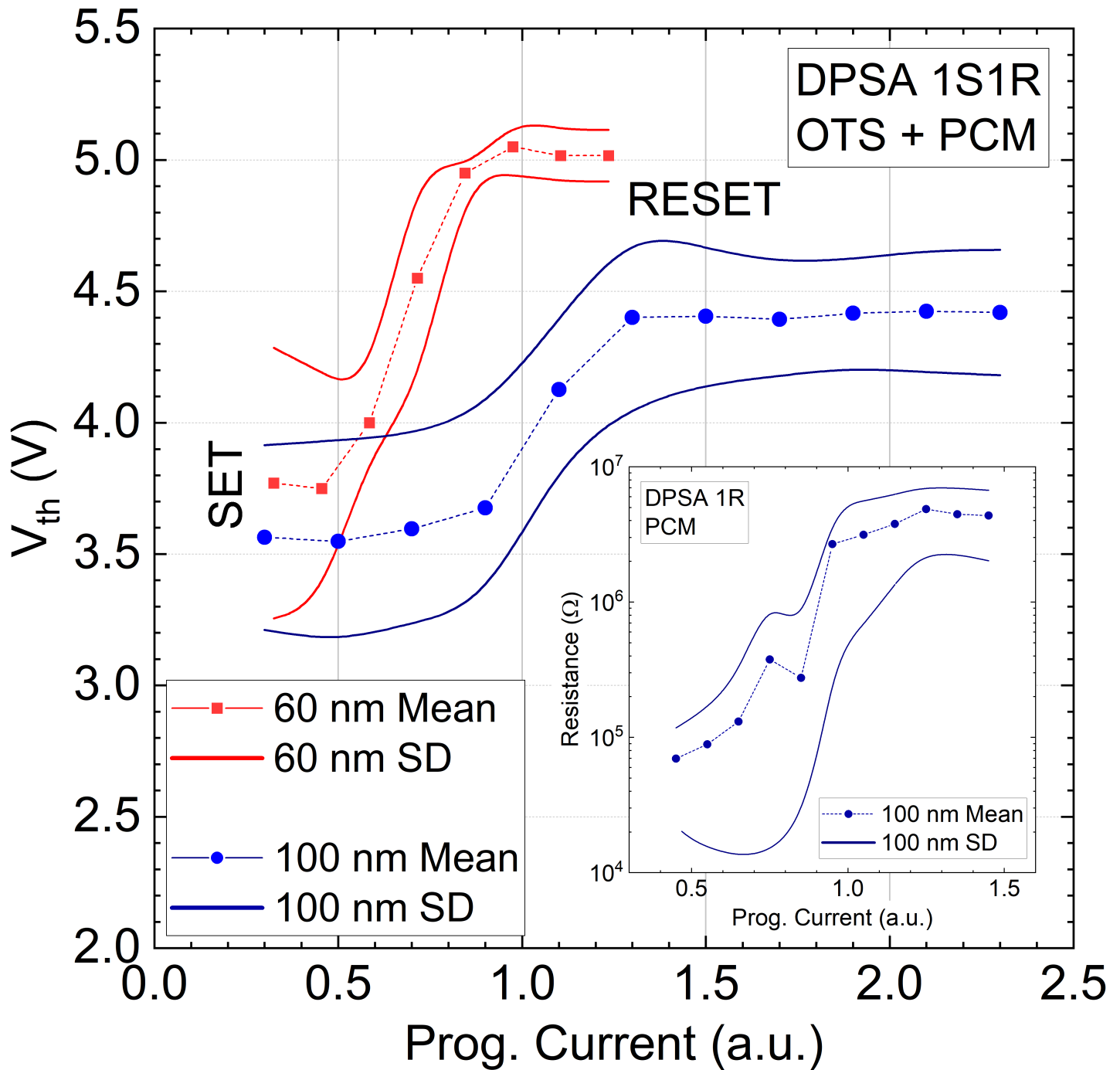


Figure 2: Evolution of the  $V_{th}$  as a function of the programming pulse current in 1S1R devices. The inset shows the resistance vs current characteristic for a 100 nm 1R device (i.e. without OTS) matching the expected SET and RESET operations verified by the direct measurement of the evolution of the resistance of the device increasing the programming current (i.e. not possible in 1S1R device).



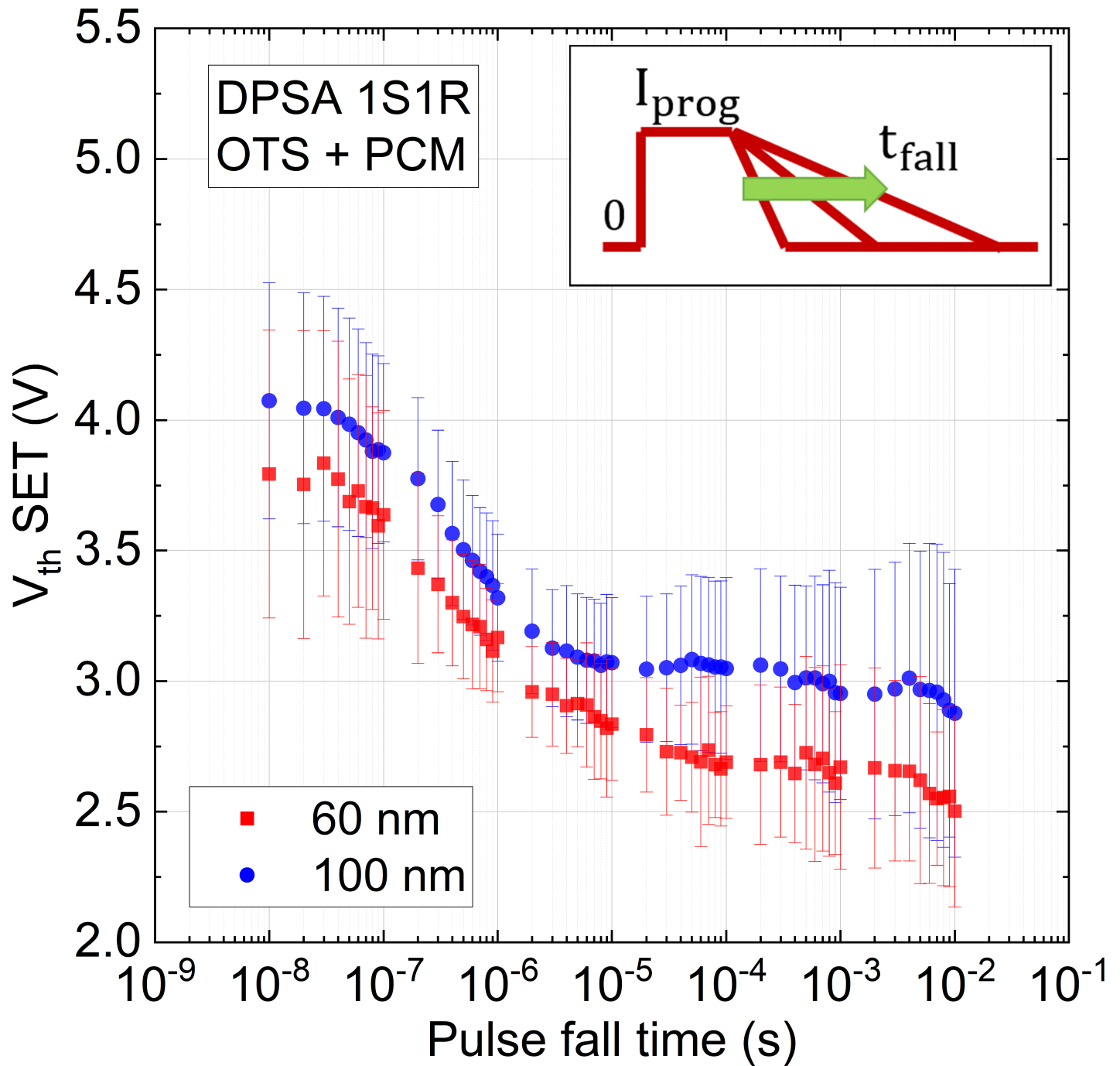


Figure 3:  $V_{th,SET}$  as a function of  $t_{fall}$ : 60 nm and 100 nm devices show a similar trend. The inset describes the pulse shape, with fixed current and variable  $t_{fall}$ .

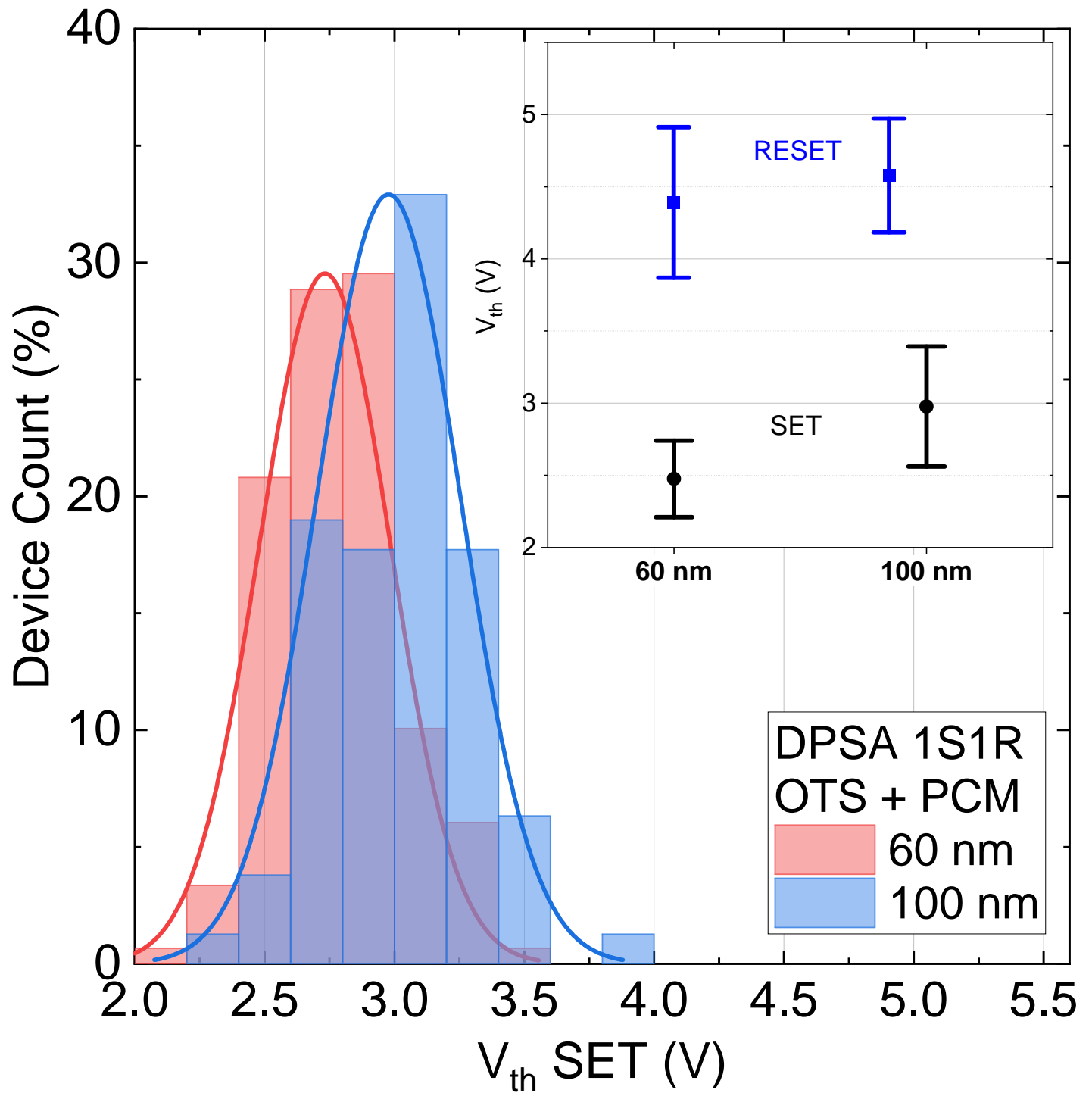


Figure 4:  $V_{th,SET}$  distributions for both 60 nm and 100 nm devices. The inset shows the achieved  $V_{th,SET}$  and  $V_{th,RESET}$  (with their 1 $\sigma$  deviation).

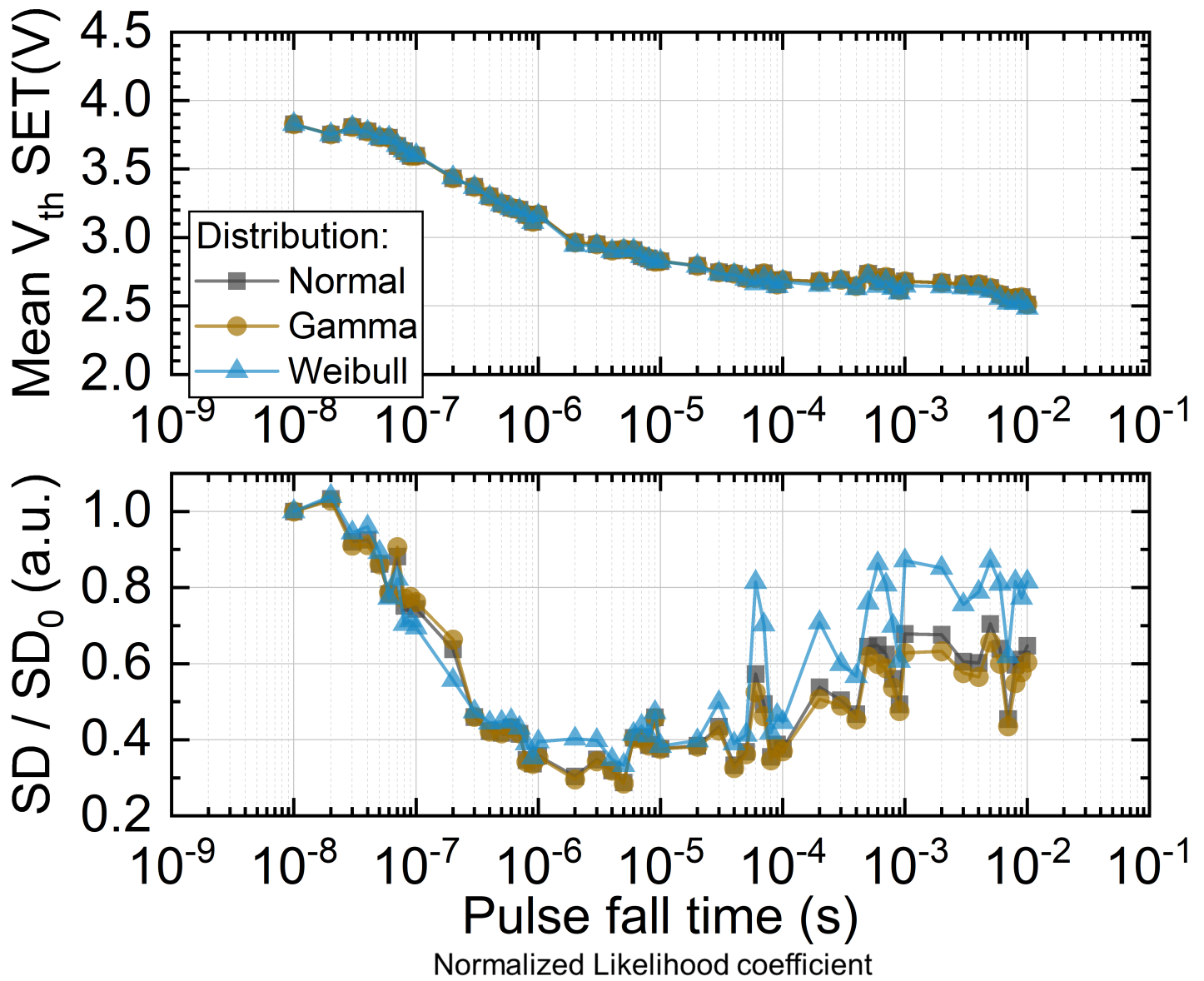


Figure 5: Mean (top) and standard deviation (bottom) values for  $V_{th,SET}$  as a function of  $t_{fall}$  extracted using Normal, Weibull and Gamma distribution models for 60 nm devices. In the table, the normalized Likelihood estimate of the fitting is reported, a higher number indicates a better fitting (over the other models). The analyses were performed using the *fitdistrplus* package of R software [21], [25].

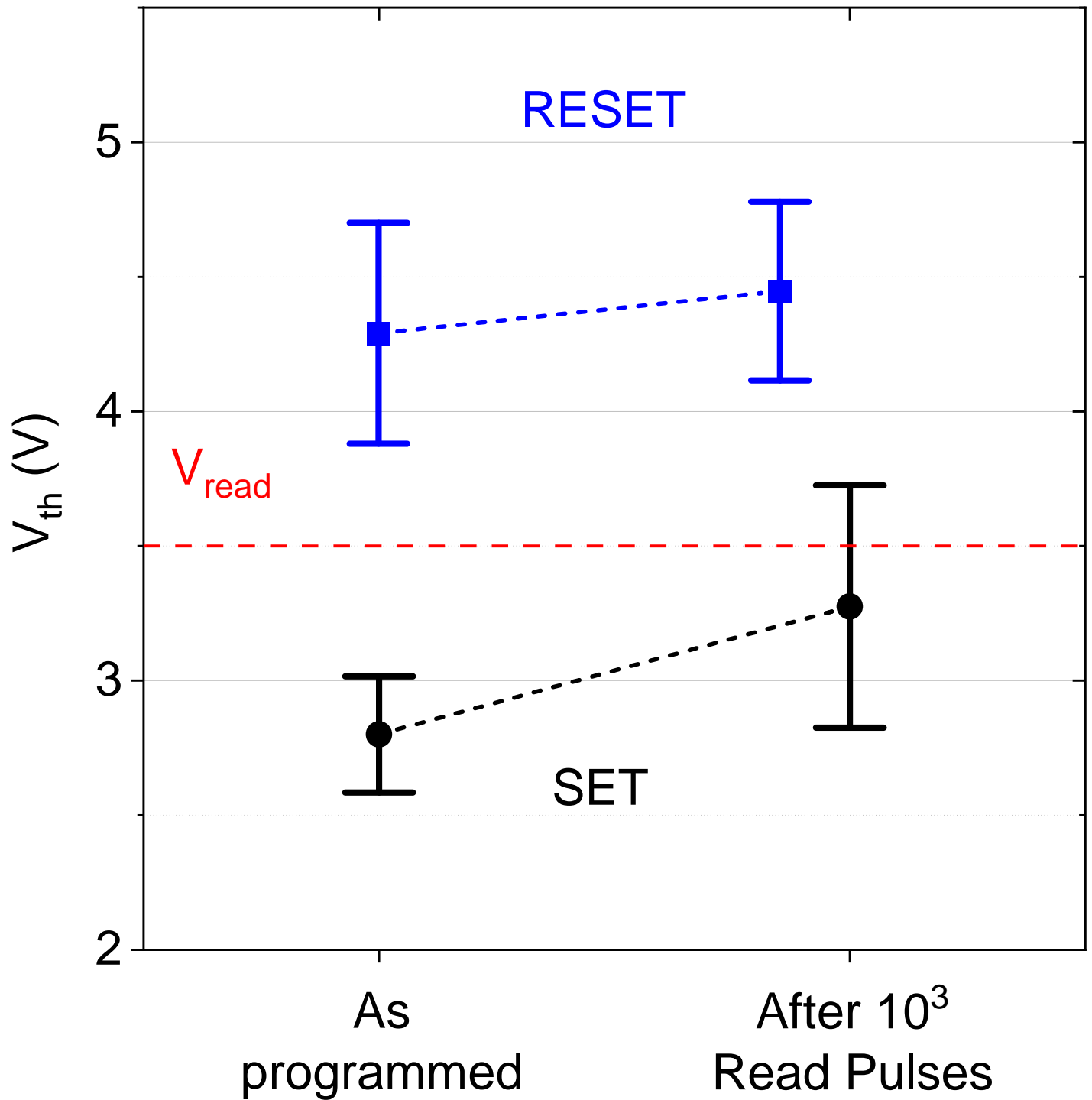


Figure 6: Impact of  $10^3$  reading operations on the evolution of  $V_{th,SET}$  and  $V_{th,RESET}$ . Data are collected from 1S1R 100 nm cells.

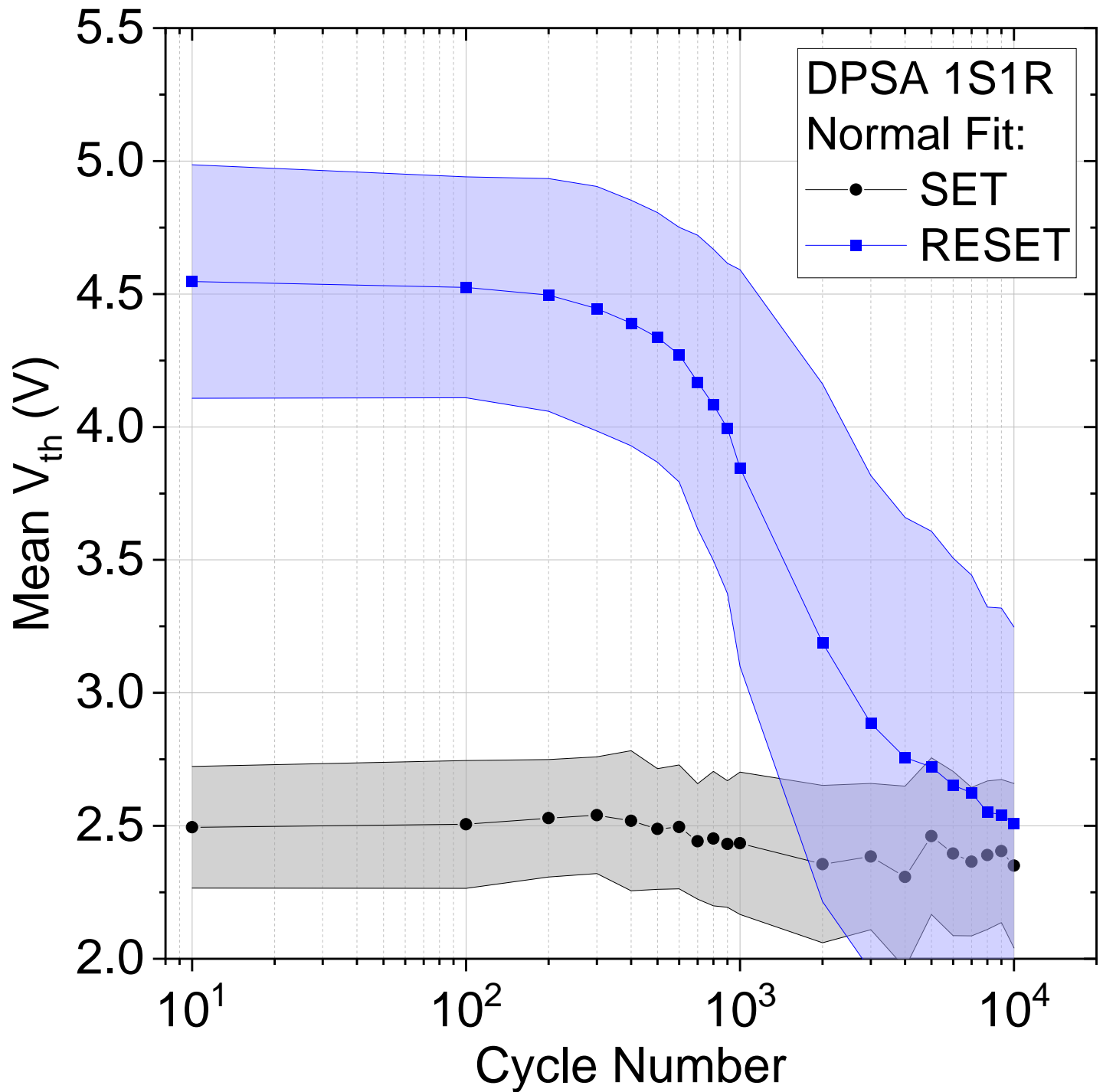


Figure 7: Programming endurance for 60 nm devices performed with a current overdrive of + 30% with respect to standard RESET programming current. Both mean and SD values are reported.

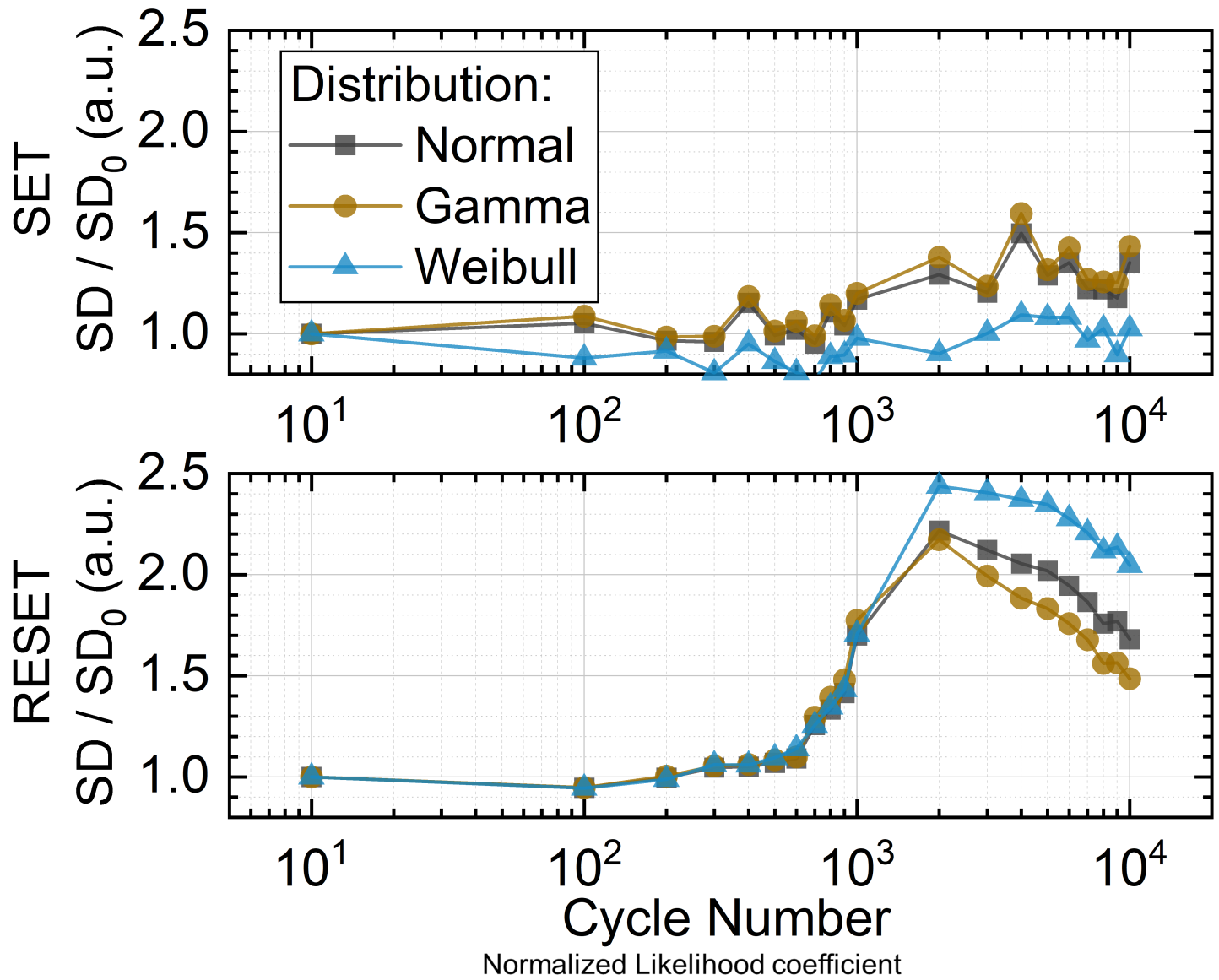


Figure 8: Normalized Standard Deviation (SD) for the SET state (top) and for the RESET state (bottom) of 60 nm devices along cycling. In the table the normalized Likelihood estimate for SET and RESET stated for two different cycling condition is reported. A higher number indicates a better fitting [21].