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Experimental three-dimensional thermal mapping of a GaN on RF-SOI chip

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Abstract—We present a novel method to determine the three-dimensional (3D) temperature field of a radio frequency (RF) chip based on a 3D heterogeneous integration of GaN HEMT and RF-SOI technologies combining the advantages of both. It is composed of a stack of multiple layers of different materials on top of a SOI substrate. A RF GaN transistor is located at the top of the stack and acts as a heat source. We use several resistance temperature detectors (RTDs) embedded at different key locations in the stack coupled to an infrared (IR) thermography. When combined to a 3D numerical model, such methodology enables us to extract the necessary information in order to retrieve the temperature 3D distribution in the whole sample.

Keywords— *GaN transistor; RTD; temperature distribution; silicon on insulator;*

I. INTRODUCTION

In the past twenty years, integrated circuits based on silicon on insulator substrates (SOI) have become ubiquitous[1]. Some practicalities of the SOI's buried insulating layer, typically silicon dioxide, are to reduce the parasitic source/drain-to-substrate junction capacitance, to limit the depth of the source/drain junction, and to allow full dielectric isolation of the device in order to eliminate latch-up. However, the buried silicon oxide layer (BOX) has a thermal conductivity about two orders of magnitude smaller than that of silicon. Hence, depending on the thickness of the BOX, the thermal conductance of the substrate may significantly be reduced causing severe undesired self-heating in the devices. This results in higher operating temperatures, thus reducing the device carrier's mobility as well as the maximum drain saturation current, which leads to the degradation of the device performance. On the other hand, the trend to improve the performance of circuits in the past decades has led to the miniaturization of device dimensions, including those of high-power RF devices, thereby increasing device packing densities[2], [3]. During operation, the RF transistors generate a large signal and a high output power. They act as heat sources that increase the surrounding temperature. Consequently, the influence of high temperatures on the electrical characteristics of the transistors must be carefully considered and controlled. As such, the knowledge of the

temperature of the transistors, as well as the surrounding temperature field is a useful tool to ensure the optimal performance of the RF integrated circuit. The most common reported experimental techniques for a thermal analysis of an IC rely on measuring its surface temperature using either an infrared or CCD camera[4], [5], Raman spectroscopy[6], thermocouples or thermometers deposited on top[7], [8], thermal scanning probe[9], liquid crystal technique[10], the temperature dependence of leakage currents[11] and noise Thermometry[12]. Nevertheless, the temperature of the transistor channel may not be the same as that of the surface of the IC. The difference is more pronounced when the materials used in the IC are poor thermal conductors, and when the IC process has a large number of layers. Based on our prior expertise in using RTDs for different heat and mass flow measurements[13], [14], [14], [15], we recently proposed a new way to obtain the three-dimensional (3D) temperature field in an SOI stack[16] using several RTDs in key location of the sample combined to a numerical heat transfer model calibrated using the RTDs measurements. We have shown in particular that it is possible using such method to obtain a reasonably accurate solution of the heat transfer problem in such samples. In the present work, we apply the previously developed method to a radio frequency (RF) chip resulting from on a 3D heterogeneous integration of GaN HEMT and RF-SOI technologies[17] combining the advantages of both. The main heat source is now the GaN transistor(s) located at the chip surface which significantly increase the energy and changes the temperature field. We have therefore enhanced the previously developed method using infrared surface thermography to obtain the temperature distribution in the whole chip.

II. MATERIALS AND METHODS

Samples of RF SOI power GaN transistors were fabricated on top of an RF-SOI wafer and below a stack of dielectric thin films crossed by metallic traces (as “m” and “q” in Fig. 1.a) and vias for interconnections. The GaN and RF-SOI are fabricated separately and then the GaN transistor is singulated to form a GaN coupon that is mounted on top of the SOI wafer. The GaN coupon is electrically interconnected to the RF-SOI using a thick Cu Re-Distribution Layer (RDL) as shown in

Fig. 1.b. Furthermore, we considered three different kinds of GaN transistors, differing in the number of fingers, making a total of 18 samples of 6 different kinds. Apart from the GaN transistors, the samples were fabricated at X-FAB France, based on a 130 nm RF-SOI industrial process. Nine to ten RTDs are distributed in the stack at different heights and lateral positions and are used to probe the local temperature in the chip as shown in Fig. 2.

The RTDs are accessed through contacting pads on the surface of the chip as shown in Fig.3. A probe card is used to simultaneously probe all the pads used either for sensing or to power supply the transistors. The probe card is connected to several Keithley source meters to perform a 4-points probe resistance measurement and to power the transistors. During the measurement, the chip is positioned on top of a 6-inch hot chuck coupled to a Julabo CORIO™ CD refrigerated/heating circulator for temperature control purposes. The hot chuck temperature is controlled either via the circulator fluid temperature or by the internal joule effect heater of the hot chuck.

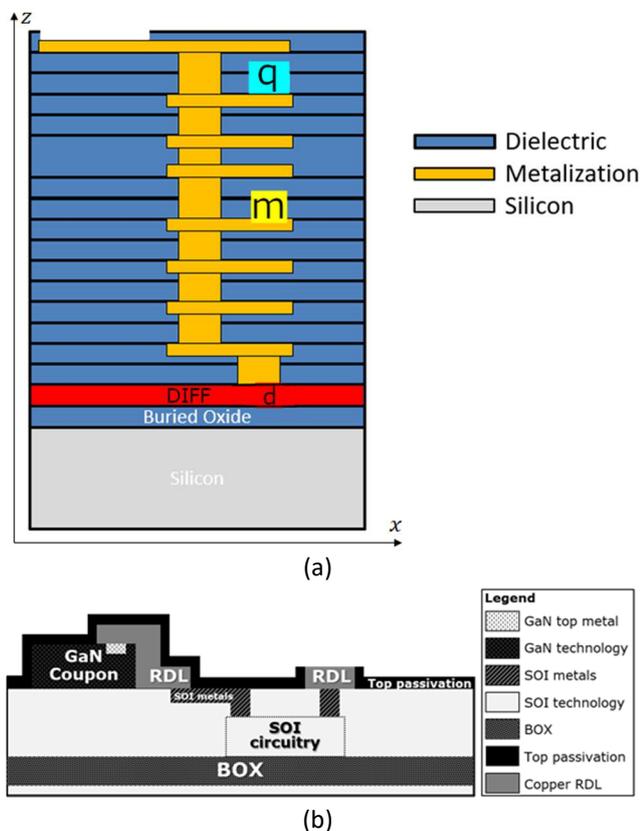


Figure 1 : a) Schematic of a typical stack on an SOI wafer similar to the one considered in the present work, with a transistor (not shown) at DIFF level (red), several metallic levels (yellow) and multiple layers of dielectrics (blue). Several metallic vias are show (yellow). The GaN transistor(s) are added on top of the structure (not shown). b) Cross-section of MTP with RF-SOI carrier and GaN coupon.

The chuck temperature is measured with a type-K thermocouple taped on the surface of the chuck, at the sample vicinity. The chuck temperature is also read by a thermocouple inside the chuck connected to an Omron temperature controller. The wafer containing the chips under test is positioned and clamped on the chuck using vacuum suction. First, we calibrate the RTDs from room temperature up to their maximal operating temperature, 250 °C in our

case. We measure their resistance as a function of temperature with a temperature step of 10 °C and obtain the resistance temperature coefficient. Then, we set the hot chuck temperature at 25 °C to ensure a constant temperature boundary condition and bias the transistors with different voltages ranging from 0 V to 1.2 V for the Si transistor, and 0 V to 2 V for the GaN transistors, which correspond to heat sources with a dissipated power of 0.35 W and 1.2 W respectively. We use a Keithley 2612B source meter to power supply the transistors and monitor their dissipated power.

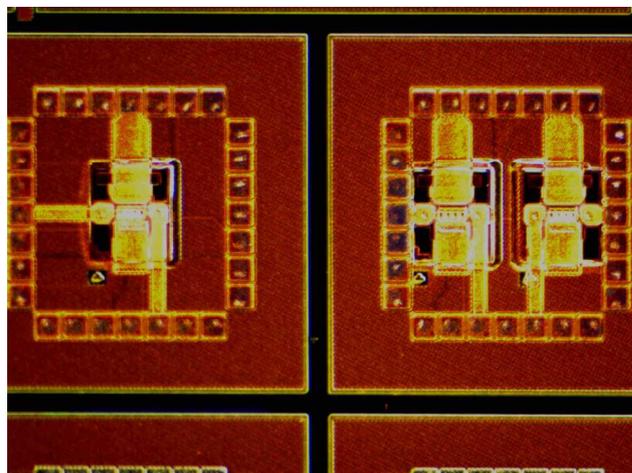


Figure 2 : Top view of a single GaN (left) and multiple GaNs (right) transistors sample. 28 contact pads are visible for each sample, in a square shape whose side is 0.7 mm long.

The measurement of the RTDs resistance value enables the determination of the temperature value at different locations around the transistors using the calibration data. We also use a FLIR A325sc infrared (IR) camera with a microscope lens providing a spatial resolution of 25 μm x 25 μm to establish a thermography of the surface of the samples under operation, thereby providing the surface temperature field as a function of the heating power. All instruments connected to a computer and controlled using a LabVIEW virtual instrument for automation purposes. The temperature values provided by the different RTDs as well as the IR camera will then be used to calibrate a finite element numerical model as previously done for an SOI stack without GaN transistors[16]. We have also previously measured the thermal conductivity of most of the materials used in the stack[16] with the 3ω method in the temperature range from 20°C to - 250°C. The obtained thermal properties are also used as inputs in the numerical model to ensure a maximal accuracy.

III. RESULTS AND DISCUSSION

First, the I-V curves of the GaN transistors are obtained for control purposes with comparison with the manufacturer datasheet and to check the power range. We have considered three different GaN transistors A, B and C with different dimensions leading to different dissipated powers. We show in Figure 3 the I-V curves obtained for single GaN transistors samples A, B and C. One should note for example that GaN transistor C is twice longer than transistor B which explains that the obtained current for C is twice larger than that of B for the same applied bias voltage leading to a dissipated power twice larger. The obtained I-V curves enable us to choose the appropriate I-V values to obtain a desired dissipated power.

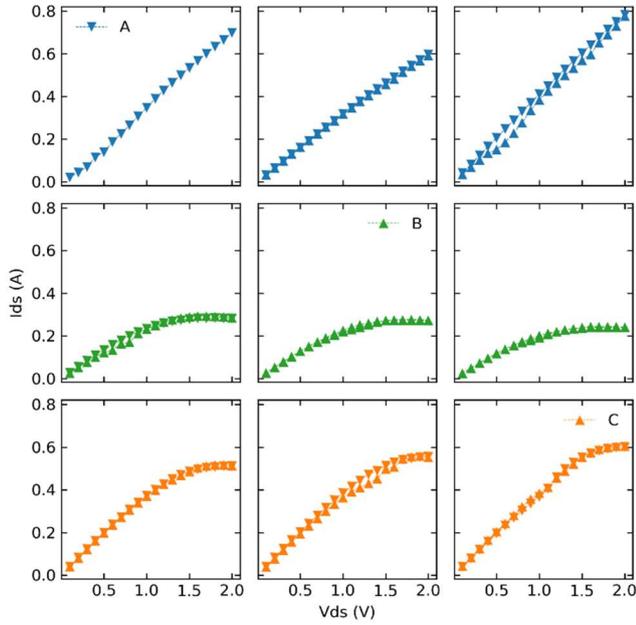


Figure 3 : I-V curves of three different types of single GaN transistor samples. Upward triangles indicate that the bias voltage was being increased, from 0 V to 2 V, whereas the downward triangles are data for a decreasing voltage. The letters A, B and C refer to the type of GaN transistors considered here.

Then the RTDs are calibrated, i.e. their resistance is measured as a function of temperature in the temperature range of interest. The RTDs exhibit a linear behavior of $R(T)$ (results not shown here. See our previous work [16] for similar results.) over the whole temperature range, as expected since the resistors are made of aluminum, copper, and doped silicon. The choice of different materials for the RTDs at different levels is due to X-FAB XR013 technology process which uses different metals at different levels of the stack. We note here that the RTDs at level “ d ” are made of semiconductors and provide a better accuracy than the metallic ones (in levels “ m ” and “ q ”) due to a smaller relative error in measuring R . This is a direct consequence of a larger resistance value at room temperature which is due to the larger resistivity of the used material. Nevertheless, the relative variation of metallic RTDs is large enough to enable a proper measurement of the temperature variation in the range of interest, considering the sensitivity of the used experimental setup, nV for voltage measurement and nA for current measurement in our case.

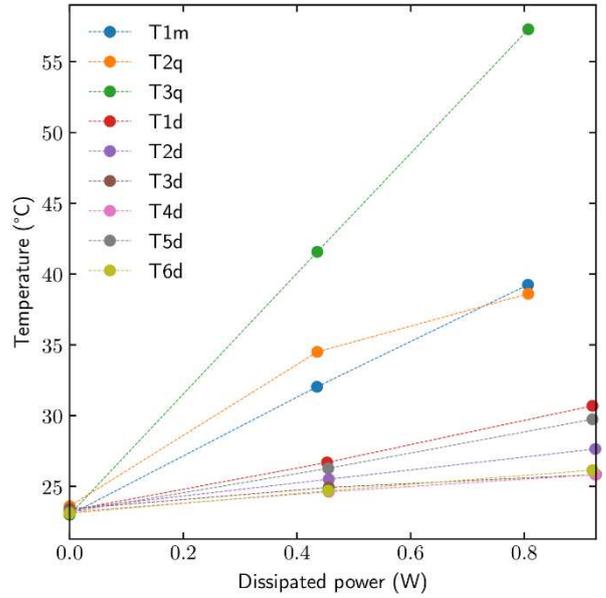


Figure 4 : Temperature of 9 RTDs at 3 different levels of the SOI stack of a single GaN transistor sample as a function of the dissipated electric power. The subscripts d , m and q refer to 3 different heights where d is located just above the BOX level m just below the GaN coupon and q at an intermediate level.

As mentioned in the previous section, the RTDs are then used to measure the temperature of the chip at different locations (those of the RTDs) under operating conditions, i.e. when one or several transistors are power supplied. For this purpose, several different experiments have been performed, on different samples containing one or multiple GaN transistors.

For single GaN transistor samples, we have measured the temperature of the thermometers for 3 different biases from 0 to 0.9 W. The results are shown in Figure 4 for one of the tested samples. We observe a linear behavior of the temperature as a function of the heating power for all the RTDs. Moreover, we observe a larger temperature at the highest levels (m and q), whereas the thermometers at level “ d ”, closer to the substrate, exhibit the lowest temperatures. In fact, the largest temperature, 55°C in this case, is reached by T_{3q} , one of the RTDs of level q , just below the GaN coupon. One should note here that this is not the maximum temperature in the chip since the RTDs enable to access directly the temperature value only at 9 different location. This distribution is expected since the GaN coupon is the heat source and the SOI substrate which is in contact with a controlled temperature chuck at a constant temperature, 25°C in our case, is the heat sink. Larger temperatures are then expected at the GaN transistor level. In addition, we observe that some RTDs are more sensitive to GaN transistors than others (for example T_{3q} compared to T_{1m}).

We show in Figure 5 the results of a similar experiment obtained with a multiple GaN transistor sample containing two GaN transistors at different biases, i.e. at different dissipated powers from 0 to 1.85 W. The two GaN transistors are biased simultaneously to investigate the effect of multiple heat sources on the temperature distribution. The dissipated power in this case is twice larger than that of a single GaN transistor sample since we double the number of heat sources.

The largest temperature recorded by the RTDs slightly increases compared to the single GaN case and exceeds 60°C . We also observe a significant change in the temperature distribution compared to the single GaN case. RTDs of level d which are located at diff level, i.e. the closest to the substrate and the farthest from the heat source, still exhibit the lowest temperatures, very close to room temperature since they are located just on top of the substrate where a constant temperature boundary condition is imposed, 25°C in our case and around room temperature) in addition to a large thermal conductivity of the silicon substrate. However, m level RTD now records the largest temperatures for all dissipated powers even if it is not the closest to the heat sources since it is at an intermediate level between level d and level q (see Figure 1-a). This apparently surprising result may be explained by a heat bridge between the heat sources, GaN transistors, and the RTD 1 of level m due to the copper metallic vias that are illustrated in yellow in Figure 1-a. If such bridge is avoided in the single GaN transistor samples, it is not the case in the multiple GaN transistor sample due to the largest footprint of the heat sources at the stack top. Finally, we complement the in-situ contact measurements obtained using the RTDs by remote measurements using IR thermography to obtain the sample surface temperature field. We show in Figure 6 a 2D surface temperature map obtained for a sample with 2 GaN transistors where the same bias of 2 V was applied to the two transistors. The two GaN transistors are biased simultaneously. As expected, the maximum temperature is observed at the center of the transistors and exceeds 147°C . Such result is expected since the maximum temperature is expected at the center of the heat sources.

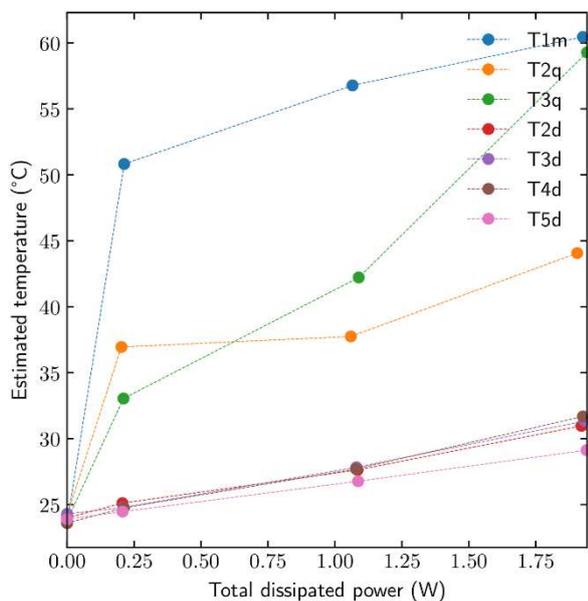


Figure 5 : Temperature of 7 RTDs, at 3 different levels of the stack on multiple GaN transistors sample, for 4 different transistor bias when the two GaN transistors are biased simultaneously.

One should note here the large temperature difference between the maximum temperatures provided by the RTDs embedded in the stack and those recorded at the sample surface. This suggests that most of the generated heat is evacuated by convective transfer at the GaN transistors surface rather than by conduction in the stack and the substrate. Consequently, an efficient cooling strategy would focus on remove the heat directly at the chip top, i.e. directly

from the heat source, either by forced convection or by contact, rather than from the stack bottom due to the large thermal resistance of the stack below the GaN transistors. The IR thermography image also reveal hot spots at the contact pads located at the chip surface (not shown in Figure 6 because of the strong zoom on the heat sources) and used to probe the different RTDs and to power supply the transistors suggesting electric power dissipation at these locations. This should be considered for an accurate quantification of the electric power actually dissipated by the GaN transistors which is probably lower than that provided by source-meter. The obtained experimental results are currently being embedded in the 3D multi-physics numerical model similar to the one we previously developed for the SOI stack with SOI transistors[16] in order to obtain the full 3D temperature field of the chip. The temperature values provided by the RTDs and the surface temperature obtained by IR thermography will be used to calibrate the model and ensure a good agreement between the simulation and the experiment.

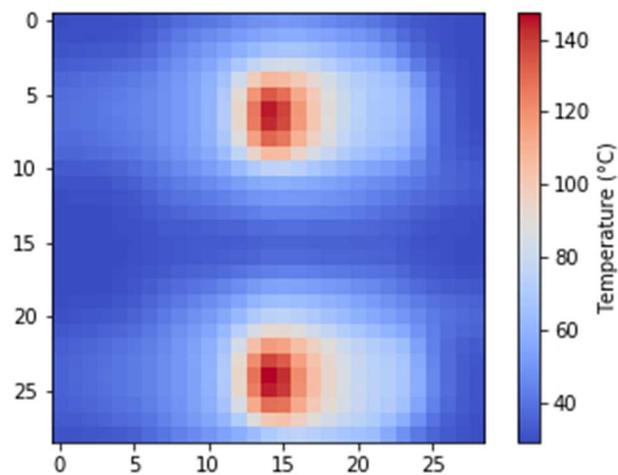


Figure 6 : Temperature map of the surface of a dual GaN transistors sample when a 2 V bias is applied simultaneously to each transistor obtained by IR thermography. The two hot spots are the zones where the GaN transistors are located. The axis numbers represent the number of pixels in each direction. The pixels are $25\ \mu\text{m} \times 25\ \mu\text{m}$ in size.

IV. CONCLUSIONS

We report on a new method to obtain the 3D temperature field in a RF chip based on a 3D heterogeneous integration of GaN HEMT and RF-SOI technologies under operating conditions using multiple distributed embedded RTDs as temperature sensors in different key locations, surface IR thermography to be coupled to multi-physics numerical simulations. The sample is made of a stack of multiple thin films of different materials including silicon, silicon oxides, silicon nitride and metals on top of an RF Si transistor fabricated on an RF-SOI substrate. One or multiple additional GaN transistors are mounted on top of the SOI stack. Experimental data obtained at the RTDs locations and at the sample surface show a maximum temperature of 147°C at the chip surface and more specifically at the center of the GaN transistors locations. They also show a decreasing temperature with an increasing depth due the effect of the surface heat source (GaN transistor) and the heat sink (substrate). We also observe different temperature distribution for single and multiple GaN transistors samples due to heat bridges in the

case of multiple transistors. Obtained results suggest and efficient cooling strategy should remove the heat directly from the transistors surface rather than from the chip backside due to a large thermal resistance of the stack. A numerical model of the chip we previously developed under COMSOL Multiphysics for the SOI has been adapted to include the GaN transistors. Its calibration is the key next step of this work in order to improve the agreement between numerical and experimental data as we have previously done for similar chips[16]. The numerical model can then be used as a tool to optimize the thermal management of the whole chip.

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