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Design of three-level flying-capacitor commutation cells with four paralleled 650V/60A GaN HEMTs

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Abstract — This paper presents two improved solutions (Vertical and Horizontal commutation cells) for three-level flying capacitor (FC) topologies with four 650 V / 60 A (25 mΩ) GS66516T GaN (Gallium Nitride) HEMTs (High Electron Mobility Transistors) in parallel per switch intended to be used in a 540 V / 70 kVA power drive system. Both solutions were built and experimentally tested, as a buck converter, regarding switching speed (15.14 kV / μs max) and overvoltage (6 % max) for different current levels (7 A to 53 A).

Keywords — Flying capacitor, GaN HEMT, low inductance loop design, PCB Layout.

I. INTRODUCTION

The concept of More Electrical Aircraft (MEA) was raised with the idea to replace conventional non-electrical systems such as pneumatic hydraulic and mechanical with electrical systems in the aircraft. These changes are intended to reduce CO₂ emissions by reducing fuel consumption, which is achieved by increasing the power density and efficiency of these systems [1]. Many of these systems are power drives which are usually composed of an inverter, cables, EMC filters and a motor. Multilevel inverters are one promising technology in this field since the high number of output voltage levels allows the reduction of switching frequency (consequently reducing switching losses), decreases input and output filter size due to lower dV/dt . Authors in [2] show a promising topology for a MEA 70 kVA power drive system achieving power density and efficiency superior to 10 kW / kg and 98.5 % respectively, in a global optimization comprising cooling system and EMI filters among others. The structure presented in the referred paper is composed of three paralleled legs connected through non-coupled inductors. Each leg is a three-level FC (flying capacitor [3]) topology with four 650 V / 60 A GaN HEMT transistors (ref. GS66516T) in parallel per switch, as presented in Fig.1, totaling 16 semiconductors per leg.

The present paper proposes two solutions for three-level FC topology by optimizing power loops considering the complexity of paralleling four GS66516T devices per switch, as presented in [1]. The state of art of paralleling GaN HEMTs and the use in multilevel topologies is presented in Section II. The design characteristics of two solutions, that comprises gate driver and power loop is presented in Section III. Experimental

verification concerning loop inductance, proper functioning, switching speed and overvoltage, as well as the comparison between the two proposed solutions are presented in Section IV. Finally, the conclusions of the study are presented in Section V.

II. STATE OF ART OF PARALLELED GAN HEMTs

The state of the art of GaN HEMT applications presented in [4] compile more than 162 technical reports and research papers and highlight the main advantages of GaN HEMT in relation to Silicon based power switches: excellent temperature capabilities allowing much higher power density (9.5 kW / in³) and efficiency (up to 99.8 %) on power converters.

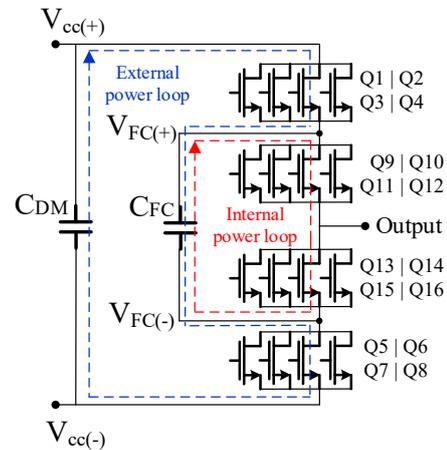


Fig. 1. Three level FC commutation cell with four 650 V / 60 A GaN HEMTs (GS66516T) in parallel.

One of the main characteristics of a Wide bandgap (WBG) semiconductors, as Silicon Carbide (SiC) MOSFETs and GaN HEMTs, is to present lower output capacitance. This implies a high switching speed as high as 100 V / ns for GaN HEMTs [5]. Due to high dV/dt and dI/dt , parasitic inductances of printed circuit board traces (PCB) are critical to safe operation of GaN HEMTs, by reducing voltage spikes on drain and source voltage, EMI noise and switching losses [6][7][8].

Reducing commutation loop inductance is probably the most affordable solution to reduce voltage across stray loop

inductances due to high di/dt [9], if packaged devices are used, since it only depends on PCB routing. The challenges of paralleling four GaN HEMTs 650 V/ 60 A (GS66516T) are presented in [9] and [10] for a half-bridge topology. Beyond power loop reduction (0.7 nH [9] and 0.81 nH [10]), gate driver loop must also be optimized (4.2 nH [9] and 2.5 nH/3.6 nH [10]) to reduce V_{GS} ringing and overshoot. An additional degree of complexity is inserted in power loop optimization for multilevel series topologies, since the power loop is defined by more than one commutation cell. In the three-level FC topology presented in Figure 1, the external power loop (in blue) is formed by all switches, C_{DM} and C_{FC} . While the internal power loop (in red) is formed by only inner switches and C_{FC} . By cascading FC commutation cells, the number of power loops is defined by the number of output voltage levels -1, and the flying capacitor of the innermost commutation cell will be part of the preceding commutation cell power loop.

The use of 650 V/ 30 A GaN HEMTs in multilevel series topologies, with no paralleled devices, is presented in a 1 kW three-level Active Neutral Point Clamped (ANPC) [11] achieving 3.51 nH and 5.37 nH for power loops. On the other hand, the use of FC topology is presented in [12] and [13] for a nine-level and a ten-level topology, respectively, with no paralleled devices. To reduce power loop inductances (2.32 nH [12] and 2.7 nH [13]), the complementary switches are oppositely placed on PCB top and bottom layers with ceramic flying capacitors placed in the input and output of each commutation cell.

Among the reviewed papers, despite the parallelism of GaN HEMTs and their use in multilevel series converters, the two problematics have not been addressed together: parallelism of GaN HEMTs in multilevel series converters. This is the main subject addressed in the present paper.

III. DESIGN OF A THREE-LEVEL FLYING CAPACITOR

As presented in the previous section, the key to parallel multiple devices is to guarantee a symmetric layout. In [9] and [10], a similar schematic for a two level with two paralleled GaN is presented as shown in Fig. 2. Current sharing between the devices is strongly dependent of gate loop inductances, in green, $L_{G1}\sim L_{G4}$, power loop inductances $L_{P1}\sim L_{P5}$ and the mutual M_1 and M_2 . In the case of four devices in parallel, the same reasoning can be done with the double of parasitic elements.

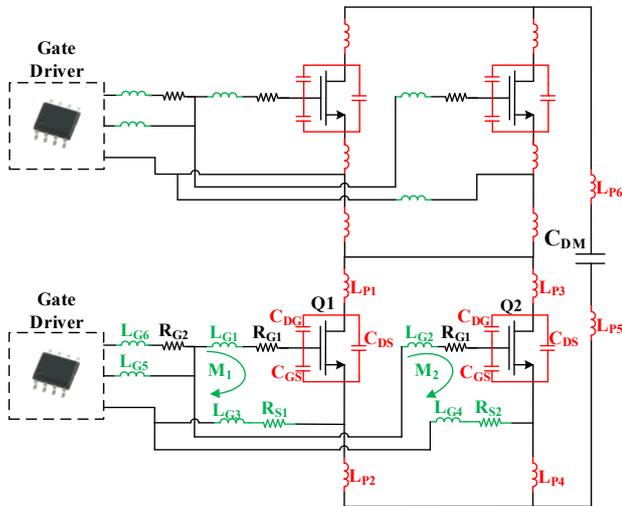


Fig. 2. Two paralleled GaN HEMTs in a two level commutation cell and their respective gate and power loops parasitic inductances.

To guarantee paralleled devices equal current sharing, the layout must consider, not only to minimize these inductances but $L_{G1} = L_{G2}$ and $L_{G3} = L_{G4}$, as $L_{P1} = L_{P3}$, $L_{P2} = L_{P4}$ and $L_{P5} = L_{P6}$. Next, the details of the gate and loop layout developed in this work will be explored.

A. Gate Driver Design

Gate loop inductances ($L_{G1}\sim L_{G4}$) presented in Fig. 2 have a strong impact on V_{GS} ringing and overshoot that can be increased if a strong unbalance between these loops is verified [9]. To reduce V_{GS} ringing, it is interesting to split R_{G1} [10] between C_{iss} (input capacitance) of paralleled devices, resulting in a R_{G-on} (turn-on resistance) equal to $R_{G1} + R_{G2}$ per device. On the other hand, R_{G-off} (turn-off resistance) is defined only by R_{G1} . The same idea of splitting resistors is employed with four paralleled transistors, so, one $R_{G1} = 1 \Omega$ is connected to each transistor in series with $R_{G2} = 5 \Omega$ for the present application.

In this project the isolate gate driver Si8271BBD-IS is used to control the four GaN HEMTs in parallel, totalizing four gate driver circuits for the three-level FC leg. The gate driver circuit layout is presented in Fig. 3 with four paralleled devices (two on the top layer and the other two on the bottom layer) based on the disposition proposed by [10]. Turn-on gate loops were estimated by using Ansys Q3D Extractor as 2.3 nH (green path in Fig. 3) and 2.5 nH for top and bottom devices respectively. Turn off gate loops, on the other hand, reached 3.6nH for both top and bottom devices (red path in Fig. 3). These gate loops' symmetry and values are achieved due to decoupling capacitors placed close to each device on both the bottom and top layers (680 nF p/ transistor), as shown in Fig. 3. This capacitor split also guarantees the balance between the quasi-common-source inductance (L_{G3} and L_{G4} showed in Fig. 2) discussed in [9], since the same distance between source connection of each GaN to respective decoupling is reached.

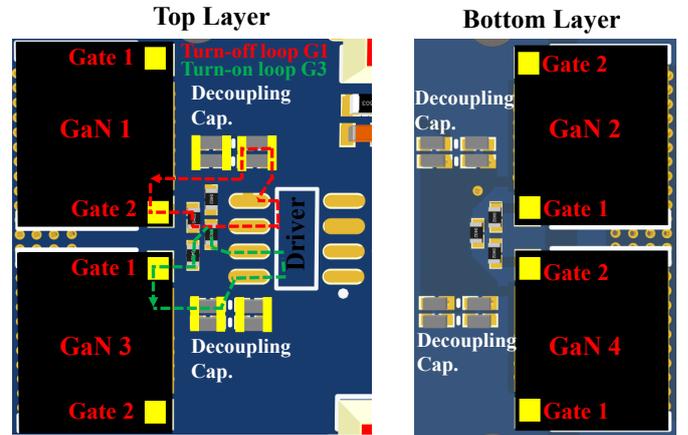


Fig. 3. Gate driver circuit responsible to drive four paralleled 650 V/ 60 A GaN HEMTs (GS66516T) in parallel with equivalent $R_{G-on} = 6 \Omega$ ($1 \Omega + 5 \Omega$) and $R_{G-off} = 1 \Omega$ per transistor. Turn-on gate loop path of GaN 3 is presented shown in green and turn-off loop of GaN 1 is presented in red.

Another important part of the gate driver design is the isolated power supply that will provide the 6 V (turn-on voltage) and -4 V (turn-off voltage) for each switch (four GaN HEMTs). This power supply must have an isolation capacitance as small as possible in order to attenuate the common-mode current passing through gate driver to auxiliary power supply [14] [7]. This common-mode current can distort the output of the isolated power supply and gate

driver, resulting in a risk to the integrity of the gate drive circuit as well as the converter itself [14]. The isolated power supply used is the 2 W/ 12 V NXE2S1212MC from Murata that presents only 3 pF. In other to regulate 12 V output voltage from the power supply, two zener diodes are connected in series, TDZ6V2J (6.2 V) and TDZ3V9J (-3.9 V), with a 400 Ω resistor.

B. Power Loops Design

Reducing power loop parasitic inductances can be done in different ways, as reducing the length of bus bars and supply terminals of the commutation cell, as well as choosing capacitors with low *ESL* (equivalent series inductance). However, the most effective way is to place ceramic capacitors as close as possible to the commutation cell [15]. These ceramic capacitors must have enough capacitance to provide the necessary energy lost and stored during a commutation instant, which is almost the same as the turn-on energy [16]. In the case of the designed commutation cell, in the worst case for C_{DM} , there would be eight GS66516T (Q1-Q4 and Q9-Q12 or Q5-Q8 and Q13-Q16) turning on at 270 V (half of bus voltage – 540 V) and 15 A for each transistor, totalizing 60 A, at the same time. The total energy lost at these conditions, according to GS66516T datasheet, would be $E_t = 8 \cdot 81 \mu\text{J} = 648 \mu\text{J}$. In the case of C_{FC} , there would be only four devices in the worst case (Q9-Q12 or Q13-Q16), totalizing 324 μJ . The final voltage level V_f at C_{DM} (or C_{FC}) providing the energy E_t at initial voltage V_{DC} is presented by [16], as:

$$V_f = \sqrt{V_{DC}^2 - \frac{2 \cdot E_t}{C_{DM \text{ or } FC}}} \quad (1)$$

By considering the maximum accepted voltage drop ($V_{DC} - V_f$) of 1 % (5.4 V) for C_{DM} and 2 % (5.4 V) for C_{FC} , a minimum value of 225 nF is needed for each one. Since these capacitors will be part of the power loops, the large the contact surface of these devices with the PCB tracks, the lower the loop inductance. Then, 8*225nF (CGA8M1X7T2J224K) of 630 V were used for C_{DM} and 6*225 nF (C3225X7T2W224K) of 450 V were used for C_{FC} , being half on the bottom layer and the other half on top layer to ensure symmetry.

According to Fig. 1, C_{FC} is part of external power loop with C_{DM} . Therefore, its positioning has direct impact on current high frequency path during the commutation of Q1-Q4 and Q5-Q8. The challenge consists on placing C_{FC} as close as possible to C_{DM} in order to reduce external power loop. However, it must take into account a safe distance between them, since they will be in different electric potential and it should not compromise internal power loop inductance. The proposed solution on this paper is to split C_{FC} in two parts. The first part is placed so the internal power loop is reduced, so, as close as possible between Q9-Q12 and Q13-Q16. The second part, named as C_{FC}' and C_{FC}'' (for the Horizontal version), is electrically connected in parallel with C_{FC} but they are placed close to C_{DM} , as presented in Fig. 4, allowing the reduction of the external power loop.

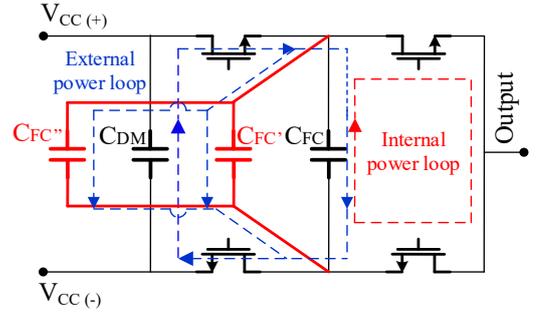


Fig. 4. C_{FC}' and C_{FC}'' positioning three level FC commutation cell.

They will provide a preferable path during Q1-Q4 and Q5-Q8 commutation regarding C_{FC} . On the other hand, since they are “electrically” far from Q9-Q12 and Q13-Q16, their contribution to the internal loop is way inferior compared to C_{FC} .

Power loop reduction is directly related to devices choice and positioning. In this paper it was defined that film capacitors (DC Link and flying capacitor) and output connectors should be placed on an external PCB (named mother board), in the way that the three-level FC commutation cell work as pluggable PCB. The present application consists of an input voltage of 540 V and output current of 43 A, working as a buck converter. To prevent flying capacitor voltage oscillation, some film capacitors were placed on the mother board. Therefore, the interface between the two PCBs should be done by a power connector with, at least, five power connections: $V_{CC(+)}$, $V_{CC(-)}$, $V_{FC(+)}$, $V_{FC(-)}$ and output connection. The connector 46114-1032 from Molex have the necessary power connections to handle the desired current and also signal connections that were used to transfer PWM signals, 12 V for the isolated power supplies and 5 V for the gate driver not isolated side.

By positioning the different devices (driver circuits, power connectors, ceramic capacitors and the 16 GaN HEMTs) different solutions were evaluated through simulations with Ansys Q3D extractor. Two solutions were selected to be build and tested, based on external and internal power loop inductances as other characteristics that are presented in Table I: Vertical and Horizontal versions.

TABLE I. THREE-LEVEL FLYING CAPACITOR COMMUTATION CELL VERSIONS CHARACTERISTICS

Commutation cells characteristics		
Item	Vertical	Horizontal
External Power Loop Inductance	6.4nH	4.4nH
Internal Power Loop Inductance	5.7nH	3.6nH
Dimensions	112mm x 94mm	132mm x 103mm
# Layers	6	8
Power Sense	Vertical	Horizontal
Gate Signal	Shielded	Shielded
Symmetry	Symmetric	Asymmetric
Increase # of output levels	Difficult	Easy
Signal and Power	Separated	Mixed

Both solutions present positive and negative points that can be used to justify the use of one over the other. Beyond the

differences of loop inductances, dimensions and the number of layers, three other characteristics must be pointed out:

1) Symmetry: This characteristic implies that high frequency current path for both top and bottom paralleled devices are identical. This characteristic may suggest that all paralleled devices will see the same impedance and consequently will switch with the same characteristics.

2) Increase of the number of output voltage levels: despite the objective of a three-level FC commutation cell, there is the interest of a PCB routing that can be generalized, in the way that flying capacitors cells can be easily cascaded in series to increase converter output voltage levels.

3) Signal and Power paths: Separate signal and power tracks is a good design rule for PCBs, it prevents noise propagation on signal tracks that can disrupt circuit proper functioning. Normally, the circuit is divided into regions with only signals and others for high current circulation.

The two different solutions shown in Table I are presented in detail in the following sections, highlighting the main differences about PCB layer stack, symmetry and power and signal separation.

C. Vertical commutation cell

The Vertical solution shown in Fig. 5 is formed by six layers (70 μ m copper thickness) and power flow between external and internal cell is in a vertical sense. Signals tracks (green arrows) are placed on the borders of the PCB, while power (yellow arrows) remains in the center. Half of all devices are placed on the bottom layer and measurement points were placed close to the power connector to evaluate commutation cell performance.

External power loop (represented in red) inductance was estimated by simulation as 6.4 nH with C_{FC} (0.9 μ F) and 10.8nH without it. This consists in 40.7 % reduction of loop inductance. On the other hand, the internal power loop achieved 5.7 nH with C_{FC} and 5.8 nH without it. These results confirm the idea of splitting ceramic flying capacitors can significantly reduce external power loop inductance and has minor impact on internal power loop.

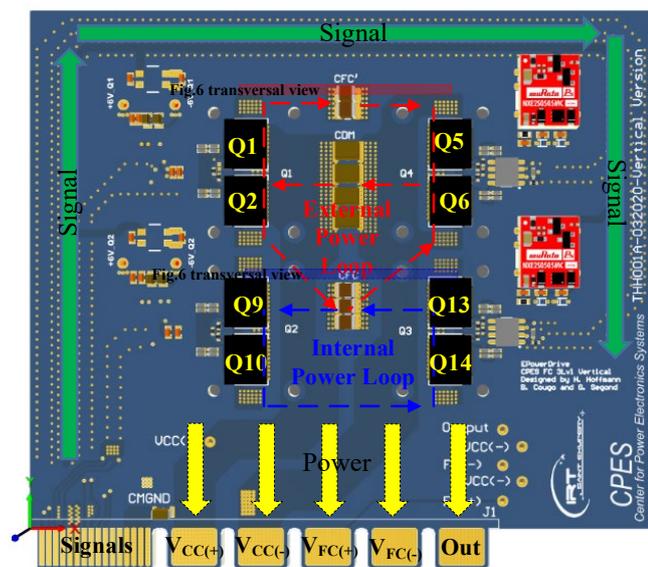


Fig. 5. Vertical version commutation cell top layer view. External power loop is presented in red and the internal power loop in blue, the green and yellow arrows presents signal and power separated path on the PCB.

Vertical version PCB has 112 mm x 94 mm and the layers were selected to ensure symmetry. In Fig. 6, it is presented two transversal cuts that show the high-frequency current path during commutation for the external (in red) and internal (in blue) power loops. Due to the presence of ceramic capacitors on both sides of the PCB, current is equally divided between top and bottom paralleled devices. However, this disposition with vertical power flow complicates cascading other flying capacitor cells in series without increasing the number of PCB layers. This is mainly due to the power connector location down on the board, since all flying capacitor connections must be connected to external film capacitors on the mother board.

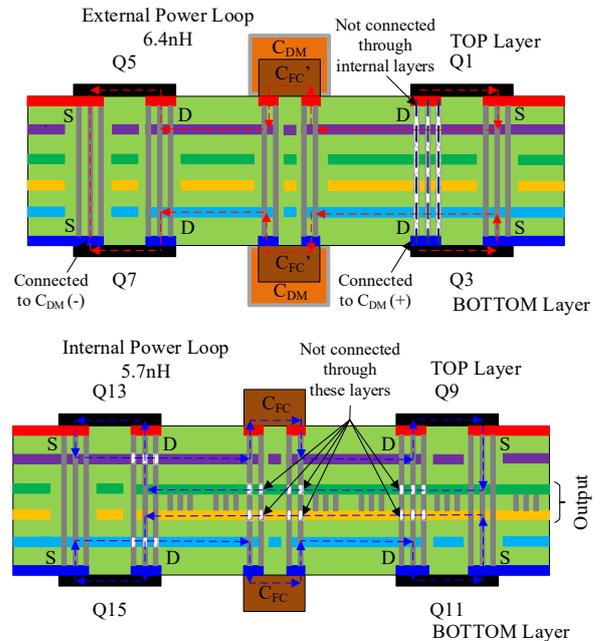


Fig. 6. PCB transversal view representing part of high frequencies current symmetric path for the Vertical version through PCB layers. The figure on the top represents the external power loop path (6.4 nH) and the figure on the bottom represents the internal power loop path (5.7 nH).

D. Horizontal commutation cell

The Horizontal solution shown in Fig. 7 is formed by eight layers (70 μ m copper thickness) and power flow between external and internal cell is in a horizontal sense. Signals and power tracks are superposed for Q5-Q8 and Q13-Q16. In that case, the layer stack has a different disposition to distance power and signals close to the power connector. The three bottom layers were reserved to signal and to solder bottom GaN HEMTs. This allows a shield to be made between PWM signals and power supply passing through the seventh layer between the sixth and eighth (bottom), as shown in Fig. 8.

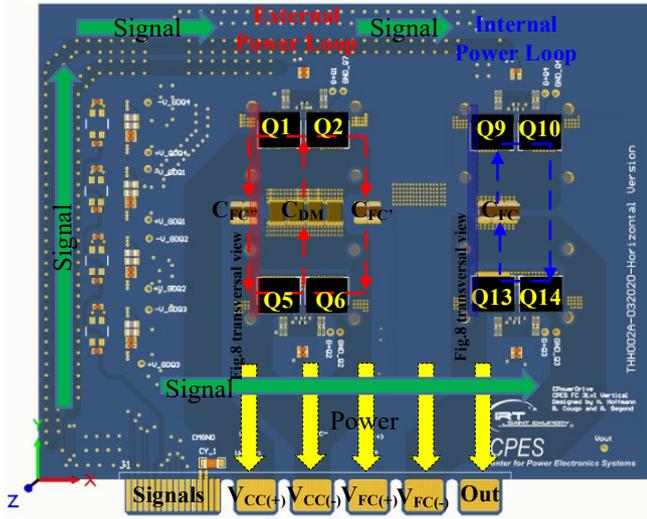


Fig. 7. Horizontal version commutation cell top layer view. External power loop is presented in red and the internal power loop in blue, the green and yellow arrows present the signal and power crossed path on the PCB close to the power connections.

Horizontal version PCB has 132 mm x 103 mm. Due to signal shielding and signal mix with power tracks, it is not possible to accomplish current symmetry between top and bottom devices as presented in Fig. 9, for both external and internal loops. Nevertheless, this version is easier to cascade flying capacitors cells in series with the same number of PCB layers as presented in Fig. 10. In that case, C_{FC}' can be used only for the first cell.

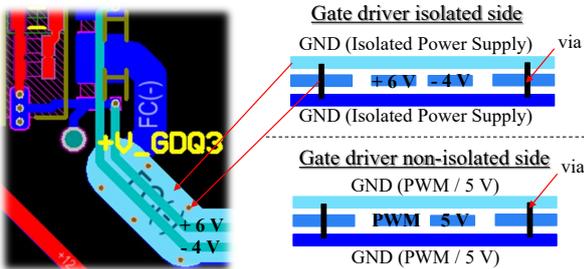


Fig. 8. Signal and auxiliary power supply shielding idea used both in Horizontal and Vertical versions to prevent coupling between power and signal tracks.

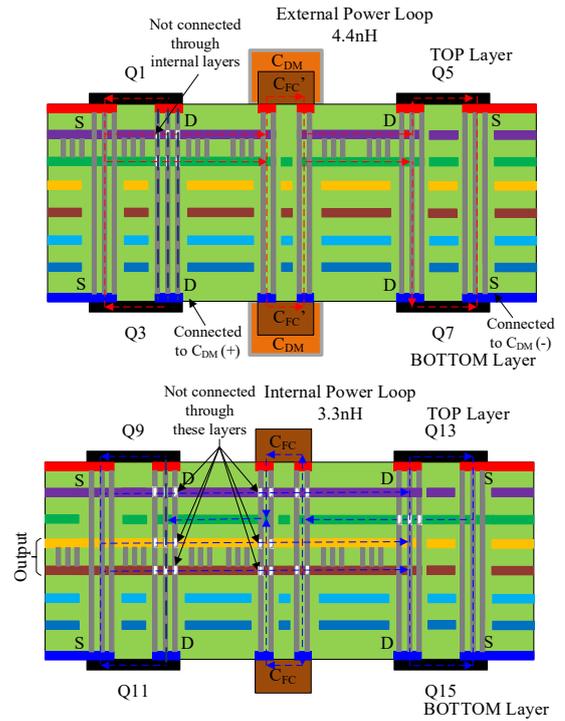


Fig. 9. PCB transversal view representing part of high frequencies current asymmetric path for the Vertical version through PCB layers. The figure on the top represents external power loop path (4.4 nH) and the figure on the bottom the internal power loop path (3.3 nH).

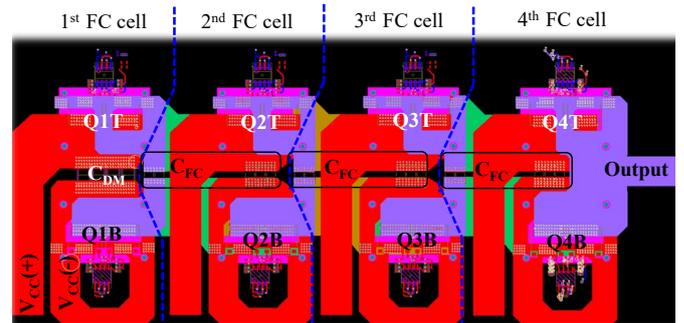


Fig. 10. Four FC cells connected (five level FC topology) in series based on the Horizontal version routing with 8 layers (5 layers used for power tracks).

IV. EXPERIMENTAL RESULTS

This section is dedicated to the experimental evaluation of the two versions presented in the previous sections. Firstly, PCBs power loop inductances are verified before soldering all devices. Then, switching speed and overvoltage at output voltage were verified for different current levels for the converter working as a buck converter with $V_{bus} = 540$ V, Duty cycle = 0.3 and switching frequency of 20 kHz.

A. Power Loop Inductance

Power Loop inductance measurement was performed to verify the results from simulation with Ansys Q3D Extractor. For this test, an impedance analyzer was used with an impedance pin probe presented in Fig. 11. All drain to source connections were shorted with conductor copper tape soldered to the respective connections. In the case of internal power loop, the probe was placed between C_{FC} connections as presented in Fig. 11. For external power loop measurement, $C_{FC} / C_{FC}' / C_{FC}''$ were shorted and pin probe was placed between C_{DM} connections.

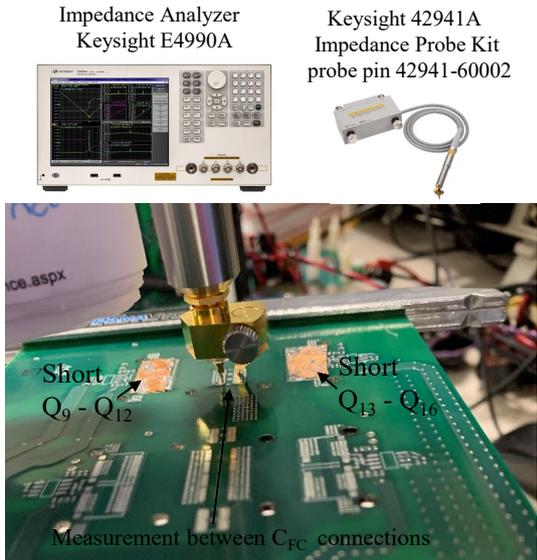


Fig. 11. Power loop inductance measurement for Horizontal version internal loop considering an impedance analyzer.

A good approximation is verified between the measurements and simulated values according to Table II at 100 MHz. A maximum error of 16 % was verified for the Internal loop of Horizontal Version.

TABLE II. SIMULATED AND MEASURED POWER LOOP INDUCTANCES FOR VERTICAL AND HORIZONTAL VERSIONS.

Parasitic Inductance		
Inductance	calculated (100 MHz)	Measured (100 MHz)
External Loop Horizontal V.	4.4 nH	4.9 nH
Internal Loop Horizontal V.	3.6 nH	4.2 nH
External Loop Vertical V.	6.4nH	6.8 nH
Internal Loop Vertical V.	5.7nH	6.4 nH

B. Switching speed and Overvoltage

The test setup to measure switching speed and overvoltage is shown in Fig. 11, where the Horizontal version is placed above a mother board where film capacitors are placed ($C_{DM-film} = 60 \mu\text{F}$ and $C_{FC-film} = 100 \mu\text{F}$) as well as input and output connectors. Voltage measurements were taken in the FC leg (after power connector) with the intent to verify waveforms as close as possible of the GaN HEMTs.

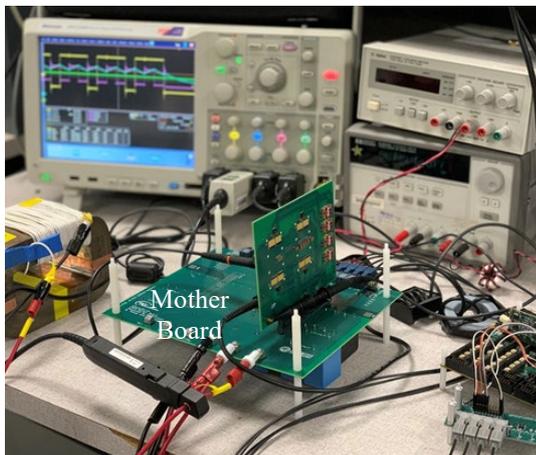


Fig. 12. Test setup with the Horizontal version connected in the motherboard. Power supply (540 V) and an inductive load is also connected to the motherboard, as well as PWM signals generated by a DSP (TMDSDOCK28379D) with an optical interface.

Two heat sinks (3-100707U from CoolInnovations) were considered for the four paralleled GaNs, as presented in Fig. 13, totaling eight (total of 50 g) per board. These two heat sinks were connected through four screws guaranteeing the same potential. A thin layer of thermal paste was considered between GaNs and heat sink. Since heat sinks are electrically connected to transistors source terminal, tests were carried out without connecting all eight heat sinks between them.

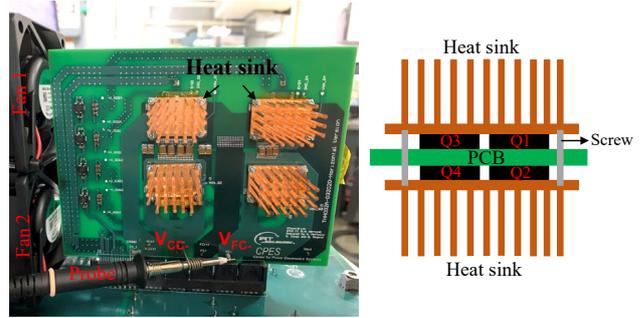


Fig. 13. Cooling system. Two heat sinks were used per four devices, that are electrically connected through four screws. Thermal paste was considered between devices and heat sinks. Additionally, two fans were placed as close as possible of the PCB.

Waveforms in Fig. 14 show the output voltage in green for 42 A (in yellow), and the flying capacitor voltage with an unbalance around of 5.5 V (2 % of 270 V) at 20 kHz. The output voltage has an equivalent switching frequency of 40 kHz, and each voltage step is related with an external loop device switching and the following step with a device of the the internal loop. The difference between the commutation of one device from the internal or the external loop is also identified by the overvoltage during commutation. The larger the loop inductance, the larger the oscillations as the overvoltage observed. In Fig. 15, it is verified that external loop causes higher overshoot than internal power loop when a device is switched, reaching maximum 6 % of output steady-state voltage (around 270 V) at 43 A.

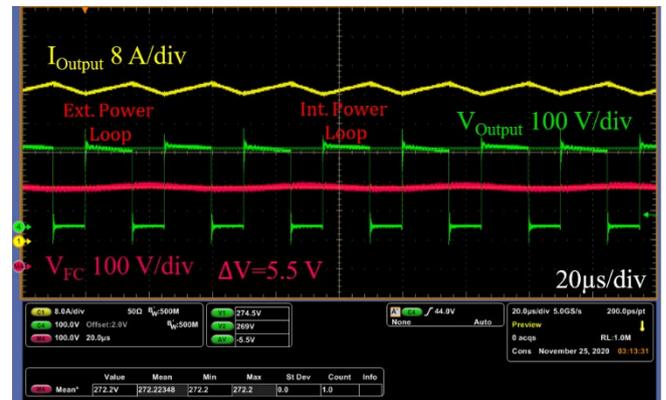


Fig. 14. Measured waveforms of Horizontal version working as a buck converter with $V_{bus} = 540 \text{ V}$, Duty cycle = 0.3, Output Current (I_{Output}) = 42.08 A at 20 kHz. The output voltage V_{Output} is shown in green.

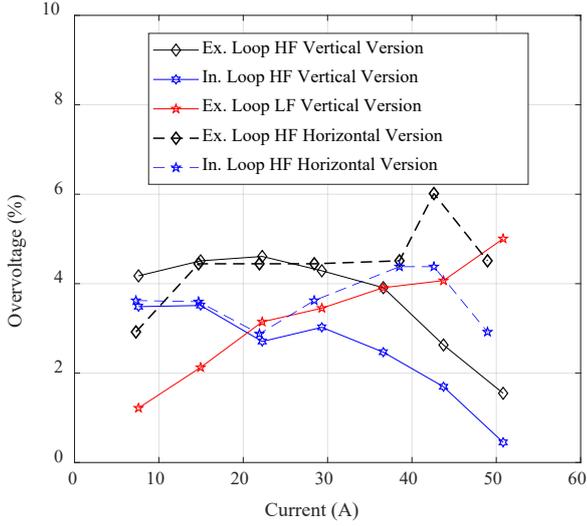


Fig. 15. Output voltage peak value measured for Horizontal and Vertical versions during the turn-on and turn-off for different current levels. Tests were performed with the commutation cell working as a buck converter with $V_{bus} = 540$ V, Duty cycle = 0.3 and $f_{sw} = 20$ kHz.

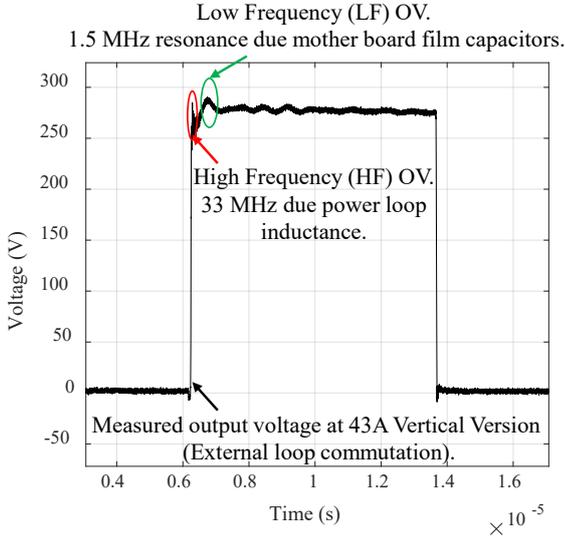


Fig. 16. In this picture overvoltage is highlighted the according to oscillation frequency of 33MHz (HF) due to power loop inductance and 1.5MHz (LF) due to the resonance with the film capacitors placed on mother board

Fig. 16 shows the overvoltage due to commutation, called HF (High frequency) and dependence on power loop inductance, but also (in red) the overvoltage due to resonance of film capacitors placed in the mother board, named LF (Low frequency). These two resonances are shown in Fig. 16, where 33 MHz was measured for HF and 1.5 MHz for LF. It is noticed that overvoltage caused by HF reduces with the current level, whereas the one caused by LF increases. But still, for the highest tested current level, it is under 6% (16.2 V).

Switching speed is presented in Fig. 17 for turn-on and turn-off, from 7 A to 53 A. Turn-off speed is dependent of output current and C_{oss} as presented in [17] and [18]. This behavior is valid if channel current (I_{Output}) does not reach the minimum value to guarantee $V_{GS} > V_{TH}$, then the channel is not formed characterizing the absence of miller effect. The

high the current, the miller effect takes place and dV/dt is less dependent of I_{Output} . Similar results (turn off) are verified for both versions, except for low current (7 A). At this current, each GaN device is switching around 1.75 A, then the switch speed is basically due to the charge and discharge of C_{oss} and parallel parasitic capacitances of PCB. The difference between the two versions (3.58 kV/ μ s Horizontal version and 2.26 kV/ μ s Vertical version) suggests that the Vertical version may have higher parasitic PCB parasitic capacitances, if all GaN devices presents the same C_{oss} .

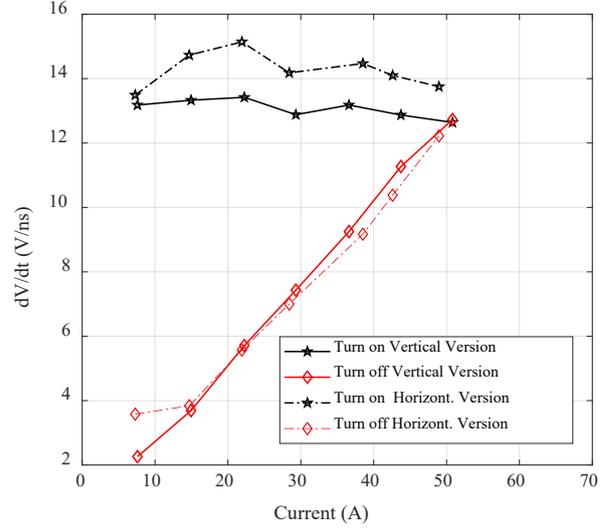


Fig. 17. Measured dV/dt for Horizontal and Vertical versions during the turn-on and turn-off for different current levels.

Turn-on switching speed, on the other hand mainly controlled by gate charge current, depending on V_{GS} ($V_{DR} - V_{GSP}$), R_{gon} and C_{GD} [19]. Gate drive voltage V_{DR} is defined by the isolated power supply and V_{GSP} is the Miller plateau voltage that increases with the current [18]. Therefore, a small decay is verified in turn on switching speed with current increase. The fact of having lower loop inductances corroborates that Vertical version presents higher switching speed than Horizontal version, reaching 15.14 kV/ μ s at 22 A against 13.42 kV/ μ s, a difference of 12.5 %. In general, dV/dt is relatively low compared to other GaN applications, this is due to the limitation of the gate driver output current (2 A_{pk}) to charge 4 x C_{GS} and gate turn on resistance of 5.25 Ω to guarantee converter proper functioning.

V. CONCLUSIONS

This paper presents two design solutions for three level FC with four devices 650V/60A (25 m Ω) GS66516T in parallel per switch. The Horizontal version presents lower loop inductances (4.4 nH / 3.6 nH) but 8 layers and asymmetry between top and bottom paralleled devices. It can reach 15.14 kV/ μ s during turn-on and may present lower PCB stray capacitances due to higher turn-off (3.58 kV/ μ s) speed at low current. The main advantage of this solution is the possibility to easily cascade FC cells in series, while the proximity of the signal and power tracks goes against PCB good design practices. The Vertical version, on the other hand, is composed of 6 layers and a symmetrical arrangement of the components that compromises loop inductance (6.4 nH / 5.7 nH). This solution reaches 13.42 kV/ μ s during turn-on and 2.26 kV/ μ s

during turn-off at a low current. This solution allows the separation between signal and power tracks, reaching a completely symmetrical circuit between the top and bottom devices as well as layers disposition.

It is worth to point out that power connectors have a big impact on routing and device disposition. So, the conclusions presented in this paper can differ if another power connector is used. Both solutions present the same gate circuit design and consequently the same gate loop (around 2.5 nH). Gate drivers have a strong influence on devices switching speed due to output current limitation that must charge all gate to source capacitances of paralleled devices.

The key to reduce power loop inductances in flying capacitor topologies with paralleled GaN devices is to split ceramic capacitors C_{FC} and consider a portion close to precedent capacitors (close to C_{DM} in the case of a three-level topology). This insight reduced power loop inductance by around 41 %.

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