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Preconditioning of Ohmic p-GaN power HEMT for reproducible V_{th} measurements

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Abstract

The fluctuation of the threshold voltage (V_{th}) presents a challenge while monitoring electrical drift in reliability studies of GaN HEMTs. While technologies, such as ohmic p-GaN, may lessen V_{th} fluctuations, the issue of recoverable charge trapping still remains. Therefore, it is crucial to adopt novel characterization methods when conducting reliability studies, in order to measure intrinsic changes rather than the charge-trapping effects that exist even in non-degraded transistors. One method expounded in this paper allows for a reliable and replicable measurement of V_{th} for an ohmic p-GaN gate HEMT GaN. A dedicated gate-bias profile is introduced immediately prior to the threshold-voltage measurement to stabilize it. This preconditioning phase necessitates a negative bias voltage followed by a suitably high voltage to be effective. The novel protocol introduced is also shown to be applicable to other HEMT GaN structures.

Keywords:

Ohmic p-GaN transistors, threshold voltage shift, preconditioning protocol, threshold voltage shift, trapping, reliability

1. Introduction

The threshold voltage (V_{th}) instability is a well-known problem for GaN transistors and has been the focus of numerous studies in recent years, particularly with regards to Schottky gate contacts [1; 2; 3].

The use of an ohmic gate contact is intended to mitigate V_{th} instability by introducing holes into the AlGaIn barrier and GaN buffer layers [4]. Despite this, fluctuation of the threshold voltage have been observed in several studies [5; 6; 7].

Unstable measured value of V_{th} is problematic when tracking V_{th} drift in reliability studies. To overcome this issue, preconditioning methods are available to obtain reproducible measurements for Schottky gate contact [8; 9], including the authors' previous works on Schottky-gate-type [10]. In [9], preconditioning for ohmic gate structure was studied with a different protocol from the one proposed in this work.

Our previous study on preconditioning enables reproducible measurement of the threshold-voltage value by simply applying a high positive gate voltage that allows to inject holes into the GaN layers [10]. This induces hole trapping and stabilizes V_{th} . Nonetheless, we found that this protocol cannot be used for Gate Injection Transistors (GIT) as it does not stabilize the measurement of V_{th} value.

This paper presents an extended version of our previous protocol, with a new modified method that applies to both Schottky and ohmic type p-GaN HEMTs. Hypotheses are proposed to explain the improved stabilization mechanism.

2. Experimental details

The main device under examination (DUT) in this investigation is a GIT transistor fabricated with an Ohmic p-GaN gate. It is rated at 600 V, 60 A, 55 mΩ. The procedure has been tested on a lot of ten transistors.

The threshold voltage (V_{th}) is measured by gradually increasing the gate voltage (V_{GS}) and drain voltage (V_{DS}) simultaneously at the same potential. This method therefore mimics a measurement with the gate and drain connected together.

The threshold voltage can also be measured by increasing V_{GS} while applying a constant V_{DS} bias. Although the value obtained by this method may differ slightly, it can still be used with this protocol. In our previous study ([10], the manufacturer of the Schottky gate device tested used this setup. Our decision to maintain a non-constant V_{DS} enables a comparison with previous results and facilitates an analysis of the differences between the two technologies under similar conditions.

The measurements were conducted at room temperature using a Keysight B1505A curve tracer/analyzer, with probe needles placed on the metal contact via an MPI2000-DP probe station.

The threshold voltage is defined as the gate voltage when the drain current value reaches $I_D = 400$ mA. This level is selected to be well after the "knee part" of the curve which allows for an easier reading and a negligible gate-current level compared with the drain current (figure 1 and 2).

In figure 1(a), the instability of V_{th} is illustrated. We observed a variation $((V_{th,max} - V_{th,min})/V_{th,min})$ of around 4.3%. Although this variation is low compared to Schottky-gate p-

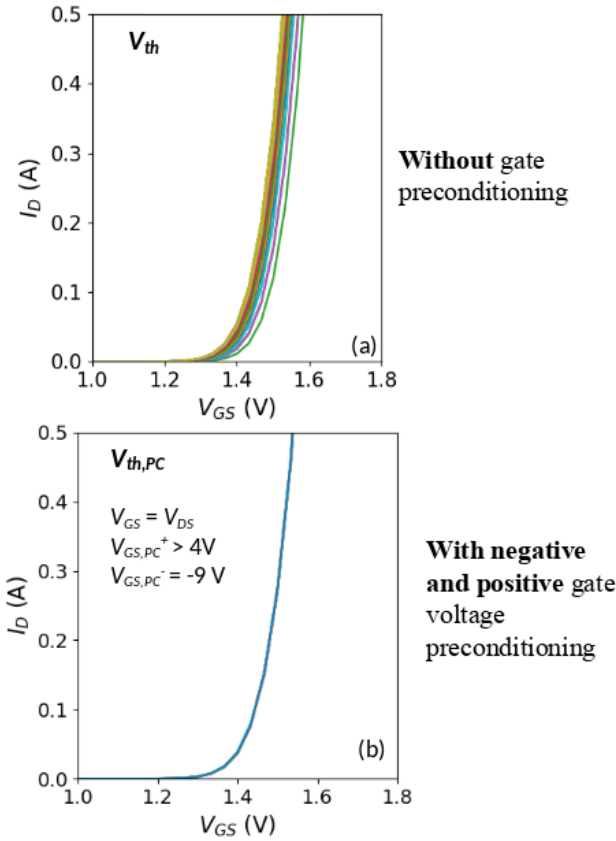


Figure 1: (a) Several measurements of V_{th} with different measurement histories such as after a positive or negative gate bias or drain bias (always within the ratings) which are related to other characterization measurements on the B1505A such as gate leakage measurement I_{gss} : V_{GS} ramped between 0 and -9 V in backward and between 0 and +7 V in forward, or drain leakage current I_{dss} : V_{DS} ramped between 0 and 600 V in a few seconds. It can be seen that the V_{th} measurement is dependent from the polarization history. (b) Several measurements of V_{th} with the same types of history but with preconditioning phase included just before the measurement phase. It is striking that the preconditioning reduces the variation of V_{th} and that the same value is retrieved each time no matter the previous measurement done.

GaN HEMT which is higher than 40 % [10], it may still be too significant to analyse gate degradation through the monitoring of V_{th} in reliability studies.

3. Preconditioning of the gate of the DUT

The preconditioning protocol is described in figure 3. A negative voltage bias $V_{GS,PC-}$ was applied to the gate for five seconds at the lowest admissible value of -9 V, as recommended by the manufacturer for this part number. Then, for the next five seconds, a voltage of $V_{GS,PC+}$ equal to or greater than 4 V is applied to the transistor gate to inject charges, making the threshold voltage stable and reproducible ($V_{th,PC}$).

To precisely control the time between the preconditioning phase (red box) and the V_{th} measurement phase (orange box), the B1505A was utilized in *direct control* mode.

The gate current is high enough to achieve preconditioning for $V_G > 4$ V (see figure 2(a)). Using voltage values above the D_{pin} threshold (around 2.5 V) 2(b) ensures hole injection which

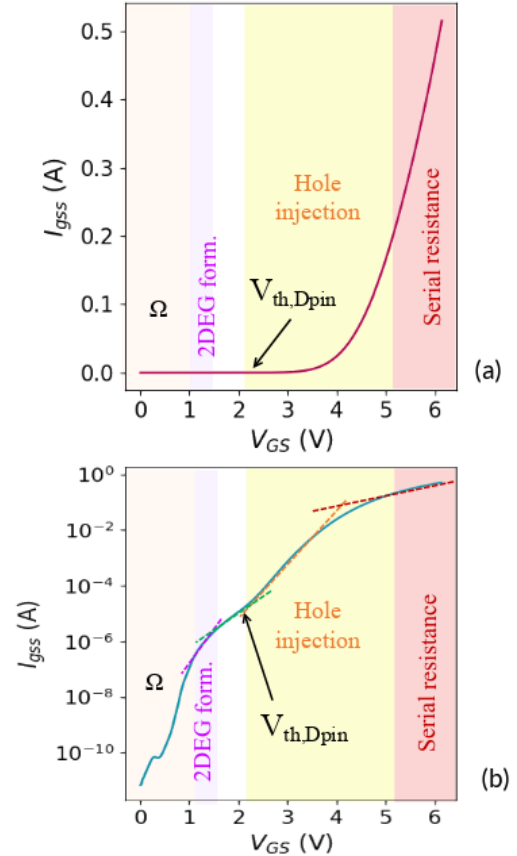


Figure 2: Gate leakage current $I_{gss} = f(V_{GS})$. (a) linear display, the leakage current increases from $V_{GS} \approx 2.5$ V, at this value the threshold voltage of the equivalent D_{pin} diode is reached. (b) log-scale display of the i_{gss} current. The log scale allows to shows all phases of the gate stack conduction mechanism: ohmic, ohmic and leakage with the 2DEG, hole injection and serial resistance.

help in stabilising the V_{th} , however an effective preconditioning requires a large amount of charge which is obtained only when the diode is fully on (above 4 V).

In figure 2(b), for V_{GS} between 0 and 1 V the conduction is purely ohmic (leakage). Above 1 V, the conduction behavior changes due to the formation of the 2DEG under the gate, and electrons are injected through tunneling. At higher voltage level, hole injection begins with the activation of the p-GaN: AlGaN/GaN diode [11]. Above 4 V the current is high enough to observe the effect of the serial resistance.

Only considering the $V_{GS,PC+}$ phase, the value must be greater than 4 V to be in the right conduction phase which implies enough injected holes.

A measurement, such as I_{dss} , is added in between two V_{th} measurements to verify the effectiveness of a set of preconditioning parameters. The I_{dss} measurement was mainly utilized due to its substantial influence on the V_{th} drift. Nevertheless, the procedure was also finally assessed with all other typical measurement used for characterization, including gate-leakage or on-resistance measurements. The yielded outcomes were identical.

A stable threshold-voltage value was never achieved by only applying either $V_{GS,PC-}$ or $V_{GS,PC+}$. Indeed, in both

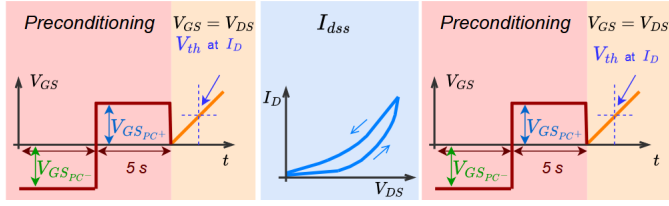


Figure 3: Protocol used in measurements on the test system: first in red the preconditioning part of the gate to obtain reproducible values of V_{th} , then in orange the actual V_{th} measurement phase. In blue any other measurement that influences the measurement of the threshold voltage such as I_{dss} displayed as an example for this figure. This later measurement is performed in between two preconditioned- V_{th} measurements to assess the stability achieved with the tested protocol parameters.

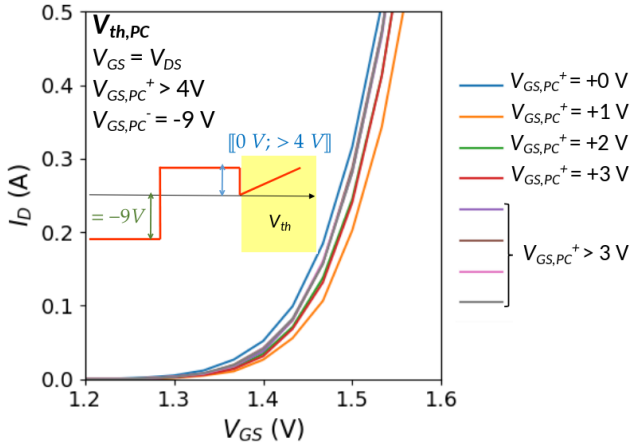


Figure 4: Shift of V_{th} depending of the $V_{GS,PC+}$ applied that follow $V_{GS,PC-} = -9$ V. It can be seen that $V_{GS,PC-} = -9$ V and $V_{GS,PC+} > 4$ V give a stable value of V_{th} . The current I_G reached at 4 V is 1 mA (datasheet maximum ratings) and is limited by the source measurement unit (SMU) chosen compliance.

case, a progressive decrease of the V_{th} is observed while the measurement are repeated. Moreover, an increase in the preconditioning voltage, in absolute value, leads to a further reduction of V_{th} .

It is actually necessary to apply both negative and positive gate bias to achieve stability in the threshold voltage value. Indeed, the reduction of V_{th} is stronger for negative bias than for positive, and the combination of both (as shown in Figure 3) results in an increase in the threshold voltage depending on the applied $V_{GS,PC+}$, as seen in Figure 4. First, the V_{th} increases at low voltages (below the D_{pin} threshold voltage of the gate stack), and then it decreases to become stable for $V_{GS,PC+}$ above 3 V.

The mechanism accountable for the rise in V_{th} (as detailed in the subsequent section) is only achieved through the combination of negative and positive gate bias. This process is necessary to attain stabilization of V_{th} and consequently, optimize the preconditioning of the ohmic p-GaN HEMT.

4. Hypothesis about the mechanisms of preconditioning.

It has to be underline that both the trapped charge within the device and all the measurement parameters (including timings)

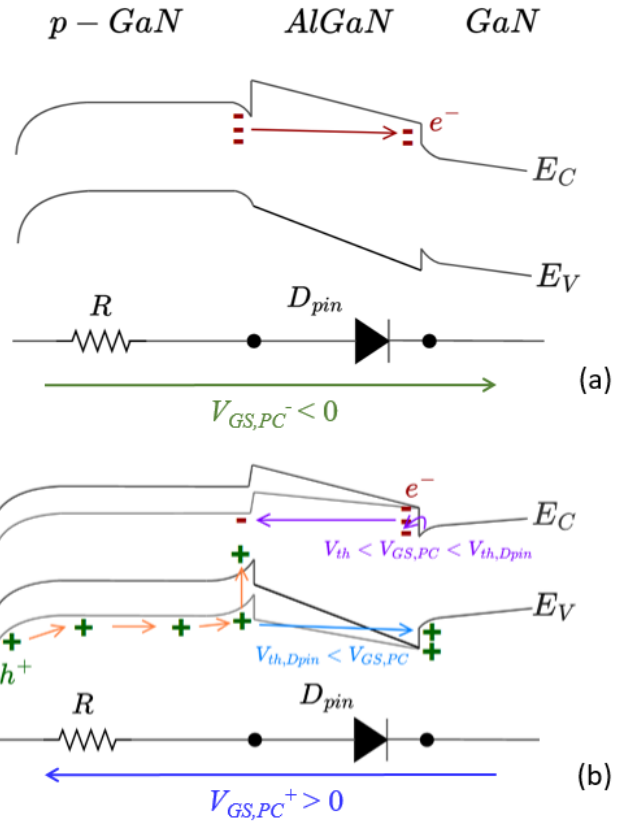


Figure 5: Simplified band diagram of the gate stack of the DUT under negative bias ($V_{GS,PC-}$)(a) [12; 13] and under positive bias ($V_{GS,PC+}$)(b), the mechanism in red is electron trapping at the interface AlGaIn/GaN and in violet at the p-GaN/AlGaIn interface. The hole trapping in the p-GaN layer is illustrated in orange. The hole depletion over the barrier to reach the buffer responsible for the preconditioning of V_{th} is only possible if the trapped negative charges are mainly at the AlGaIn/GaN interface and not in the p-GaN layer. This situation is depicted in blue.

needs to be well controlled by the preconditioning phase and the curve-tracer (timings through direct control, sweeping slopes...) respectively. It is then guaranteed that the same conditions are applied at each $V_{th,PC}$ -measurements which make this protocol successful.

As expressed in our previous work, our hypothesis states that only holes trapped within the GaN layer are capable of generating stable trapped charges to obtain a repeatable V_{th} . However, for an ohmic-gate transistor architecture, it works only if $V_{GS,PC-}$ is applied before a positive polarization $V_{GS,PC+} > 3$ V for an extended period of time (5 seconds) to amplify the likelihood of hole trapping.

The negative phase (applied $V_{GS,PC-}$) is essential to eliminate the trapped electron in the p-GaN layer via the electric field or, at least, attain a reproducible occupation rate. The trapped electrons shall shift towards the AlGaIn/GaN interface (depicted in red in figure 5 [14; 15]).

The origin of the previously trapped electrons can be explained by other mechanisms not related to the preconditioning phase but to the previous history of the device. According to [16; 12], it can be explained by the movement of the electrons

of the 2DEG with the upward movement of the quasi-Fermi level with low positive gate bias (resulting in AlGaN barrier lowering). Some of these electrons can recombine with holes in the p-GaN and others get trapped in the p-GaN.

Then the application of a high positive gate bias of at least $V_{GS,PC+} > 3\text{ V}$ enables hole injection into the AlGaN/GaN interface through the equivalent D_{pin} diode (AlGaN/GaN diode) of the gate stack (shown in blue in figure 5). The threshold voltage of the D_{pin} diode is approximately 2.5 V.

These trapped charges appear to be more stable than charges trapped in the p-GaN region, for instance, as they exhibit less tunneling and have a higher time constant. These positive charges will create a positive electric polarization near the 2DEG, which results in a reduction of the threshold voltage value [5; 4]. This phenomenon can be observed in figure 4.

The stabilization of the threshold voltage and effectiveness of preconditioning require the implementation of the hole injection mechanism. If $V_{GS,PC+}$ is lower than 3 V, the D_{pin} will not be activated and not enough holes will be able to reach the AlGaN/GaN interface. In this case, electron injection near the 2DEG in the AlGaN barrier (violet mechanism in figure 5) becomes the dominant mechanism. These charges produce a negative electric polarization close to the 2DEG, reducing the amount of electrons in the 2DEG and causing an increase in the V_{th} shown in figure 4 for $V_{GS,PC+} < 2\text{ V}$ (below the D_{pin} threshold voltage). These trapped charges are unstable and can quickly combine with acceptors in the barrier, unable to maintain stability in the threshold voltage during measurement.

The drain current leakage, $I_{dss} = f(V_{DS})$ that can be measured right after $V_{th,PC}$ such as depicted in figure 4, demonstrates changes post $V_{th,PC}$, which are related to the $V_{GS,PC+}$ phase. For $V_{GS,PC+} > 3\text{ V}$ the hysteresis is more pronounced, indicating that more charges are trapped due to the preconditioning protocol because holes are injected through the D_{pin} diode after $V_{GS} = 2.5\text{ V}$.

The rise in I_{dss} , as shown in Figure 6(b), may be due to holes trapped in the buffer layer changing the overall electrical polarization of the layers and it boosts the electron density in the 2DEG. This I_{dss} effect is more pronounced at low V_{DS} in particular before the depletion caused by the field as the blocking area is smaller (only the area under the p-GaN). The polarization of the p-GaN layer is constant, the additional polarization caused by injected holes counteracts the p-GaN effect which increases the leakage current. At high voltage, this effect is less significant because the field plates increase the depletion area. The most populated 2DEG caused by the injected holes leads to a smaller channel equivalent resistance, the leakage current at the same V_{GS} (always 0 V for this measurement) is then increased.

In terms of protocol parameters optimization, the preconditioning voltage used should be the maximum values advised by the manufacturer datasheet to ensure a better trapping probability. The preconditioning times of figure 3 could be the subject of another study to be minimized while keeping the same effectiveness than in this study for each part number.

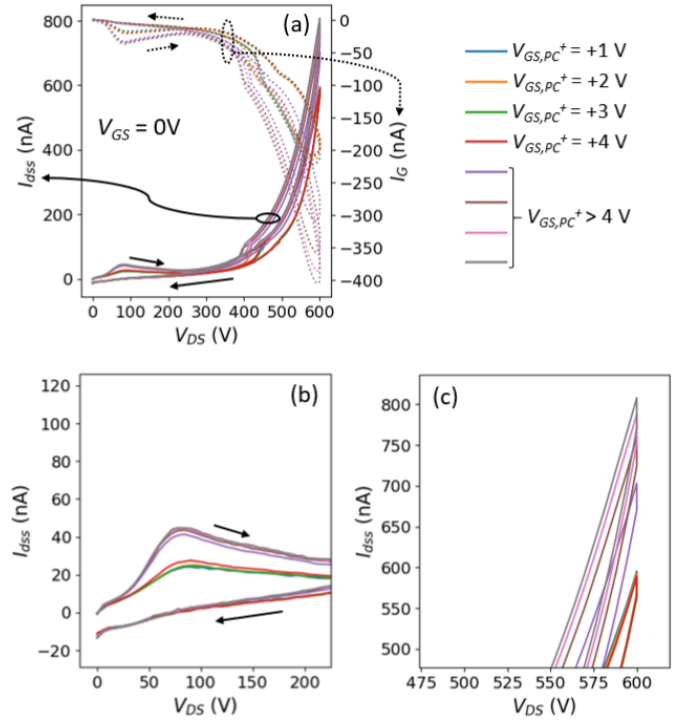


Figure 6: (a) Current leakage $I_{dss} = f(V_{DS})$ at $V_{GS} = 0\text{ V}$ after the preconditioned V_{th} measurement for $V_{GS,PC-} = -9\text{ V}$ and $V_{GS,PC+}$ between 1 V and 7 V. (b) zoom on the small V_{DS} values, (c) zoom on the high V_{DS} values. V_{DS} sweep is done forward and backward to take into account a possible hysteresis effect.

5. Application to other structures and manufacturers of HEMT GaN.

The preconditioning protocol described here is effective for the studied ohmic- gate GaN HEMT.

In our previous study [10], the negative part $V_{GS,PC-}$ was found unnecessary to obtain stable and reproducible $V_{th,PC}$ in a 650 V and a 100 V Schottky gate HEMT GaN (manufacturer 1). We have applied the protocol outlined in this paper to these transistors and another Schottky gate HEMT from a different manufacturer (manufacturer 2).

The aim is to establish a universal and efficient method for all technologies that produces satisfactory results and simplify the process.

Referring to figure 7 and table 1, it is evident that the new protocol leads to excellent measurement stability. For the Schottky-gate HEMT transistors produced by manufacturer 1, the variation remains below 0.1%. The value of $V_{th,PC}$ differs from the one reported in [10] due to different preconditioning, but the stability remains the same. It is observed that this technology exhibits reasonable stability despite being intrinsically less stable. The voltage bias values utilized are the highest acceptable values specified by each manufacturer.

The device from manufacturer 2 remains sensitive on historical factors that can affect V_{th} by up to 1%. While it may suffice for most studies, optimization may be necessary to further reduce this fluctuation. Compared to other technologies, intentional trapping procedure (preconditioning) seems more chal-

lenging to leverage, most probably due to variations in design, layer quality, and thickness.

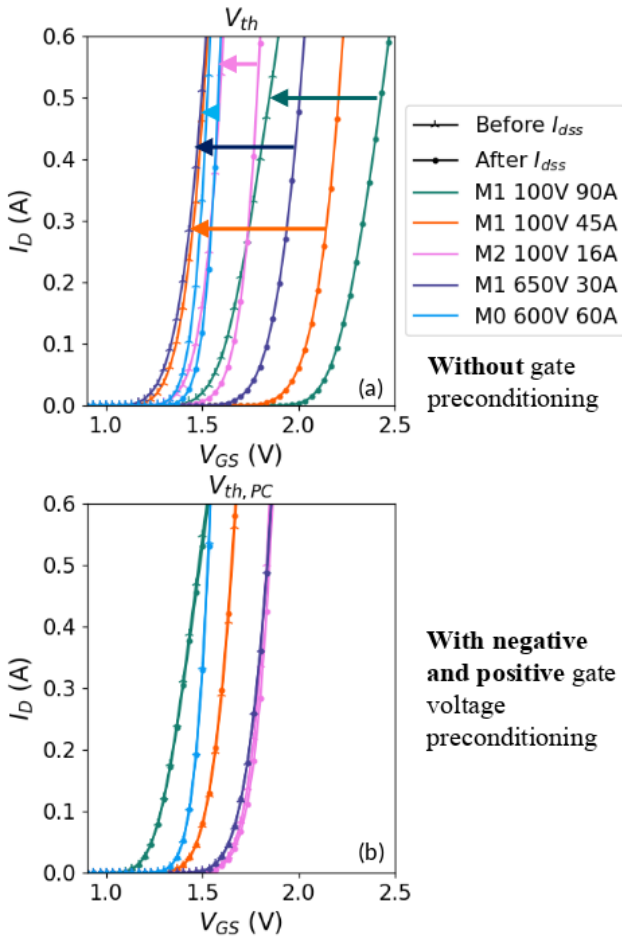


Figure 7: V_{th} measurement stability improvement illustrated on five different transistors including the DUT of this paper. (a) History effect illustrated by the comparison of two non preconditioned V_{th} measurements before and after an I_{dss} measurement. (b) Comparison of two preconditioned V_{th} : $V_{th,PC}$ after I_{dss} . It is striking that the preconditioning phase gives a stable value of V_{th} or at least drastically reduces the variation due to the biasing history.

6. Conclusion

Adding a preconditioning phase immediately prior to measuring the threshold voltage allows for reproducible V_{th} measurements. This phase, to be effective for both Schottky and Ohmic p-GaN HEMT involves negative biasing the gate for a few seconds, followed by forward biasing above the threshold voltage of the gate-stack pin diode. These biases should be applied long enough to completely saturate any negative shifts of the threshold voltage linked to hole injection into the buffer. The injection of holes is confirmed by the increase of static leakage current I_{dss} and change of hysteresis. This preconditioning protocol is applicable to several p-GaN HEMT structures and gives a stable and reproducible measurement of the threshold voltage.

Table 1: Comparison of the maximum variation of V_{th} and $V_{th,PC}$ obtained for different bias history (within the ratings of each part number reference).

Device part number	standard V_{th}	$V_{th,PC}$
Schottky p-GaN 100 V 90A (manuf. 1)	40 %	0.1 %
Schottky p-GaN 100V 45 A (manuf. 1)	40 %	0.1 %
Schottky p-GaN 100 16 A (manuf. 2)	18 %	< 1 %
Schottky p-GaN 650V 30 A (manuf. 1)	40 %	0.1 %
GIT 600 V 60 A (manuf. 0)	4.3 %	< 0.1 %

7. Acknowledgments

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