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S-parameters characterization of GaN power transistors for high frequency power converters design

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Abstract

Gallium Nitride (GaN) power devices that have been developed these recent years are ideals candidates for high frequency power conversion, leading to a reduction of size, cost and weight of power converters. This work presents a new modeling methodology of GaN power transistors based on radiofrequency characterizations in order to design efficient high frequency high power converters. The characterization of extrinsic and intrinsic device's parasitic up to the gigahertz range using 2-port S-parameters measurements and characterization fixtures designed on printed circuit boards is presented in this paper.

Introduction

Classical power electronics characterizations, such as Double Pulse Test, provide data on the switching behavior of power devices, however there are limitations to understand the real switching process. In order to design efficient power converters at high frequencies, having accurate devices models in a wide frequency range is of great interest. This work proposes a new method based on radiofrequency (RF) techniques such as pulsed I(V) and S-parameters measurements. The GaN High Electron Mobility Transistor (HEMT) GS66502B 650V/7.5A will be used to develop our methodology. The model of such a component, shown in figure 1(a), is composed of the channel and the gate diodes which are represented by nonlinear current sources, the intrinsic nonlinear capacitances and the extrinsic parasitic due to internal design and packaging effects. This paper presents the use of new characterization fixtures to extract model parameters. The frequency range for this study is 1 MHz to 1 GHz.

Calibration for S-parameters characterization

S-parameters measurement is widely used for RF transistors characterization due to its accuracy up to frequencies higher than the gigahertz range. The technique lies on performing a 2-port measurement, using a Vectorial Network Analyzer (VNA), considering the transistor as a quadripole and determining the parameters of the equivalent circuit for a specific bias couple (V_{GS}, V_{DS}). However this measurement requires coaxial connections which are not suitable to characterize packaged power transistors. Thus a specific test fixture has been designed on printed circuit board using transmission lines and coaxial connectors to propagate RF signals as shown in figure 1(b). Then the problem encountered is the need to separate the effects of the transmission medium (in which the device is embedded for testing) from the device characteristics. Figure 1(c) gives the equivalent circuit of the test fixture. Y_0 represents the coupling between the transmission line and the ground plane. This parameter is determined using the OPEN 1-Port calibration standard presented figure 1(d). Z_1, Z_2, Z_3 are the transmission lines impedances and are given by the THRU standard (cf. figure 1(d)). Y_4, Y_5, Y_6 result from the capacitive coupling between lines and are obtained using the OPEN 2-Ports standard (cf. figure 1(d)).

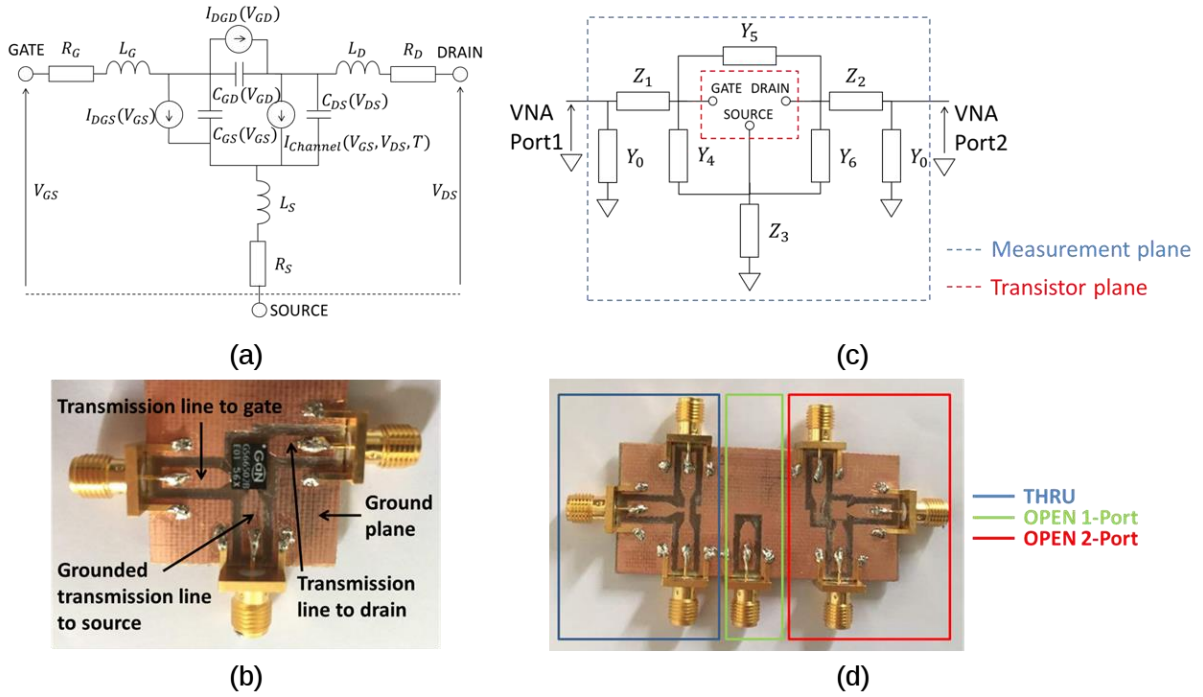


Figure 1: (a) Transistor model (b) Test fixture to characterize the transistor using S-parameters (c) Equivalent circuit of the test fixture (d) Calibration standards

The calibration process developed in this work allows getting the impedance parameters (Z-parameters) at the input of the transistor in the device reference plane. Therefore the extrinsic and intrinsic parameters from the model in figure 1(a) can be extracted.

Extrinsic resistances extraction

Extrinsic resistances are important parameters for power losses estimation and driving circuit design. “Cold FET” technique [1] consists in applying a specific bias to the transistor to simplify its equivalent scheme. The drain and source are shorted ($V_{DS} = 0V$) in order to cancel the channel conduction and a gate to source voltage $V_{GS} = 6V$ allows shunting C_{DS} . Thus, referring to figure 1(a), the transistor’s equivalent circuit is made of three impedances:

$$\underline{Z}_G = R_G + \frac{G_G}{G_G^2 + C_G^2 \omega^2} + j \left(L_G - \frac{C_G}{G_G^2 + C_G^2 \omega^2} \right) \omega ; \underline{Z}_D = R_D + jL_D \omega ; \underline{Z}_S = R_S + jL_S \omega \quad (1)$$

C_G is the remaining gate capacitance related to C_{GS} and C_{GD} . G_G is the gate diodes conductance related to I_{DGS} and I_{DGD} . R_D and R_S are extracted from the real parts of \underline{Z}_D and \underline{Z}_S respectively, while R_G is extracted from the real part of \underline{Z}_G at high frequencies. The extracted resistances are presented in figure 2(a) and the values given by the manufacturer are shown as indicators.

Parasitic capacitances extraction at pinch-off state

The internal capacitances of the device have significant effects on the switching behavior and power losses. By biasing the gate of the transistor at $V_{GS} = 0V$ (below the threshold voltage), every current sources in figure 1(a) are canceled. Thus, after deleting the effects of the extrinsic parameters determined previously, the inter-electrode capacitances C_{GS} , C_{GD} and C_{DS} are obtained. The test bench used to extract these capacitances is shown in figure 2(b). High voltage “Bias Tee” systems have been designed to couple bias and RF signals and allow accurate measurements from 2 MHz to 500 MHz. The evolution of the input capacitance $C_{ISS} = C_{GS} + C_{GD}$, the output capacitance $C_{OSS} = C_{DS} + C_{GD}$ and the Miller capacitance $C_{RSS} = C_{GD}$ is given in figure 2(c) at $V_{GS} = 0V$ and V_{DS} up to 200V and are

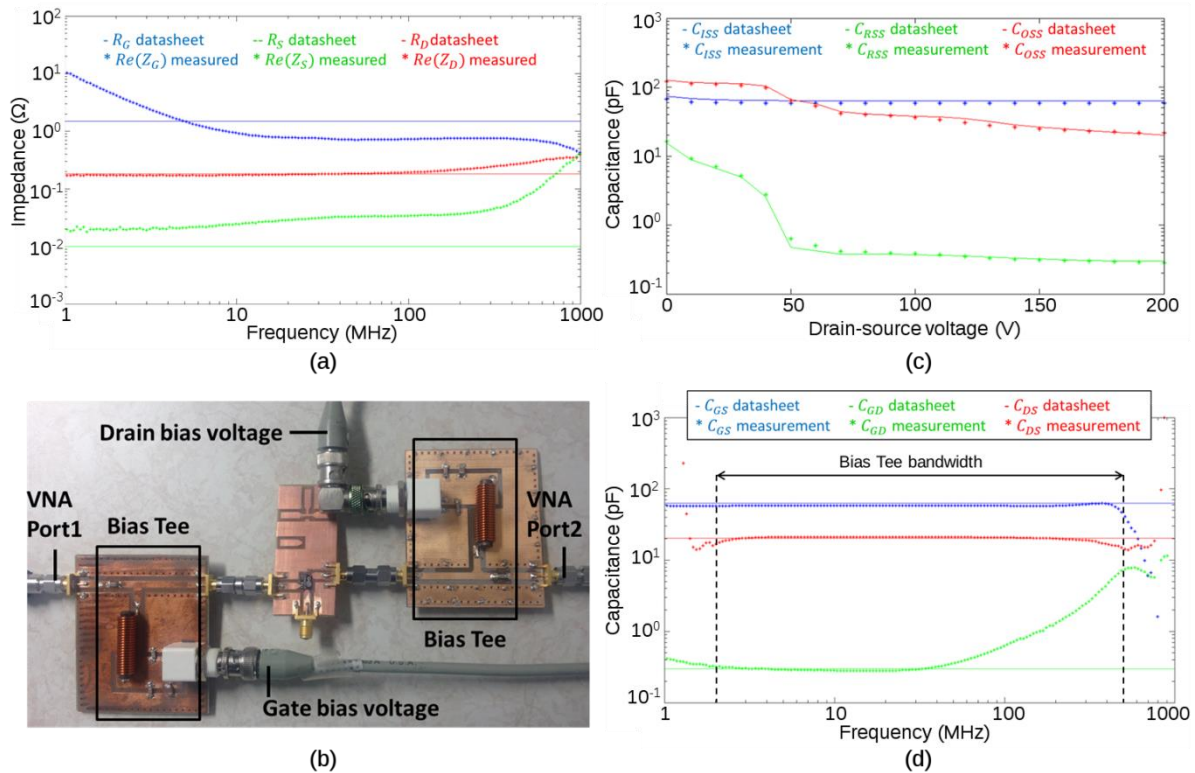


Figure 2: (a) Extrinsic resistances vs. frequency (b) Experimental test bench (c) capacitances at pinch-off vs. voltage at 10 MHz (d) Capacitances at pinch-off vs. frequency at $V_{DS} = 200V$

extracted at 10 MHz. The extracted capacitances values in the study frequency range are presented in figure 2(d) at $V_{DS} = 200V$. The values given by the manufacturer are shown as indicators. Other results will be given in the full paper version.

Conclusion

In this paper, the use of S-parameters is proposed to characterize GaN power transistors for high frequency power conversion applications. Previously a method to characterize the inter-electrode capacitances of GaN transistors using S-parameters and current probes up to the picofarad range and up to 2 MHz has been proposed [2]. The method proposed in this work, inspired from RF characterization techniques, allows determining accurately the capacitances below the picofarad range and in a wider frequency band. Furthermore, the method only requires simple and low cost test fixtures designed on classical printed circuit boards and potentially allows extracting all parameters of the device, such as extrinsic parts which have significant impacts on power converters efficiency. The next steps are to characterize the device's channel using DC and pulsed I(V) measurements [3]. A method to extract the extrinsic inductances will be proposed in the final paper. Then a complete model of the transistor can be built and experimentally validated.

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