**Advancements in HZO Layer Engineering for Ultimate 3D Vertical Transistors : Towards a Logic-In-Memory Application**

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In recent years, the Von Neumann bottleneck has become increasingly evident in computing device fabrication, prompting the research community to explore alternative architectures that address the data transfer issue between memory and processing units while minimizing energy consumption. One promising architecture is memory computing[1] or LiM architecture, which involves integrating the memory unit closely or within the same cell as the processing unit. Ferroelectric materials play a crucial role in this approach, as they exhibit remanent and reversible polarization when subjected to an external electrical field. Hafnium oxide (HfO2) emerges as a strong candidate due to its ferroelectric behaviour observed since 2011[2], along with its compatibility with High-k CMOS materials commonly used in semiconductor manufacturing.

In this study, we present a comprehensive investigation of the Hf-Zr (Hf0.5Zr0.5O2 - HZO) doped layer for its integration in 3D transistors. Our starting point is on characterizing the material properties of this layer when integrated into planar devices with a thickness of 10nm of HZO on a Si substrate, along with a 1.5nm SiO2 interfacial layer and a TiN capping layer. We explore the stabilization parameters of HZO in its orthorhombic crystalline phase at low anneal temperatures starting from 400°C. The orthorhombic phase is verified using XRD measurements, and the ferroelectric properties are analysed through electrical measurements for different fabrication parameters. Moreover, we investigate the crystallization of the HZO layer on both planar and 3D vertical nanowire structures using TEM observations. Our findings confirm the presence of nanosize HZO grains on the sidewalls of the nanowires, establishing their crystalline nature.

Furthermore, we have investigated the challenges associated with integrating this layer into 3D nanostructures. Specifically, we have employed anisotropic plasma etching techniques with optimized end point detection to selectively remove the TiN/HZO/SiO2 stack from the extremities of 3D vertical nanostructures. This process ensures the removal of unwanted layers while preserving the integrity of the ferroelectric layers surrounding the nanostructures, facilitating the subsequent formation of alloy contacts. Additionally, we propose a novel approach for performing ferroelectric polarization characterization on an actual 3D architecture, allowing for a comprehensive characterization of the ferroelectric properties in a realistic device configuration.

This research provides insights and expertise for incorporating HZO in 3D NW-FET technology, paving the way for a disruptive vertical logic-in-memory cell.

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*[2] T.S.Bösche, Appl. Phys. Lett., (2011)*

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