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High quality drift layer thickness scaling in vertical GaN-on-Silicon PIN diodes

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Abstract

We report on high drift layer quality in vertical PIN diodes grown on silicon substrate combining low $R_{on} = 0.35 \text{ m}\Omega\cdot\text{cm}^2$, and high critical electric field of 1.82 MV/cm . The impact of the drift region thickness on the device performances shows an excellent breakdown scaling with $640 \text{ V} / 820 \text{ V}$ for $3.5 \mu\text{m} / 4.5 \mu\text{m}$ drift layer thickness, favourably comparable to the state-of-the-art.

Introduction

As response to the need of developing new materials that surpass silicon limitation in the field of power electronics, lateral GaN based devices have been demonstrating their potential by combining high physical properties such as high critical electric field, electron mobility and low cost of fabrication. Despite these advantages, the development of lateral GaN devices has been restrained by trapping issues and large size of components. By analogy with the transition of silicon power devices from lateral to vertical structure (end of the 1960s), the transition from lateral to vertical GaN based devices is critical. That is why, there is an increasing interest from the research community on vertical devices grown on bulk GaN, thus demonstrating the high potential of these devices: with a better management of the electric field, an avalanche capability, small fingerprint, and certainly less prone to trapping effects as compared to lateral architectures. However, native GaN substrates are currently expensive with limited wafer diameter.

In this work, cost-effective GaN-on-Silicon vertical architectures are investigated. High quality quasi- and fully-vertical GaN-on Si P-I-N diodes have been fabricated showing high breakdown voltage, low R_{on} and excellent drift layer thickness scaling. Although quasi-vertical devices are good test vehicles to evaluate the material properties, this architecture suffers from the so-called crowding effect, additional parasitic resistance and sidewall leakage issues preventing large size devices with low R_{on} . Therefore, the fully vertical configuration is desired to unlock the potential of vertical GaN-on-Silicon power devices.

Device processing

Two heterostructures have been grown on silicon substrate with similar epi-layers except for the drift layer thickness. The growth started with a nucleation and buffer layers followed by an 800 nm thick N^+ -GaN layer ($5 \times 10^{18} \text{ cm}^{-3}$) and a drift layer ($3 \times 10^{16} \text{ cm}^{-3}$) with 2 different thicknesses $t_1 = 3.5 \mu\text{m}$ and $t_2 = 4.5 \mu\text{m}$. The top P-GaN layer is 700 nm thick with a Mg doping of $5 \times 10^{19} \text{ cm}^{-3}$ and a corresponding active doping of $3 \times 10^{17} \text{ cm}^{-3}$ (see Fig. 1). Fabrication of quasi-vertical PIN diodes started with a Cl2/Ar deep mesa etching using ICP. This step allowed the establishment of the Ti/Al/Ni/Au ohmic contacts that were formed on top of the N^+ layer. The P top layer was contacted with Pd/Ni/Au to form ohmic contacts. Finally, a rapid thermal annealing at 600°C was performed to alloy both n- and p-type ohmic contacts. In the case of fully vertical PIN diodes, the fabrication starts with a mesa etching to isolate the device. The P-GaN ohmic contact metal stack was deposited and annealed at 600°C using RTA. After protection of the front side, the silicon substrate and the buffer layers are locally removed using DRIE and ICP etching, respectively all the way to the N^+ layer. Then, the backside N^+ layer is contacted with a Ti/Au metal stack by sputtering.

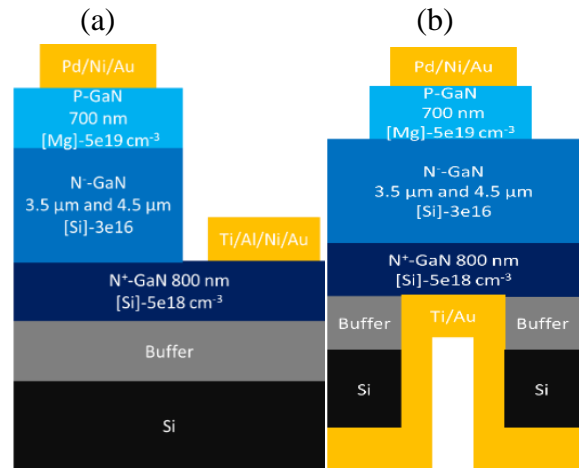


Fig. 1. (a) Quasi-vertical and (b) fully vertical schematic cross section of PIN diodes.

Results and Discussion

Fig.2. (a) shows the current density vs voltage $J(V)$ for the quasi-vertical PIN diodes ($3.5 \mu\text{m}$ and $4.5 \mu\text{m}$ of drift thickness). Since the two diodes have a similar doping within the drift region, the resulting R_{on} is quite similar for both PIN diodes between 0.3 to $0.35 \text{ m}\Omega\cdot\text{cm}^2$ (Fig.2. (b)).

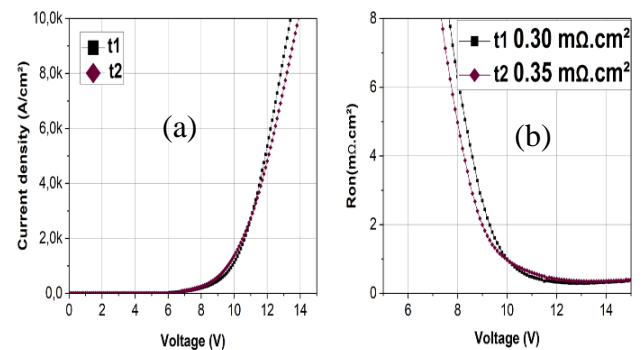


Fig. 2. (a) On-state characteristics of quasi-vertical PIN diodes. (b) R_{on} extraction from $J(V)$ curves

The two diodes showed a high breakdown voltage of 640 V for t_1 and 820 V for t_2 , respectively (see Fig. 3.a). This translates to the same breakdown field of about 1.8 MV/cm in both cases, thus showing an excellent scalability of the drift layer thickness. Silvaco TCAD simulation tool was employed to extract the electric field distribution of the two diodes at the breakdown. A similar electric field distribution is observed, which confirms the proper thickness scaling.

It can be pointed out that no edge termination nor field plate have been used to enhance the breakdown voltage. Nevertheless, the breakdown vs R_{on} benchmark (Fig. 4) of quasi-vertical GaN-on-Si PIN diodes shows that the reported PIN diodes using $4.5 \mu\text{m}$ drift layer thickness are favourably comparable to the state-of-the-art with a BFOM (Baliga figure of merit) around 1.92 GW/cm^2 despite the absence of peak electric field mitigation.

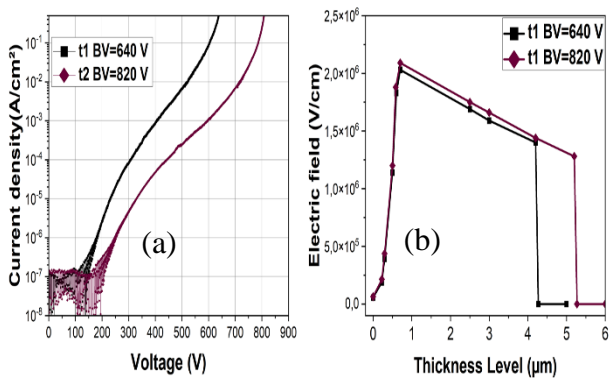


Fig. 3. (a) Off-state characteristics of quasi-vertical PIN diodes (b) TCAD simulation of the electric field distribution at the breakdown voltage

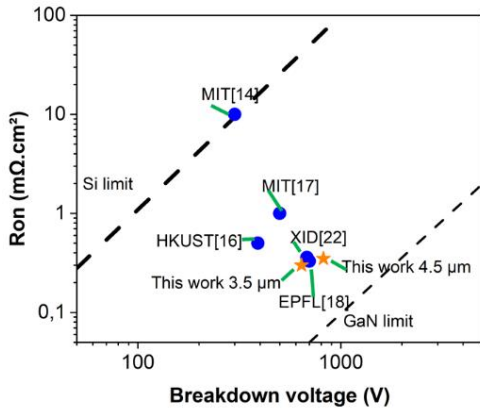


Fig. 4. Benchmark of quasi-vertical GaN-on-Si PIN diodes

As can be observed in Fig. 5.a, the quasi-vertical structure suffers from a current crowding effect within the N+ layer, generating an additional parasitic resistance. This represents a major bottleneck for the quasi-vertical configuration as this result in a significant Ron degradation when increasing the anode size. Simulation shows that the Ron of fully vertical diodes will be independent on the device dimension (Fig. 5.b).

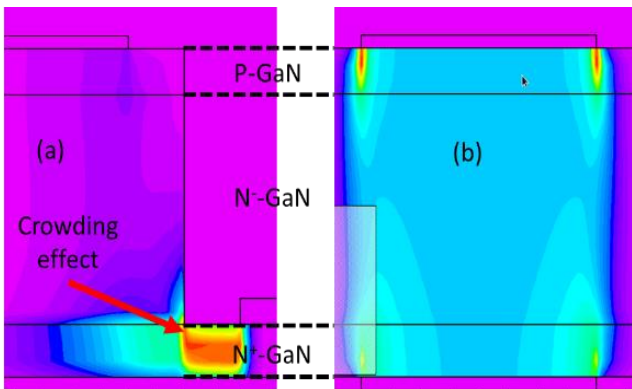


Fig. 5. Current density distribution of (a) quasi-vertical (showing crowding effect) and (b) fully vertical PIN diode

Fully vertical PIN diodes deliver an identical breakdown voltage than the quasi-vertical devices (Fig. 6.a). The benchmark of drift layer doping vs critical electric field shows the possibility to reach 2 MV/cm by further tuning the drift layer doping and achieve kV-class breakdown voltage (Fig. 6.b).

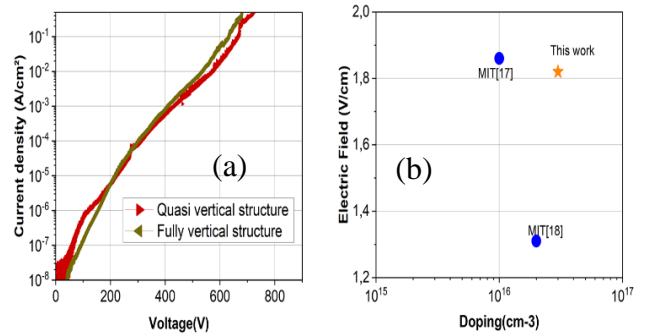


Fig. 6. (a) Comparison of BV of the fully and quasi vertical PIN diodes (b) Benchmark of doping vs electric field of fully vertical GaN-on-Si-PIN diodes

Conclusions

In this work, vertical GaN-on-Silicon PIN diodes were investigated with respect to the thickness of the drift layer and device architecture. High quality PIN diodes were demonstrated with low Ron (<0.35 mΩ.cm²), high critical electric field of 1.82 MV/cm, and excellent scaling of the breakdown voltage with the drift layer thickness delivering a BV of 640 V and 820 V for 3.5 μm and 4.5 μm. No edge termination nor field plates were implemented to improve the breakdown voltage, which further proves the excellent quality of the process and epi-layers. The achievement of the same breakdown capability but potentially much lower Ron with large anode size, confirms the potential of fully vertical GaN-on-Silicon devices for power electronics.

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