

Process optimization of Fully Vertical GaN-on-Silicon PIN diodes

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Lateral GaN-on-silicon power transistors are now qualified up to 650 V voltage operation [1]. On the other hand, the development of cost-effective GaN-based vertical devices grown on large diameter silicon substrate combines the advantages of potentially higher voltage operation with avalanche mechanism, high current, high threshold voltage together with a smaller footprint, unreachable with lateral transistors. In addition, vertical architectures rely on current conduction through a drift layer with a uniformly distributed electric field that should prevent the issue of surface charge trapping effects [2]. Nevertheless, this technology is still at an early stage and both material and device fabrication need to be optimized. In this work, we report on process optimization of fully vertical GaN-on-Si PIN diodes delivering a state-of-the-art combination of breakdown voltage (BV) and on-state resistance (Ron).

The MOCVD grown structure consists in a nucleation and buffer layers followed by an 800 nm thick N+-GaN layer ($5 \times 10^{18} \text{ cm}^{-3}$) and a drift layer ($3 \times 10^{16} \text{ cm}^{-3}$) with a thickness of 4.5 μm . The top P-GaN layer is 700 nm thick with a doping of $5 \times 10^{19} \text{ cm}^{-3}$ and a corresponding active doping of $3 \times 10^{17} \text{ cm}^{-3}$. Key optimizations within the overall process flow are the achievement of low ohmic contact resistances on the p type and backside n+ layers. For the n+ backside contacts, the improvement has been achieved by means of TLMs fabrication within the membranes by laser writing lithography. An HCl-based pretreatment prior to the metal deposition has been used to overcome the specific oxidation of the N-face backside GaN layer resulting in extremely low contact resistances without the need of any additional annealing. Proper metal stack followed by an optimized annealing allowed for a significant drop of p-type contact resistances. The optimized fully vertical PIN diodes shows an ON state resistance below $0.2 \text{ m}\Omega \cdot \text{cm}^2$ combined with a breakdown voltage around 800V, corresponding to an average breakdown field close to 2 MV/cm and a $(V_b)^2/\text{Ron}$ figure of merit of 4 GW/cm², which is beyond the state-of-the-art. These results further demonstrate the potential of vertical GaN-on-Si devices for power applications.

[1] H Amano *et al.*, *Phys. Lett.*, **51**, 163001 (2018).

[2] J. Hu *et al.*, *Materials Science in Semiconductor Processing*, **121**, 092103 (2022).

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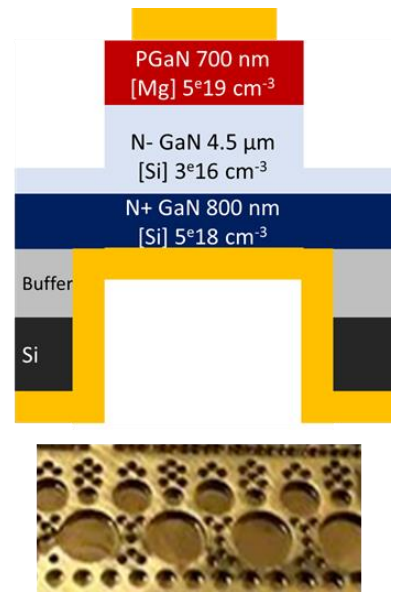


Fig. 1: Schematic cross section of the fully vertical GaN/Si PIN diodes and optical image of backside membranes

Supplementary information

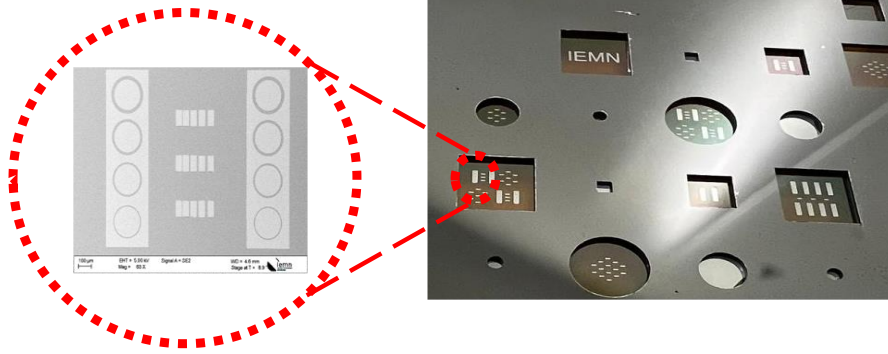


Fig. S1: SEM and optical view of TLMs achieved by laser writing within the membranes

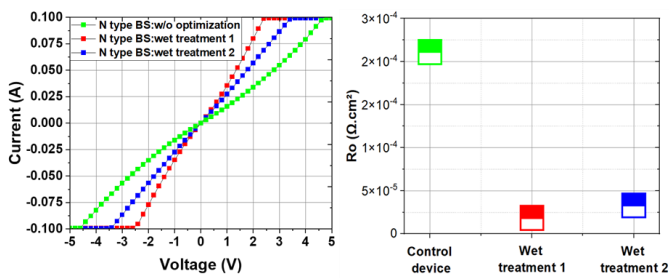


Fig. S2: IV characteristics of 10 μm TLMs on backside n+ GaN with and w/o wet treatment, and corresponding contact resistances

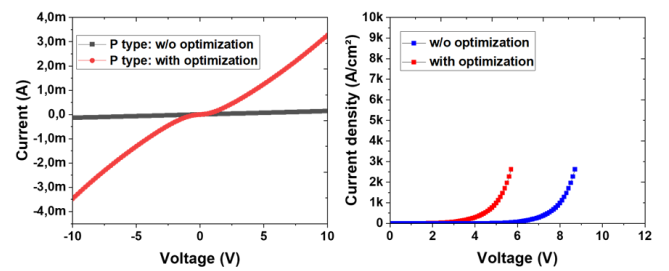


Fig. S3: IV characteristics of 10 μm TLMs on pGaN with and w/o optimization, and corresponding forward diode characteristics

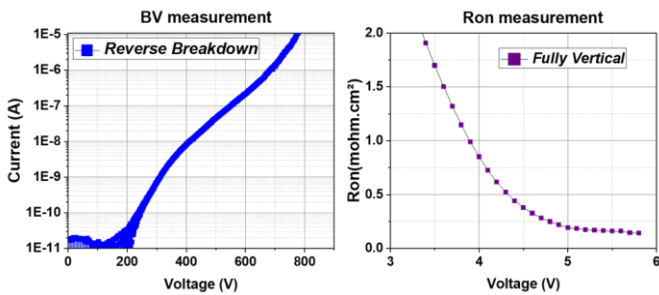


Fig. S4: Reverse and forward characteristics of the optimized fully vertical GaN-on-Si PIN diodes

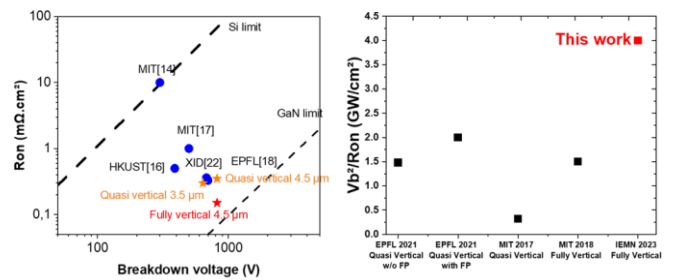


Fig. S5: Baliga Benchmark and FoM of vertical GaN-on-Si PIN diodes