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## Dislocation density reduction for vertical GaN devices on 200 mm Si

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650 V lateral GaN devices penetrate the power-switching market and replace incumbent Si technology. For devices with a 1200 V rating, vertical GaN devices on foreign substrates, such as Si and Sapphire offer significant area and cost reduction potential. With Si substrate back-etching or sapphire laser lift-off, the substrate could be separated from GaN buffer afterwards, allowing overall a higher critical electric field in the GaN layer. For vertical GaN devices, the dislocation density is a critical parameter, as certain dislocation types are electrically active.

To obtain a reduction of the dislocation density, we present engineered SiN<sub>x</sub> masking layers that limit dislocations propagation without blocking further epitaxial growth. All experiments were performed in AIXTRON planetary systems on 200 mm Si substrates. Extracted from XRD measurements, reduced dislocation density from 10<sup>8</sup> cm<sup>-2</sup> to mid-low 10<sup>7</sup> cm<sup>-2</sup> for both screw-type and edge-type after using SiN<sub>x</sub> masking layer is achieved while the uniformity of the epitaxial layers is maintained through the whole wafer area.

To assess the threading dislocation density, a new dislocation decoration technique has been applied to identify threading dislocation distribution through specific epilayer. Instead of *ex-situ* KOH etching or *in-situ* SiH<sub>4</sub>, here Cl<sub>2</sub> gas is employed for the *in-situ* threading dislocation etch process. Combined with metrology such as XRD, AFM and SEM, profound and comprehensive information about dislocation could be obtained for buffer optimization (Figure S1). On stacks with 0.5 μm drain contact and 3.5 μm low-doped drift layer (Figure S2), FWHM from rocking curves recorded at wafer center varied between 265 and 290 arcsec for the GaN <002> peak and 296 and 337 arcsec for the GaN <102> peak depending on utilization, and position(s) of the SiN<sub>x</sub> masking layer(s) (Figure S3). There is further room for improvement by SiN<sub>x</sub> optimization and drift layer scaling.

To assess the electrical performance, vertical p-n diodes were grown on 200 mm Si without and with SiN<sub>x</sub> masking layer. Device fabrication was performed including mesa isolation, ohmic p-contact formation, Si substrate removal and backside ohmic drain contact. I-V characteristics are compared between the samples.

## Supplementary information

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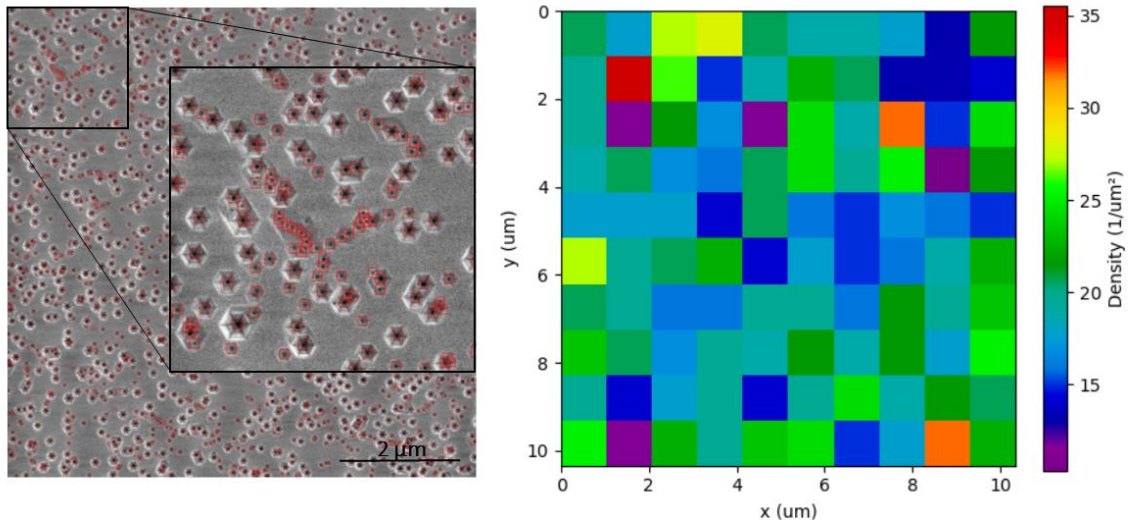


Figure S1 (Left) SEM image of GaN surface (w/o SiNx insertion) after Cl2 in-situ defects decoration, using inlens detector and reprocessed for automatic pits detection. (Right) pits count displayed as statistic mosaic chart on 1x1  $\mu\text{m}^2$  pixel.

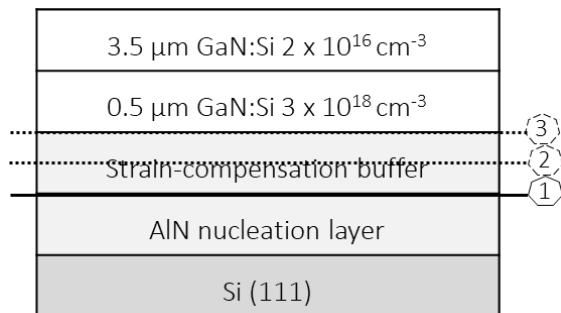


Figure S2: Stack to evaluate influence of SiNx masking layers, ①-③ indicate position of SiNx masking layer.

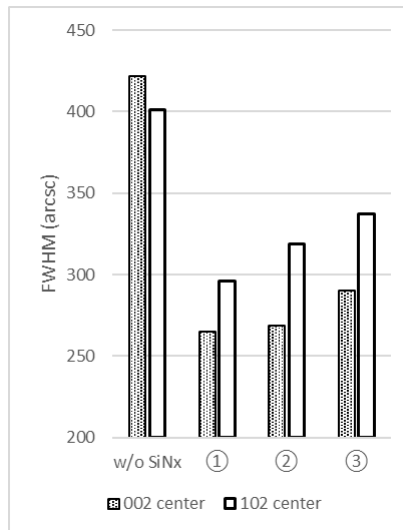


Figure S3 Comparison of wafer FWHM data among four of the experiments showing the significant potential of the method on vertical device stacks.