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Youssef Hamdaoui, Idriss Abid, Sondre Michler, Katir Ziouche, F Medjdoub. Towards High Performance Fully Vertical GaN-on-Silicon PIN Diodes. Compound semiconductor week 2023, May 2023, Jeju, South Korea. hal-04436387

HAL Id: hal-04436387

<https://hal.science/hal-04436387>

Submitted on 3 Feb 2024

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Towards High Performance Fully Vertical GaN-on-Silicon PIN Diodes

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Abstract— In this work, we demonstrate quasi and fully vertical PIN GaN on Si diodes with a low on state resistance of 0.35 mΩ.cm² and high average electric field of 1.82 MV/cm, which is favorably comparable to the state-of-the-art considering the absence of edge termination or field plates. The breakdown voltage scales well with the drift layer thickness of 3.5 μm and 4.5 μm resulting in hard breakdown values exceeding 800 V. The achieved results are promising towards kVolt-class fully vertical GaN-on-Silicon devices.

Keywords—Wide band gap semiconductor; GaN-on-Si; Vertical power devices

In the past two decades, GaN HEMTs (high electron mobility transistors) have been demonstrating its high potential to exceed the silicon power device limitations. However, GaN based lateral HEMTs suffer from several prominent issues such as electron trapping and related device reliability due to both the sharp peak electric field at the gate edge and the absence of avalanche effect. Furthermore, higher breakdown voltage requires increased gate to drain distances resulting in undesired large device size. This is why vertical GaN power devices are increasingly of interest and intense efforts from the community are currently on-going. Indeed, the high breakdown voltage, the avalanche capability, the electric field management with high current spreading and the small device footprint are some of the main advantages of vertical power devices. If grown on silicon substrate, the overall cost can be significantly reduced. In this work, we demonstrate quasi-vertical GaN-on-Si PIN diodes with high performance and linear breakdown voltage scaling with the drift layer thickness. Fully vertical PIN diodes have also been fabricated yielding similar breakdown field and potentially even lower on-resistances Ron.

Two PIN GaN diode structures have been grown on Silicon substrate with similar N⁺ bottom layer (Thickness=800 nm and doping= 5×10^{18} cm⁻³) and P top layer (Thickness=700 nm and doping= 3×10^{17} cm⁻³). The drift layers have the same doping (3×10^{16} cm⁻³) but two different thickness of 3.5 μm and 4.5 μm. The fabrication process of the PIN diodes started with mesa etching using ICP system by Cl₂/Ar. Then, a Ti/Al/Ni/Au metal stack was deposited on top to form the N⁺ contacts while Pd/Ni/Au metal stack was deposited on top of the P layer (see Fig. 1 and 2). Both P and N contacts were annealed at 600°C. High on-state current density (normalized with the anode area) and similar low differential Ron of 0.35 mΩ.cm² are observed in both cases, as expected from the N-doping level within the drift layers (see Fig. 5 and 6). Furthermore, a high breakdown voltage Vbr was achieved and a linear correlation between the drift region thickness and the breakdown voltage was observed. For 3.5 μm drift layer, Vbr is around 640 V corresponding to an average breakdown field of 1.82 MV/cm (see Fig. 7). For 4.5 μm drift layer, a Vbr around 820 V resulting in an identical breakdown field (1.82 MV/cm). These results indicate that the epitaxial and process quality can be maintained with larger drift layer thicknesses, considering that no specific edge termination or sidewall treatment was employed. It can be pointing out that these results are favorably comparable to state-of-the-art quasi vertical GaN-on-Si PIN diodes without edge termination or field plates (see Fig. 10).

Additional fully vertical PIN diodes were fabricated on the same wafers as this architecture is highly desired for proper device integration in a large scale as well as reduced Ron. The process of fully vertical PIN diodes started with the Silicon substrate thinning followed by the front side processing. The silicon substrate and buffer layers are then locally removed using DRIE and ICP tools. The N⁺ backside layer was contacted using Ti/Au metal deposition by sputtering while similar P-contacts were used on the frontside (see Fig. 3 and 4). Interestingly, the fully vertical PIN diodes showed a similar off-state behavior than the quasi-vertical ones (see Fig. 8). As can be seen in the benchmark Fig. 11, the corresponding breakdown field and associated doping concentration are promising, as the Ron of fully vertical devices should be even lower than the quasi-vertical devices since the current flow in the N⁺ layer at the edge of the mesa, which creates an additional serial resistance is suppressed. This is illustrated in the TCAD simulation Fig. 9 and will be experimentally validated once the optimization of the backside contacts will be completed.

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2. K. Fu, et al., Appl. Phys. Lett. 121, 092103 (2022)
3. Y. Zhang et al, IEEE, 39, 5 (2018)

Acknowledgments: This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement No 101007229.



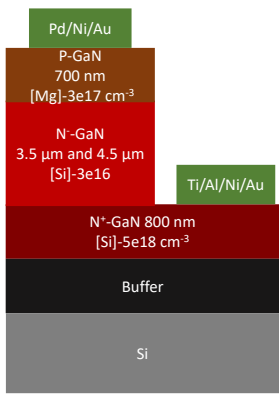


Fig.1. Schematic cross section of quasi vertical PIN diodes

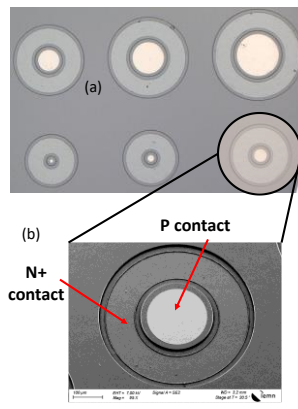


Fig.2. SEM images of quasi vertical PIN diodes

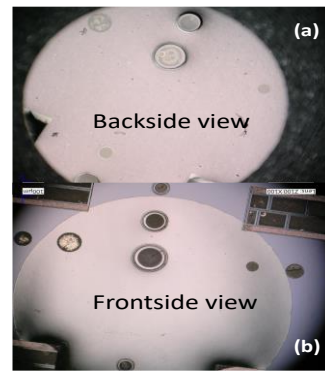


Fig.3. Backside (a) and frontside view (b) of fully vertical PIN diode with Silicon substrate and buffer layer removal

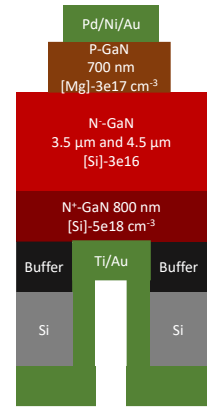


Fig.4. Schematic cross section of fully vertical PIN diodes

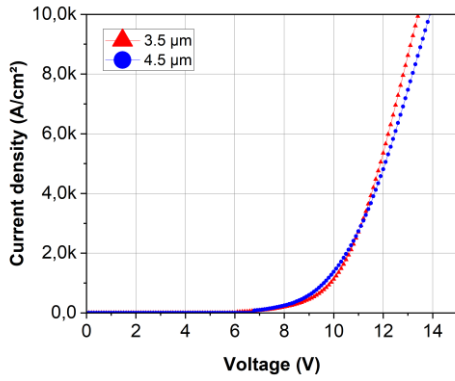


Fig.5. Forward I(V) of PIN diodes with 3.5 μm and 4.5 μm of drift layer

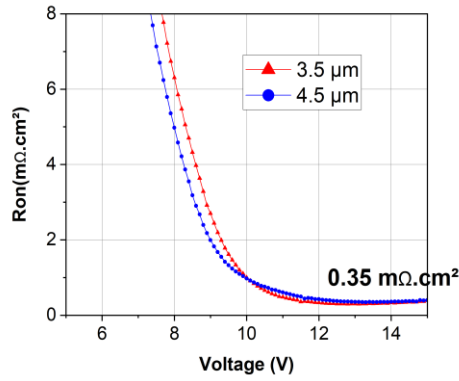


Fig.6. Differential Ron measurements of PIN diodes with 3.5 μm and 4.5 μm of drift layer

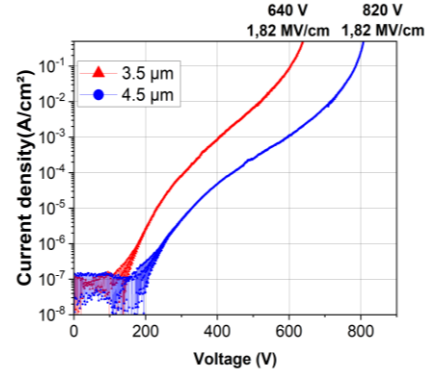


Fig.7. Breakdown voltage measurements of PIN diodes with 3.5 μm and 4.5 μm of drift layer

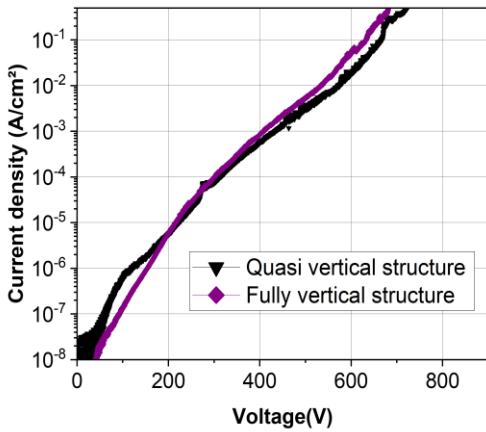


Fig.8. Comparison of PIN diodes Breakdown voltage of fully and quasi vertical architectures

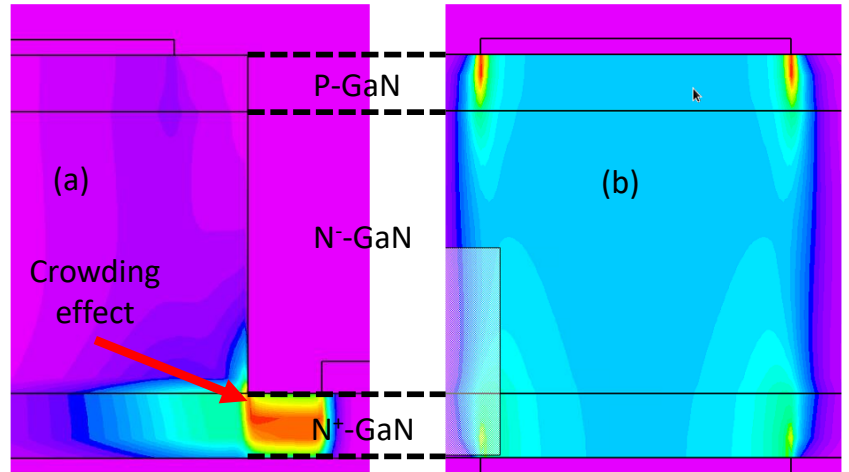


Fig.9. TCAD simulation of current density distribution of the on-state (a) quasi vertical with crowding effect and (b) fully vertical structure.

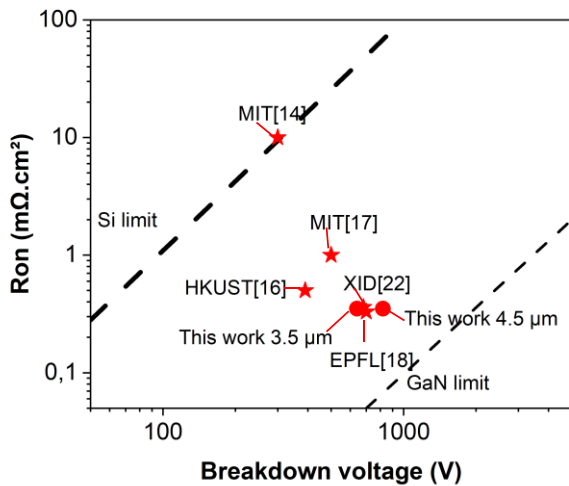


Fig.10. Benchmark of Breakdown voltage versus Ron of Quasi vertical GaN-on-Si PIN diodes without edge termination or field plate

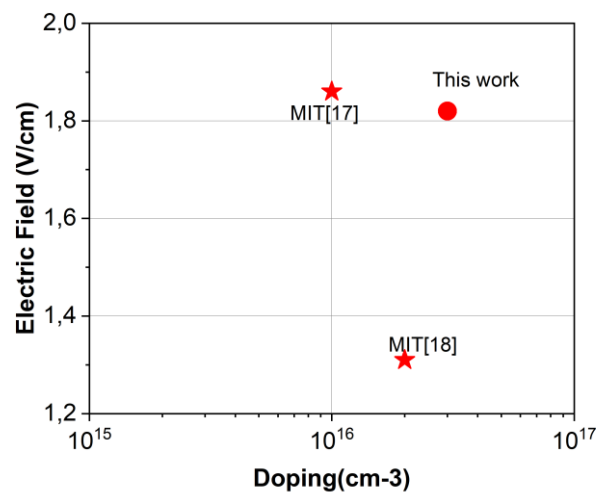


Fig.11. Benchmark of doping vs Electric field of fully vertical GaN-on-Si PIN diodes