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► **To cite this version:**

M Barbero, P Barrillon, D Fougeron, A Habib, P Pangaud. Digital cells radiation hardness study of TPSCo 65 nm CIS technology by designing a ring oscillator. Topical Workshop on Electronics for Particle Physics, Sep 2022, Bergen, Norway. pp.C02063, 10.1088/1748-0221/18/02/c02063. hal-04429169

HAL Id: hal-04429169

<https://hal.science/hal-04429169>

Submitted on 31 Jan 2024

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1 **Digital cells radiation hardness study of TPSCo**
2 **65nm CIS technology by designing a Ring Oscillator**

3 **M. Barbero^a, P. Barrillon^{a*}, D. Fougeron^a, A. Habib^a and P. Pangaud^a**

4 ^a *Centre de Physique des Particules de Marseille*

5 163, avenue de Luminy – Case 902

6 13288 Marseille cedex 09

7 France

8

9 *E-mail: barrillon@cppm.in2p3.fr

10 ABSTRACT: The CPPM group has long been designing and testing HV-CMOS blocks to complete
11 monolithic chips in various technologies (TJ180, LF150, AMS) in the framework of several
12 collaborations. In 2020, we participated in the MLR1 run in TowerJazz 65 nm technology through
13 CERN's EP-R&D WP1.2, by designing a ring oscillator test chip. Its aim is to characterize the
14 standard cells of this technology and evaluate their radiation hardness against TID. There were
15 48 ring oscillators formed of different cells with different sizes and two thresholds. In 2022,
16 characterization, temperature, Xray irradiation (up to more than 500 Mrad) tests and annealing
17 took place, leading to encouraging results presented here.

18 KEYWORDS: Ring oscillator; irradiation; TID; annealing.

19 **1. Introduction**

20 In 2020, CPPM group joined a common effort (CERN EP-R&D work package 1.2 [1]) aiming to
 21 submit blocks or test chips in TPSCo 65nm CIS technology. Our task was to design a large set of
 22 ring oscillators (see Table 1) differing from each other by the type of cells they were made of
 23 (Inverter, NAND, NOR and DFF), with variations in the transistor width (e.g: Inv0, Inv4 and
 24 Inv8, the width being larger with increased number) and threshold (Low VT and Super Low VT).
 25 In total 24 different ring oscillators were designed and duplicated to form two identical banks: the
 26 Functional (or “F”) bank which is made to oscillate during irradiation and the Static (or “S”) bank,
 27 under bias in a static state while the chip is being irradiated. The objective is to study the effect
 28 of Total Ionizing Dose (TID) on various library cells, as well as the difference in damage due to
 29 irradiation, between static logic cells and commutating logic cells.

Low VT		Super Low VT	
Size Min	Size+	Size Min	Size+
INV0_LVT	INV4_LVT	INV4_SLVT	INV8_SLVT
NOR1_LVT_A	NOR4_LVT_A	NOR4_SLVT_A	NOR8_SLVT_A
NOR1_LVT_B	NOR4_LVT_B	NOR4_SLVT_B	NOR8_SLVT_B
NAND0_LVT_A	NAND4_LVT_A	NAND4_SLVT_A	NAND4_SLVT_A
NAND0_LVT_B	NAND4_LVT_B	NAND4_SLVT_B	NAND4_SLVT_B
DFF1_LVT	DFF4_LVT	DFF1_SLVT	DFF4_SLVT

30 **Table 1.** List of the base cells forming the ring oscillators in the test chip.

31

32 Each bank is controlled by a Start/Stop signal (cf Figure 1), that puts the entire bank into
 33 oscillation mode while high. All the ring oscillator outputs are being multiplexed into the input
 34 of a single 12-bit counter at the bottom of the chip. From the outside, the tester has access to the
 35 12 bits, which can be read in DC mode to determine the number of oscillations. Each ring
 36 oscillator is composed of 101 cells forming a chain, interrupted by an AND gate, that commands
 37 the start/stop of the cell. For the cells with two inputs (NOR, NAND), two flavours
 38 (Name_cell_A&_B) have been designed and tested in order to observe the effect of the proximity
 39 of the power supply rail (cf. Figure 1). Simulations and measurements show that the B type is
 40 systematically faster than the ‘A’ type.

41

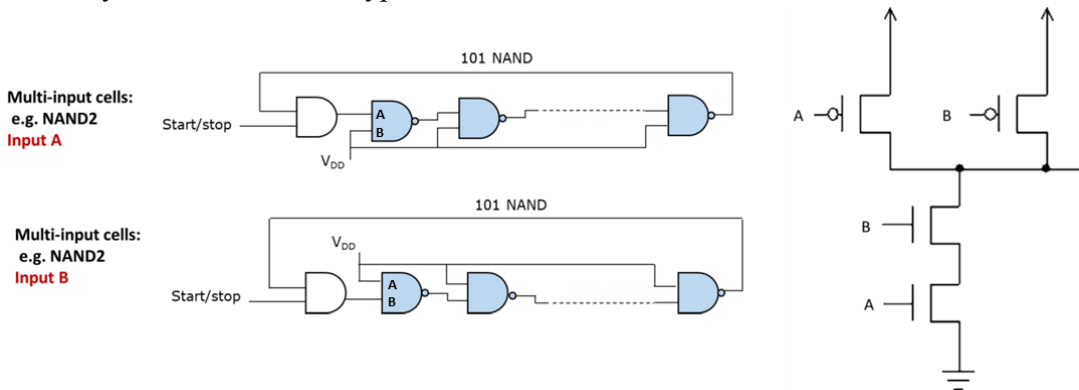


Figure 1. Ring oscillator NAND2 architecture with types A and B inputs.

42 The counter bits can also be used as frequency dividers to monitor any ring oscillator in real time.
43 The time window, where ring oscillators are enabled, is common for all parts. It is considered
44 during tests as a parameter which can be tuned until:

45
$$\text{Time_Window_max} = 4095 \times 10\text{ns}$$

46 where 4095 is the maximum value of a 12-bit internal counter and 10 ns corresponds to the period
47 of a reference clock ($f_{\text{REF}} = 100 \text{ MHz}$) of our test bench. It also corresponds to the precision of
48 our test system.

49 In practice, a third of the maximum counter value is set in order to not saturate an output of the
50 chip. The formula to obtain the corresponding frequency (in Megahertz) is as following:

51
$$f_{\text{RO}}[\text{MHz}] = \frac{\text{Mean_Counter_Value} \times 1000}{\text{Time_Window} \times 10}$$

52 where Mean_Counter_Value is a mean of x measured frequency values (x=10 typically).

53 The chip, powered with 1.2V, has dimensions of 1.5 mm x 1.5 mm, and a total of 48 pads. It was
54 tested on a board developed at CPPM. After initial demonstration of basic functioning, two main
55 test campaigns were carried out with temperature tests and irradiation tests (TID) followed by an
56 annealing study at different periods. The test set-up and the facilities used for these tests are
57 described in the next section.

58 2. Test set-up and facilities

59 The core elements of the test set-up are a board, with the test chip is bonded on it (see Figure
60 2 - left), connected to a Beaglebone DAQ system (Linux Os embedded). For the communication,
61 each sequence is described in VHDL inside an FPGA and launched thanks to a C++ script. Data
62 recorded are analyzed with python programs.



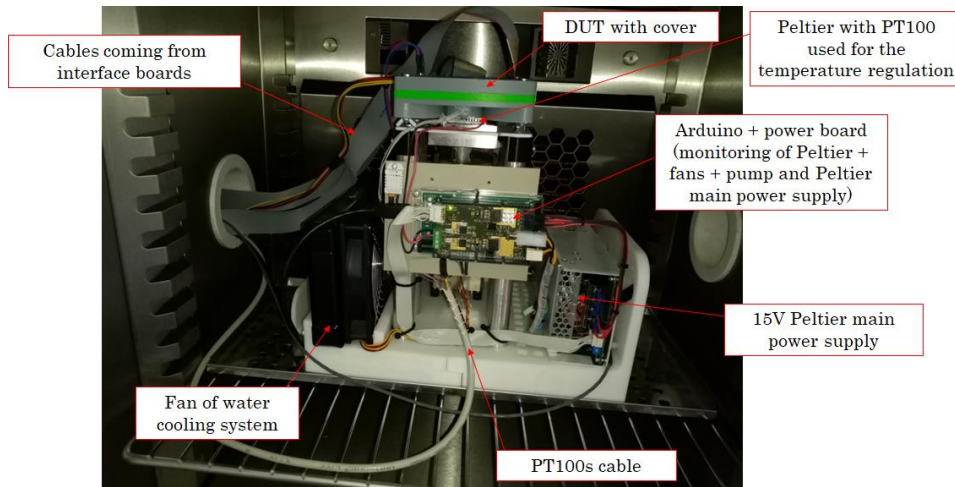
63 **Figure 2.** Left: DUT board with the chip bonded. Right: irradiation tests set-up.

64 This set-up was used for the tests as a function of temperature, the tests under irradiation and
65 then under several annealing phases. During the irradiation tests, we benefited from an X-ray
66 machine (cf Figure 2 – right) that was delivering a dose rate of 20 kRad/mn (calibration performed
67 with an AXUVH5 photo-diode + 150 μm thick Al filter before each campaign). The temperature
68 of the room was regulated at 25°C with a portable air conditioner.

69 Concerning the temperature tests, the DUT board was installed inside a climate chamber whose
70 temperature was regulated (at 20 and 40°C) and dry air supplied to avoid any condensation at low
71 temperature. A Peltier system (cf Figure 3) has been used in combination to the climate chamber

72 to regulate the temperature of the chip from -40 to 30°C . The same climate chamber was used for
 73 the annealing period carried out at 80°C .

74



75

Figure 3. Set-up inside the climate chamber for the temperature tests.

76 3. Temperature tests

77 The measurements of the frequency of each ring oscillator were carried out from -40°C up to
 78 30°C (with steps of 10°C) with V_{dd} set at 0.9, 1.0, 1.1, 1.2 (nominal) and 1.3V. For each couple
 79 (Temperature, V_{dd}), 10 measurements were taken for all ring oscillators. Each one exhibits a
 80 decrease of the frequency while the temperature increases (5-10 % over 70°C) whatever the V_{dd}
 81 or the bank. The figure 4 gives the results for 8 ring oscillators of the bank S as an example.
 82 Simulations performed for temperatures in the range $[-30, 30]^{\circ}\text{C}$ showed a similar trend.

83

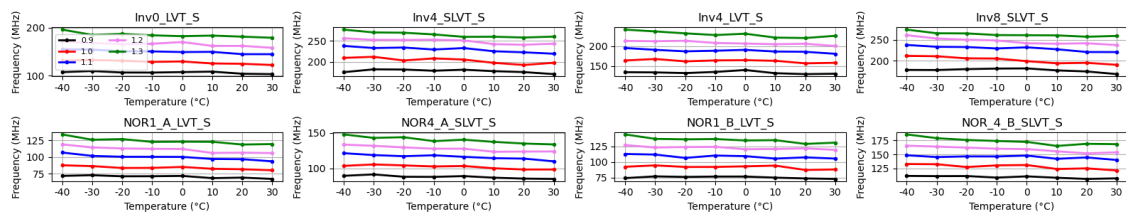


Figure 4. Frequency (in MHz) vs temperature (in $^{\circ}\text{C}$) for different V_{dd} for a sample of 8 ring oscillators of the bank S.

84 4. Irradiation tests

85 In 2022, two chips were irradiated, at ambient temperature with an X-ray machine, up to 830
 86 and 520 Mrad respectively. During the exposure time, the ring oscillators from the functional
 87 bank were kept oscillating while the ones from the static bank were not. Regular measurements
 88 of the frequencies, with both banks put in oscillating mode, were performed along the irradiation
 89 periods.

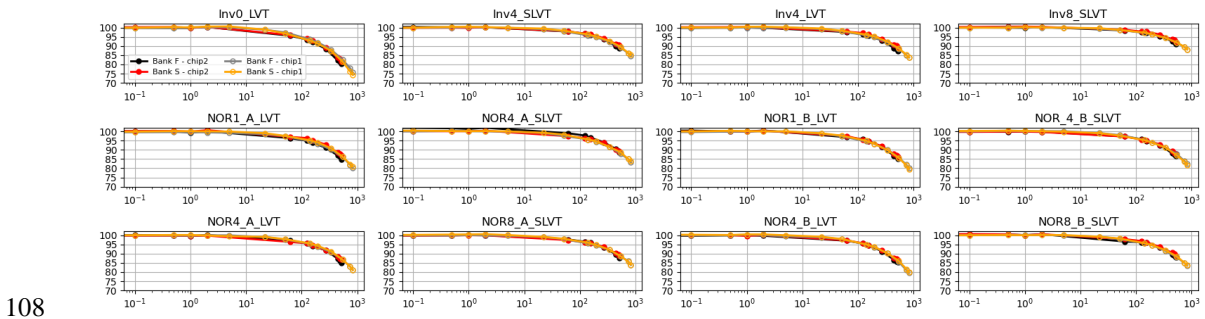
90 During the first period (spring, chip 1) the temperature was stable around 25°C in the
 91 chamber, while during the second one (summer, chip 2) we suffered from warm temperature that
 92 affected the X-ray tube cooling system and we had to stop at a lower TID (520 Mrad).
 93 Nevertheless, both chips responded similarly to the irradiation and exhibited a decrease (up to
 94 25%) of the frequencies. We observed differences between ring oscillators, depending on the type,

95 length, and threshold of the transistors of the base cells. The output frequency of each ring
 96 oscillator follows a relation depending on the number of cells (101 in our case) and the
 97 propagation delay (Tp):

$$98 \quad f_{RO} = \frac{1}{2 \times \text{Nb Cells} \times T_p}$$

99 Thus, the values of frequency we measured correspond to a propagation time of few ten
 100 picoseconds for each cell. If we assume that the beam is homogeneous on the whole chip, the
 101 delay degradation is distributed on each cell. The shift of the frequency we measured is directly
 102 related to the I_{ON} of the transistors which also depends on the threshold, the transconductance and
 103 finally on its geometry. Then, to know which type of transistor (N or PMOS) is more sensitive to
 104 irradiation, this study must be correlated with the irradiation of single transistors in order to
 105 understand well the observed behavior.

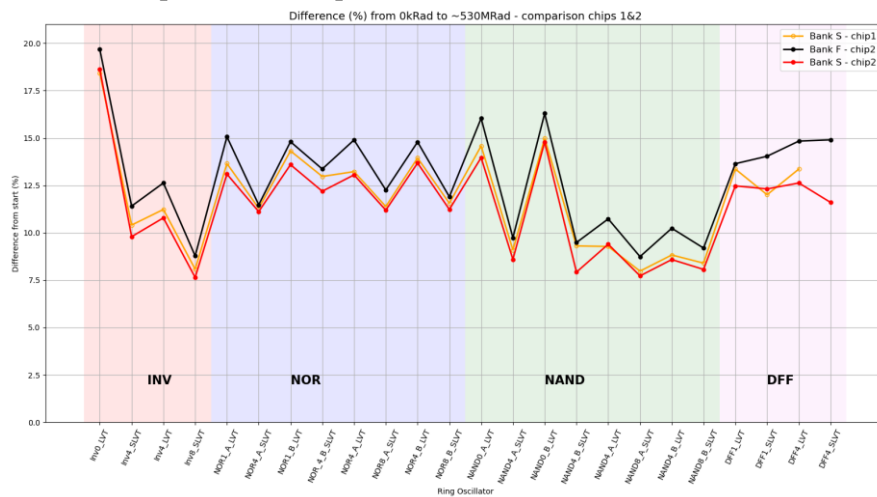
106 The figure 5 represents, for 12 ring oscillators (as an example), the evolution of the relative
 107 frequency as a function of the TID for both chips and banks.



108

Figure 5. Relative frequency vs TID (log scale) for 12 ring oscillators, both chips and banks.

109 It is worth noticing that the functional bank of the chip 1 was incorrectly configured during
 110 the irradiation and therefore was also kept static. This resulted in measurements similar for the
 111 two banks of this chip. For chip 2, the two banks were configured properly and differences of a
 112 few % between static and functional banks were observed. This difference is illustrated by the
 113 figure 6 which gives the relative frequency difference (before irradiation – after ~500 MRad) for
 114 each ring oscillator (chip1, bank S, chip2 banks F & S).



115

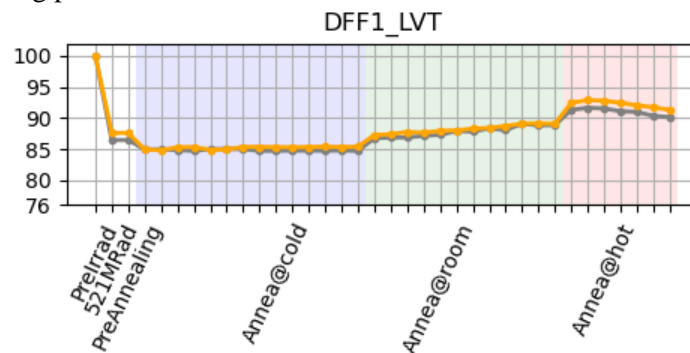
Figure 6. Relative frequency difference (before-after approximately 500Mrad TID) for each ring oscillator (chip1, bank S, chip2 banks F & S).

116 5. Annealing

117 After irradiation, the chips went for annealing periods at three different temperatures, successively
118 -20, 25 and 80 °C, following a procedure described in a document from the ESA [2]. The duration
119 of each period was adjusted from a week to several weeks. Using the data from the temperature
120 tests, we applied a correction (linear rescaling) to take into account the temperature difference of
121 the three annealing periods. This correction is not ideal since the frequencies were not measured
122 up to 80°C before irradiation but allows us to have a better overall view of the annealing.

123 For all the ring oscillators, we observed no recovery at cold temperature (-20°C), a small recovery
124 (few %) at room (25°C) and what looks to be a reverse annealing at warm temperature (80°C).

125 The figure 7 gives an example of the relative frequency before irradiation, after irradiation and
126 during each annealing period.



127

Figure 7. Relative frequency before irradiation, after 521 Mrad and for the three annealing periods.

128 6. Conclusions

129 The study of radiation hardness of TPSCo 65nm (TJ65) technology based on ring oscillators
130 measurements showed relevant results. The frequencies decreased for all types of ring oscillators
131 exhibiting different impact of the TID (from 12 to 25% at 830 Mrad). The size of the cells is an
132 important parameter, the smaller cells (e.g Inv0) being more affected than the bigger ones (e.g
133 Inv8), in agreement with similar tests performed for other technologies [3]. This limited
134 degradation opens perspective for the usage of digital cells of this technology in high radiation
135 environments. The temperature has an impact (decrease of the frequencies with increasing
136 temperature) that can be quantified and partially corrected with a simple linear rescaling approach.
137 Finally, the annealing period at high temperature (80°C) can be interpreted like a reverse
138 annealing behavior and must be considered for the future developments in this technology.

139 References

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