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# Pulse Current Characterization of SiC GTO Thyristors with Etched JTE

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**Abstract.** In this paper we highlight our latest results on high voltage SiC thyristors comprising an etched JTE. Compared to our previous design concepts, the thyristors described here are larger in size and have been investigated regarding pulsed power applications. Quasi-static on-state characteristics show that the devices withstand a repetitive current load of up to 16 A corresponding to a current density of 825 A/cm<sup>2</sup>. Their switching behavior was evaluated up to 1000 V demonstrating characteristic waveforms at turn-on and gate turn-off. Moreover, pulsed current characteristics show that the typical device under test sustained a current pulse of 20 μs with a peak value of 200 A and 10 kA/cm<sup>2</sup>, respectively.

## Introduction

At present, power switches based on SiC are on their way into the market. Thyristors are among them [1], however, the commercial ones are not optimized specifically for pulsed power purposes. Otherwise, progress has been achieved in tailoring the structure of the thyristor termination in order to avoid electrical field crowding at the device edges [2]. In this context, we have employed an advanced etched junction termination extension (JTE) featuring a multiple-step layout [3,4, and refs. therein]. In principle, this kind of termination allows for a protection efficiency of 96% accompanied by a very low leakage current level until the onset of the avalanche breakdown. Following this kind of termination, we recently completely overhauled the entire design of our first-generation thyristors [5], particularly allowing for large-area contact pads. First results based on this design concept have been published elsewhere [6]. Here, we report on thyristors which are larger in size and aimed at pulsed power applications.

## Device Design and Fabrication

**Structure and Layout.** The source material of our devices is an 8° off-axis n-type 4H-SiC wafer from SiCrystal AG. The epilayer structure was grown at Acreo AB according to the target specifications given in Fig. 1. The stacking sequence of n<sup>+</sup>(substrate)/n (buffer)/p/p<sup>-</sup>/n/p<sup>+</sup> is typical for SiC GTO thyristors. It is an asymmetrically blocking structure with an ideal forward breakdown voltage of 13.7 kV as determined by one-dimensional finite-element simulations.

The devices are terminated by our so-called graded etched (GE) JTE, conceptual details of which can be found elsewhere [3,4]. As for the thyristors presented here, the JTE consists of two steps, having a length of 250 μm and 50 μm (*cf.* Fig. 1). The remaining n-base height underneath these two steps is 800 nm and 600 nm, respectively. Initially, it was intended to add more steps, however, electrical inspection measurements performed after each etching step in a vacuum probing chamber indicated that the two-step JTE structure was sufficient to attain a reasonable blocking capability of the device structure on target. In fact, all thyristors originating from the concerned wafer batch revealed a breakdown voltage limited to 4.5 kV, remaining unchanged even at high temperature. As

signaled by depth profiling analysis using secondary ion mass spectroscopy (SIMS) the buffer layer suffers from an unexpected low doping concentration. As a consequence, this suggests that the premature breakdown is driven rather by a punch-through effect within the buffer layer than by an avalanche-like behavior of carriers in the drift layer.

The active area of the devices presented here is  $1.96 \text{ mm}^2$ . With a total JTE length of  $300 \text{ }\mu\text{m}$  and a safety margin to the cutting edge, the total die surface attains  $2.7 \times 2.7 \text{ mm}^2$ . The layout resembles that of a GTO thyristor with interdigitated gate and anode stripes. The structure counts 15 anode stripes,  $1.2 \text{ mm}$  long and  $60 \text{ }\mu\text{m}$  wide, which are separated by  $30 \text{ }\mu\text{m}$  wide gate trenches. Isolated by a thick  $\text{SiO}_2$  layer, the contact stripes of gate and anode are interconnected on a second metallization level, thus forming large area contact pads. This surface-optimized gate design, enabling a large number of bonding wires to be connected, is one feature which is distinctly different from our first-generation thyristors [5].

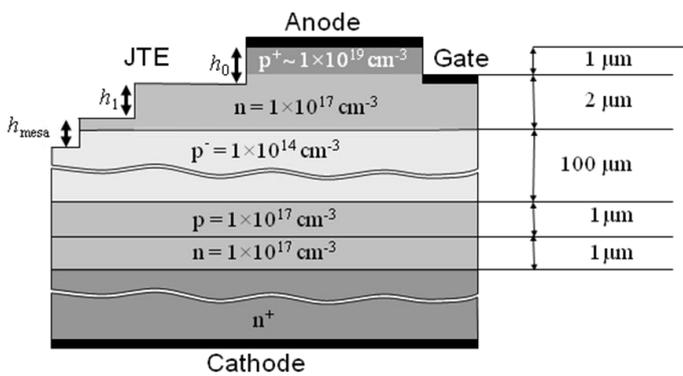


Fig. 1: Schematic cross-section of the employed thyristor structure with an etched JTE ( $h_0 = 2.2 \text{ }\mu\text{m}$ ,  $h_1 = 0.2 \text{ }\mu\text{m}$ ,  $h_{\text{mesa}} = 1.7 \text{ }\mu\text{m}$ ).

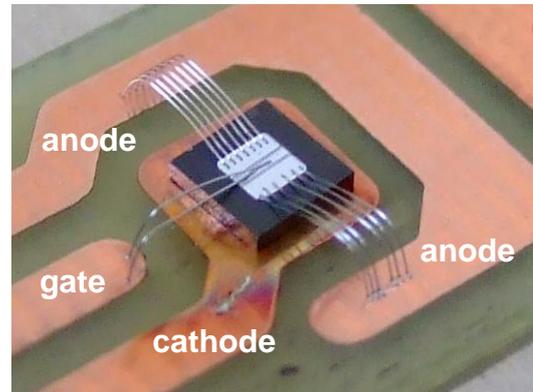


Fig. 2: Viewgraph of a  $2.7 \times 2.7 \text{ mm}^2$  SiC GTO thyristor die with large area contact regions.

**Processing.** For reasons of material costs and in order to vary processing parameters, as for instance the number and height of the termination steps, the wafer has been cut in advance into samples measuring  $10 \text{ mm}$  by  $10 \text{ mm}$ . The fabrication process is based on a mask set with ten levels, including three levels for realizing a JTE within three steps: First, the anode/gate structure and the termination steps were etched using reactive ion etching (RIE). For etching the anode, a nickel mask has been used aiming at steep edges precisely bordering the gate fingers. For the termination steps, a resist mask was employed. In all cases, the etching was performed in a gas flow of  $\text{SF}_6$  and  $\text{O}_2$ , thus resulting in an average removal rate of  $145 \text{ nm/min}$ .

Following the RIE and an extensive cleaning procedure, the primary metallization has been realized directly on the interdigitated structure of anode and gate. The primary metallization consists of nickel on the gate as well as the cathode and of a Ti/Ni/Al trilayer on the anode. All metal layers were annealed in a RTP reactor. Gate and anode fingers were subsequently covered by a  $1 \text{ }\mu\text{m}$  thick Al layer. Then a  $\text{SiO}_2$  passivation layer was deposited using PECVD. Opening windows were etched to interconnect the primary metallization with three contact pads formed on top of the device structure (see Fig. 2). This second metallization level consists of a  $3 \text{ }\mu\text{m}$  thick Al layer.

**Packaging.** The dies are solder attached to a PCB type of support having the foot print of a TO 254 housing. As can be seen in Fig. 2, the connection to the outer periphery has been realized by means of numerous Al bonding wires, each  $50 \text{ }\mu\text{m}$  in diameter. Devices tested at elevated voltages are additionally isolated by a translucent silicone gel.

## Electrical Characterization

**On-state.** The on-state characteristic of the device under test as obtained using a curve tracer is illustrated in Fig. 3. It turned out that the gate current must exceed 20 mA in order to switch the device on. Moreover, the device withstands a repetitive current load of up to 16 A corresponding to a current density of  $825 \text{ A/cm}^2$  which demonstrates its ruggedness and current handling capabilities. The on-state voltage drop reaches 6 V at  $100 \text{ A/cm}^2$  which is quite high even for a device with a  $100 \mu\text{m}$  thick drift layer. It can be attributed to some processing failure during the formation of the primary metallization, resulting in a relatively high contact resistance.

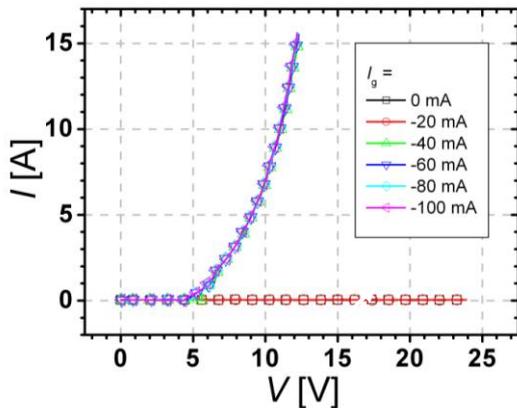


Fig. 3: On-state characteristic of a SiC GTO thyristor measured using a curve tracer.

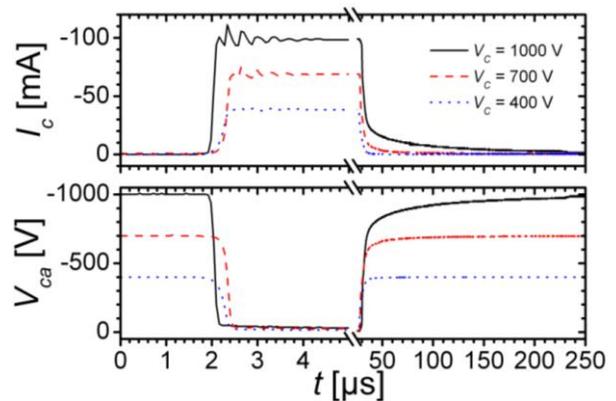


Fig. 4: Switching waveforms of a SiC thyristor at turn-on and gate turn-off.

**Switching.** Fig. 4 depicts the switching behavior of a SiC thyristor at turn-on and gate turn-off. The device under test has been switched up to a cathode-anode voltage of  $V_{ca} = 1000 \text{ V}$ , the present limit of the used test bench. For these tests, the cathode current  $I_c$  was limited by a resistance of  $10 \text{ k}\Omega$ . To turn the thyristor on, a triangular gate current pulse with a peak current of  $-100 \text{ mA}$  and a width of  $10 \mu\text{s}$  was applied. The onset of  $I_c$  observed at about  $t = 20 \mu\text{s}$  (Fig. 4) occurs when the gate current surpasses a threshold of  $20 \text{ mA}$ . After that, the cathode current steeply rises. For the highest voltage ( $V_C = 1 \text{ kV}$ ), the turn-on time amounts to  $120 \text{ ns}$ .

While the turn-on is uncritical, the gate turn-off posed some problems at higher voltages. For the lowest voltage ( $V_C = 400 \text{ V}$ ), the thyristors could be turned off with a  $20 \mu\text{s}$  gate current pulse, similar to turn-on but with a positive amplitude ( $+100 \text{ mA}$ ). However, to ensure a safe turn-off at voltages of  $700 \text{ V}$  and  $1 \text{ kV}$ , the gate current needed to be maintained for  $30 \mu\text{s}$  or even  $200 \mu\text{s}$ , respectively. As shown in Fig. 4, this recovery time is reflected by a considerable current tail.

**Pulse Characterization.** In order to evaluate the capabilities of the developed SiC thyristors for pulsed power applications [7], they were tested in a capacitive discharge circuit. Fig. 5 is showing the last current pulse in a series of discharge tests with successively increasing peak current. In this way, several thyristors have been tested up to their performance limit. The typical device under test sustained a current pulse of  $20 \mu\text{s}$  with a peak value of  $200 \text{ A}$  and  $10 \text{ kA/cm}^2$ , respectively. After the series of current pulses the device was still functioning but, as shown in Fig. 6, degradation of the thyristor blocking capability hindered further enhancement of the capacitor charging voltage. It is important to note that these performance tests have not been limited by any bonding wire failure which applied to our first-generation thyristors [5]. The wire bonding appears to be quite reliable and should permit evaluating our devices up to much higher peak currents.

## Conclusion

Here, for the first time, we present pulse current characteristics of our new generation of devices comprising an etched JTE. Thanks to their new gate/anode layout the devices could be reliably

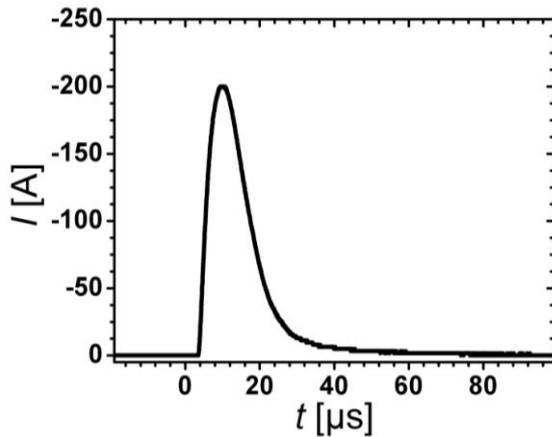


Fig. 5: Pulse current characteristic of a  $2.7 \times 2.7 \text{ mm}^2$  SiC thyristor.

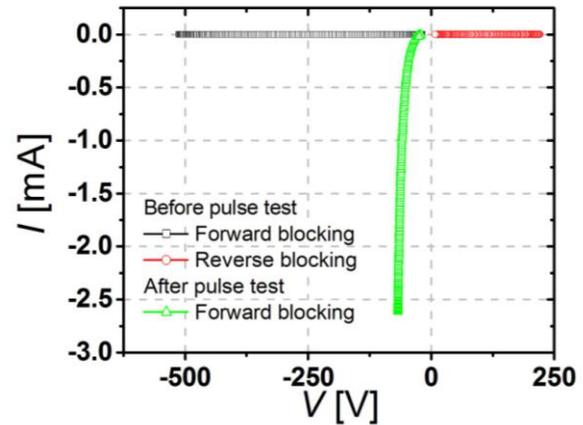


Fig. 6: Blocking characteristics of a SiC thyristor before and after pulse testing.

connected with a large number of bonding wires and thus be tested up to their intrinsic limits. Just like other early-stage SiC thyristors [8,9] the presented devices suffer from a degradation of the blocking characteristics. Although no particular optical inspection has been made yet, the cause of failure is likely due to local overheating and damage to the passivation layer. On the other hand, a degradation of the on-state characteristic is not observed referring to the pulse stress series performed. So far, these results are of preliminary nature and a comprehensive analysis is necessary to draw final conclusions about our SiC thyristors. In particular, it is necessary to study the evolution of the degradation step-by-step looking at both the static on-state and blocking characteristics.

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