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## Investigation of fully integrated power stage for piezoelectric DC-DC converters

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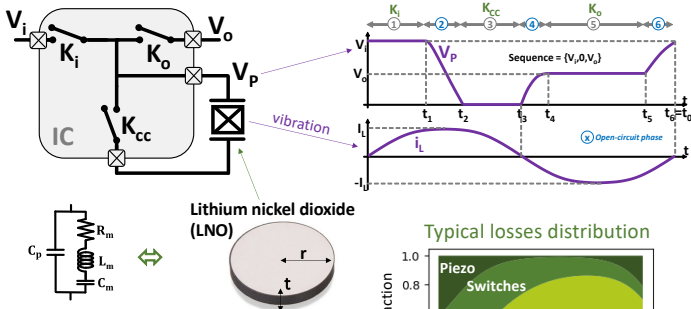
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**Abstract** – This work explores the potential of piezoelectric DC-DC converters as a viable alternative to inductive-based converters. Their exceptional frequency-scale property and planar shape make them highly promising. However, for seamless integration, it is crucial to incorporate the power stage into a single chip. By utilizing the most favorable piezoelectric material, namely LNO in thickness vibration mode, this study examines the achievable performance metrics such as efficiency, power density, and silicon surface area using a fully integrated power stage within a classical BCD technology.

## PIEZOELECTRIC DC-DC CONVERTERS

**Pro:** scaling properties compared to magnetics, planar, soft-switching

**Cons:** switches carry reactive power and block high-voltages  
Discrete demonstrations but no PMIC yet



Piezoelectric Resonator (PR)

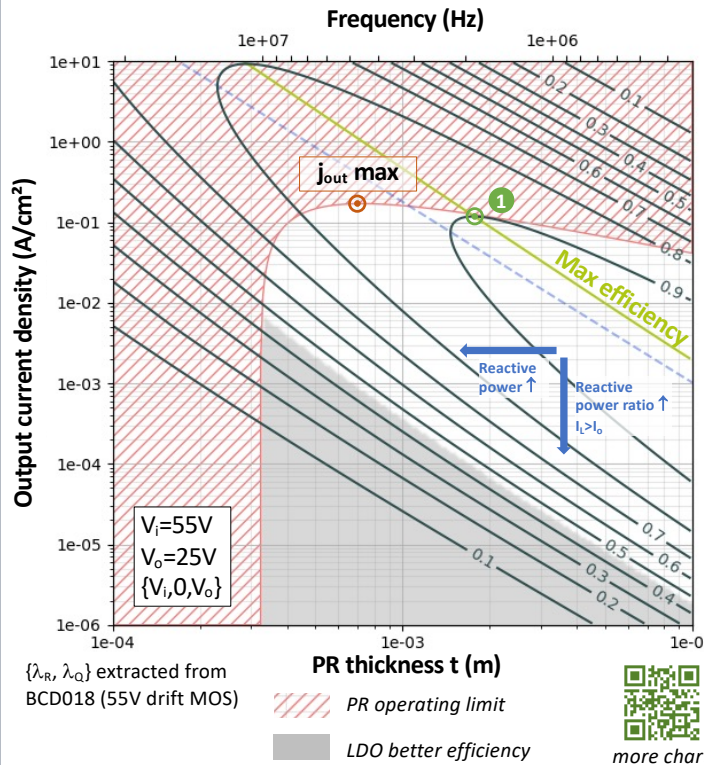
Vibration mode: **Thickness**

Thickness sets the frequency range

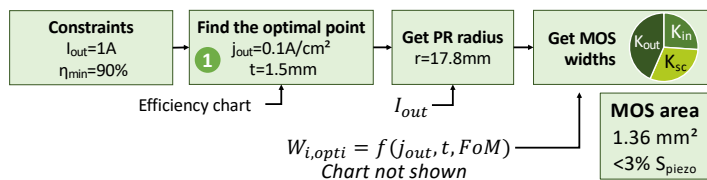
Power is limited by the surface area ( $\pi r^2$ )

What if the power stage is integrated?

## 1 EFFICIENCY CHART FOR A GIVEN SI TECHNO



Sizing Methodology with example (denormalization)



## FRAMEWORK

Loss mechanism and normalized optimization approach

$$P_{loss} = R_m(t)I_L^2 + \sum_{SW} \frac{\lambda_R}{W_i} I_i^2 + \lambda_Q W_i F(t) V_G \quad j_{out} = \frac{I_{out}}{S_{piezo}}$$

Piezo loss      Conduction loss      Driving loss      Chart independent on radius

- Find the optimal efficiency and current density for a given input voltage, Silicon technology and piezo material  
→ optimize  $\{t, W_i\}$
- Find the switch requirement to reach an efficiency target for a given VCR  
→ Find the maximal  $(\lambda_R \lambda_Q \lambda_{V_G})^{-1}$  switch FoM

Assumptions

Switching frequency:  $f \propto t^{-1}$

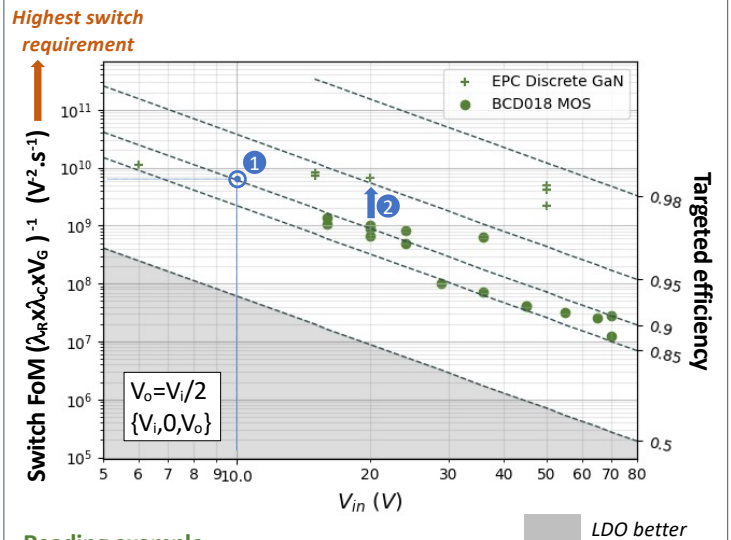
Max PR current density scaling law:  $j_{L,max} \propto f^{0.7}$

BVD model scaling law [3] with LNO:  $R_m \propto t^2$

Switch Parameters

$\lambda_R$	On-state res. per width
$\lambda_Q$	Gate charge per width
$W_i$	Channel width
$V_G$	Gate voltage

## 2 SWITCH REQUIREMENT FOR GIVEN EFFICIENCY



Reading example

- To achieve 90% efficiency at  $j_o$  max,  $FoM_{SW} > 3 \times 10^{10} V^2 \cdot s^{-1}$
- GaN reduces the losses by factor of 2, compared to BCD

Current Si technology limits the achievable efficiency (<90%)  
GaN is preferred to fully exploit the piezo DC-DC potential

## CONCLUSION

- Even if the converter has soft-switching operations and the piezo has high quality factor, the driving loss and conduction loss are still presented.
  - As other resonant converter type, the conduction loss is magnified due to reactive current ( $I_L > I_O$ ).
  - Piezo DC-DC requires high-quality switches (low specific resistance and low gate charge) not to be the limited factor.
- Perspectives:
- Open-source code available soon
  - PMIC allows easier phases control in VHF, one of the main challenge