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Investigation of fully integrated power stage for piezoelectric DC-DC converters

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Abstract – This work explores the potential of piezoelectric DC-DC converters as a viable alternative to inductive-based converters. Their exceptional frequency-scale property and planar shape make them highly promising. However, for seamless integration, it is crucial to incorporate the power stage into a single chip. By utilizing the most favorable piezoelectric material, namely LNO in thickness vibration mode, this study examines the achievable performance metrics such as efficiency, power density, and silicon surface area using a fully integrated power stage within a classical BCD technology.

PIEZOELECTRIC DC-DC CONVERTERS

Pro: scaling properties compared to magnetics, planar, soft-switching
Cons: switches carry reactive power and block high-voltages
Discrete demonstrations but no PMIC yet

Piezoelectric Resonator (PR)
Vibration mode: **Thickness**
Thickness sets the frequency range
Power is limited by the surface area (πr^2)

Lithium nickel dioxide (LNO)

Typical losses distribution

Input power fraction vs Output power

What if the power stage is integrated?

FRAMEWORK

Loss mechanism and normalized optimization approach

$$P_{loss} = R_m(t)I_L^2 + \sum_{SW} \frac{\lambda_R}{W_i} I_i^2 + \lambda_Q W_i F(t) V_G$$

Piezo loss Conduction loss Driving loss

$$j_{out} = \frac{I_{out}}{S_{piezo}}$$

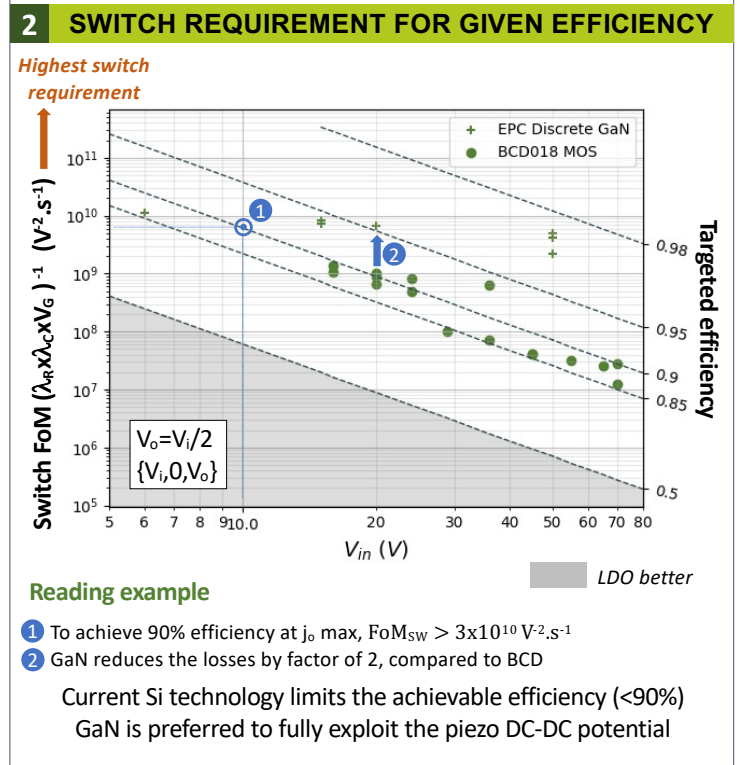
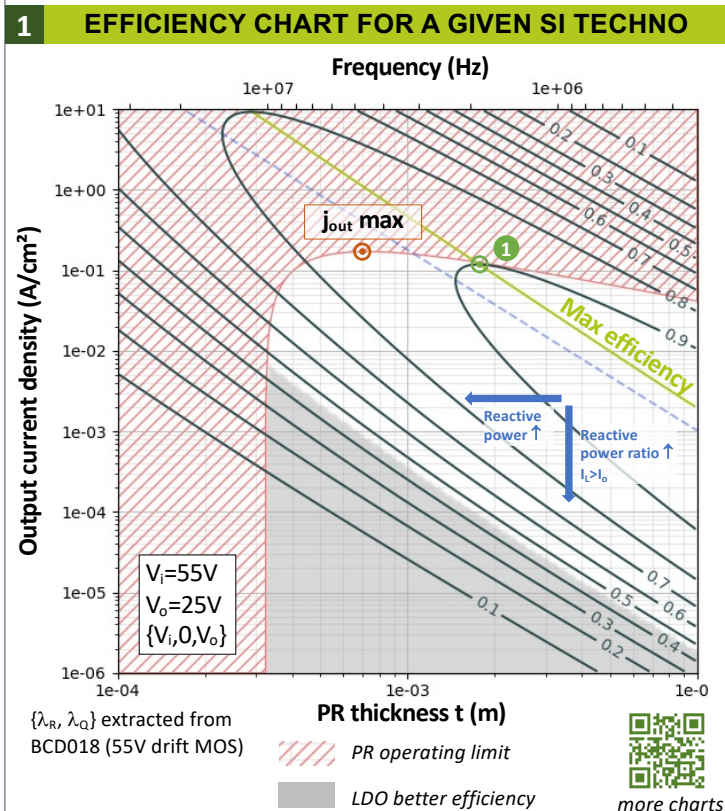
Chart independent on radius

- Find the optimal efficiency and current density for a given input voltage, Silicon technology and piezo material
→ optimize $\{t, W_i\}$
- Find the switch requirement to reach an efficiency target for a given VCR
→ Find the maximal $(\lambda_R \lambda_Q \lambda_{cQ} V_G)^{-1}$ switch FoM

Assumptions
Switching frequency: $f \propto t^{-1}$
Max PR current density scaling law: $j_{L,max} \propto f^{0.7}$
BVD model scaling law [3] with LNO: $R_m \propto t^2$

Switch Parameters

λ_R	On-state res. per width
λ_Q	Gate charge per width
W_i	Channel width
V_G	Gate voltage



Sizing Methodology with example (denormalization)

Constraints: $I_{out}=1A$, $\eta_{min}=90\%$

Find the optimal point: $j_{out}=0.1A/cm^2$, $t=1.5mm$

Get PR radius: $r=17.8mm$

Get MOS widths: K_{out}, K_{in}, K_{sc}

MOS area: $1.36 mm^2$, $<3\% S_{piezo}$

$W_{i,opti} = f(j_{out}, t, FoM)$
Chart not shown

CONCLUSION

- Even if the converter has soft-switching operations and the piezo has high quality factor, the driving loss and conduction loss are still presented.
- As other resonant converter type, the conduction loss is magnified due to reactive current ($I_L > I_o$).
- Piezo DC-DC requires high-quality switches (low specific resistance and low gate charge) not to be the limited factor.

Perspectives:

- Open-source code available soon
- PMIC allows easier phases control in VHF, one of the main challenge