Backside cavities for thermal tuning optimization of silicon ring resonators

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Thermal optimization of silicon microring resonators with backside cavity etching

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Abstract—Silicon ring resonators on SOI substrates are well known and widely studied. They are commonly used in datacom and high-performance computing for wavelength multiplexing and spectral filters. They can be tuned to the desired frequency with resistive heaters, which is the primary power budget of the device. In this work, the impact of backside cavities etched in the bulk silicon of SOI substrates below ring resonators is studied. Simulations show that those backside cavities improve significantly heat confinement and minimizes heat losses usually due to conduction in the Si substrate. Backside cavities have been successfully etched in the bulk of the SOI substrate to improve heat trapping within the silicon rings. The etching process is compatible with the standard silicon photonics interposer process flow.

Power consumption studies have been performed with a reference ring resonator on SOI and ring resonators with different backside cavity diameters. These results will be discussed with respect to the backside cavity opening. A 72% power consumption reduction for a 10 µm diameter ring resonator on SOI has been achieved with a backside opening of 100 µm deep and 40µm diameter. The cavities opening did not impact the optical ring performances.

***Index Terms*—Silicon photonics, Three-dimensional integrated circuits, Optical resonators, Thermal management**

I. Introduction

Silicon photonics propose an interesting path for increasing bandwidths for high speed communications in datacenter and high-performance computing applications. This technology can leverage the technical know-how of traditional CMOS foundries to make performant and reliable systems. A common optical solution in the field of silicon photonics is to use wavelength multiplexing to increase bandwidths of transceivers and optical networks on chips (ONoC) communication. In this framework, multiple wavelengths of infrared light are injected in a single waveguide. The multiple wavelengths are then demultiplexed at the point of use, thanks to a spectral filter, such as a ring resonator (RR).

An accurate tuning of RR is needed to grant data transmission. This tuning is generally performed using thermo-optic effect in silicon, which links a change in refractive index of the silicon with temperature. In the case of silicon, this value is:

$$dn/dT = 1.8.10^{-4}\ K^{-1}$$

The change in refractive index caused by heating also affects the effective index, and finally the resonant wavelength of the ring lres, expressed as:

L_res = pi*d/lambda*m

Where m is an integer.

In order to heat the RR, resistors within the silicon layer can be placed at the vicinity of the ring [1], or by using a metal film above the ring. Throughout this paper, the rings are designed with a radius of 10 µm.

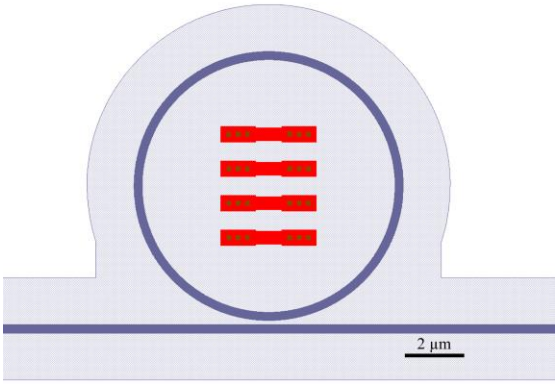


Figure 1: Scheamtic view of the ring resonator (purple) and the silicon heaters (red)

We define the "tuning power" as follows:

$$\eta = \delta P / \delta\lambda$$

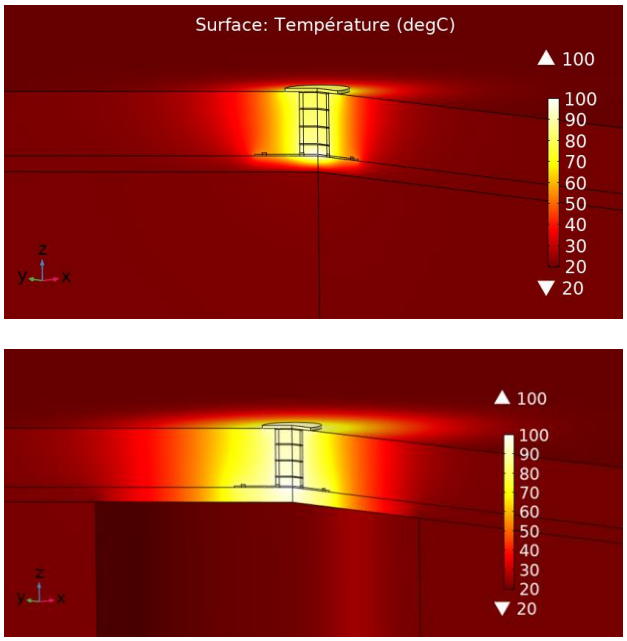
The tuning power η represents the power needed δP to shift the resonant wavelength by δλ and will be expressed in mW/nm throughout this study. The smaller this quantity, the better as it represents a larger wavelength shift for the same amount of power.

As introduced in [2], the thermal tuning consumes half of the

total power of the whole transceiver system. This work aims to reduce this thermal tuning power consumption by isolating the silicon ring resonator to lower heat loss due to conduction in the bulk Si of SOI substrates. In this letter, simulations are first conducted to evaluate the impact of backside cavities on heaters power consumption. In a second part, silicon photonics technology and cavity process flow will be detailed to fabricate the micro-ring resonators. The testing methodology will be then described. Finally, the impact of backside cavities on the tuning power and on the dynamics will be discussed.

II. FEM SIMULATION

In this part, the effect of a cavity on the backside of the substrate is studied. A 3D model of a RR with appropriate dimensions id created using COMSOL software. A power density is applied at the center of the ring such that the temperature inside the ring reached 100°C. This is repeated with three different cavity diameters: 25, 30 and 40 µm. For each cavity diameter, the power density is adjusted to match the temperature of 100°C in the ring. This power density is finally converted to power by multiplying the power density by the volume of the heater element.



As shown on figure N, the presence of the cavity changes the temperature field. The temperature is more uniform in the ring region. The heat also diffuses farther away from the ring, as illustrated in figure X, which shows the temperature along the ring radius. The temperature in the case of a ring without a backside cavity (in black) reaches equilibrium at 10 µm from the center (i.e. 2 radii), while backside cavities increase this distance up to 25 µm, or 5 radii. In most real-world designs, the rings are spaced out by more than 25 µm, therefore the thermal cross talk between adjacent rings can be neglected.

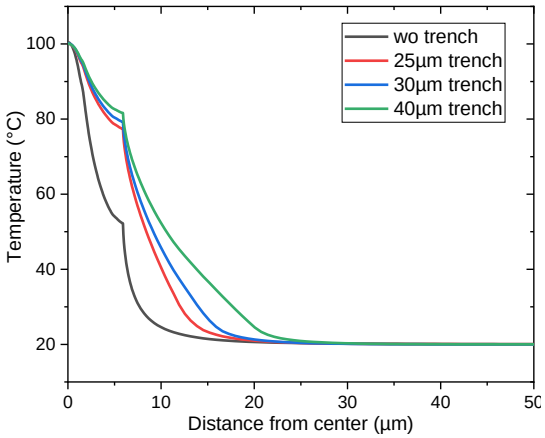


Figure 2: Temperature profile along a ring radius

The power required to reach 100°C inside the ring for the three cavities and a reference without cavity is presented in table 1. The simulations show that the power required can be reduced significantly, from 57% for the smaller cavity to 65% for the larger cavity.

Table 1: Power required for 100°C increase in model temperature with different cavity sizes

Cavity diameter	Power required for 100°C temperature increase (model) in mW	
Reference	5.65	-
25 µm	2.43	57%
30 µm	2.25	60%
40 µm	1.98	65%

III. PROCESS

This work is based on STMicroelectronics 2nd generation Si-photonics process, using 300 mm SOI wafers with 1.5 µm buried oxide layer (BOX) [3]. The silicon RR of interest have a 10 µm diameter with heaters of doped silicon on the waveguide level, in the middle of the resonator. The heater module is composed of 4 strips of doped Si located on the waveguide level, as shown in the middle of the ring of Figure 3, with 4 rows of 2 rectangular marks. By supplying them a direct current, these resistors will heat up thanks to Joule effect, increasing the temperature in their vicinity. The waveguides used in our rings are in deep-rib configuration with a 50 nm slab. The rings are connected thanks to four metal levels and Al pads for testing. A schematic cross section of the wafer can be seen in Figure 4.

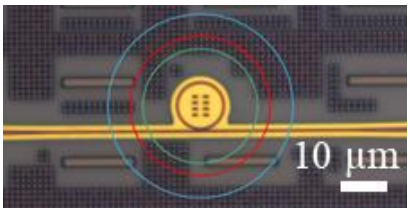


Figure 3: Optical top view of microring (purple and yellow) and etched cavities footprint to scale (green – 25 µm, red – 30 µm and blue – 40 µm)

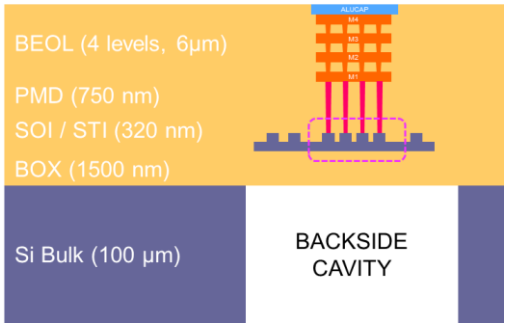


Figure 4: Schematic cross section of the stack at the end of process (not to scale)

After this standard photonic process (Figure 5 a), the front side of the wafers are bonded on carrier wafers with temporary glue (Figure 5 b), and thinned down to 100 µm. This thickness is compatible with the height of TSV-Mid process (10×100 µm) that will be integrated in similar wafers in order to create photonic interposers. The cavity patterning alignment is done on front side with Metal 1 marks thanks to a dedicated infrared Canon stepper. Marks have been chosen at Metal 1 level to insure a strong infrared contrast through the thinned silicon substrate from the wafer backside. Our alignment approach grants an accuracy below 1 µm between the waveguide level and the backside cavity. An 8 µm thick TCIR photoresist has been selected for the backside cavity lithography thanks to high etching selectivity with Si.

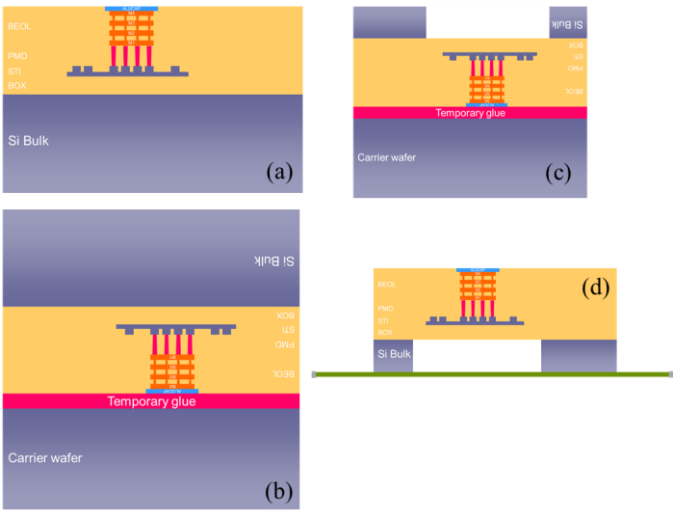


Figure 5: Process flow of the backside cavity

Cavities with diameters ranging from 25 to 40 µm are then etched from the backside in the bulk silicon down to the BOX, using deep reactive ion etching (DRIE). DRIE Bosch process was chosen for its highly anisotropic etching, ideal for high aspect ratio cavities. The selectivity of Si etching process over SiO_2 also allows an etch stop on the BOX layer.
On optical microscope observation, the RR is presented through the buried oxide layer from the backside of the wafer on Figure 6. This witnesses the quality of the alignment between the active photonics layer and the cavity.

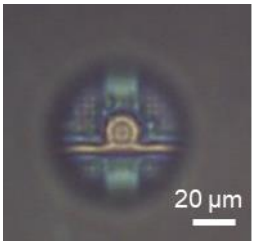


Figure 6: Optical back view of silicon microring resonator (yellow) through the BOX (from wafer backside)

Thanks to the high selectivity of the etching process between Si and SiO_2, it has been possible to perform only one single etching step for the 3 diameters cavity of 25, 30 and 40 µm despite the aspect ratio dependent etch effect.
After the backside etching (Figure 5 c), the thin wafer is debonded from its temporary carrier using an EVG820 tool to a handling tape and frame compatible with the prober station (Figure 5 d). In the case of TSV-mid process integration for photonic interposers [4], processed wafers could follow the standard backside process route (BRDL, organic passivation and under ball metallization). However, in this study no TSVs are implemented in the tested wafers.

IV. Tests

To measure the thermal tuning efficiency of the ring resonators, 4 test structures have been designed. Figure 7 shows the layout of the structure. RR structures are then processed with 25, 30 and 40 µm cavity diameter opening and one with no opening.

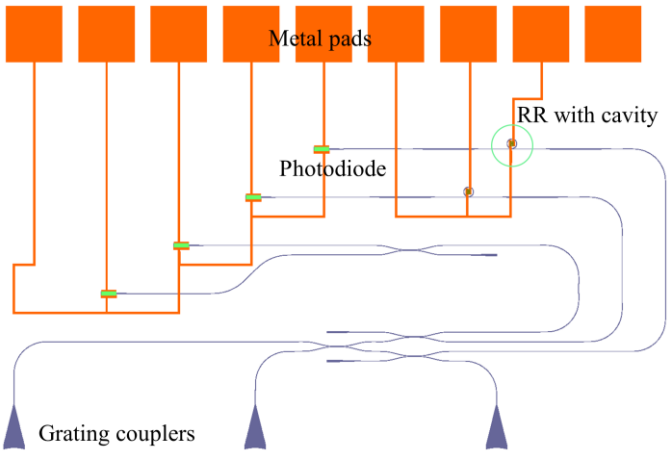


Figure 7:Test structure layout

Optical fibers are placed on top of grating couplers to infect light in the optical circuit. Fiber alignment is performed at each die using light exiting the circuit on the rightmost grating coupler. For this experiment, only the top row is of interest. Light passes through a ring resonator with (or without) backside cavities. The resonance peaks are be caused by destructive interference, resulting in an extinction peak in the output spectral response. Output light is then collected and converted to electrical current using a germanium p-i-n photodiode. The output current from the photodiode is then amplified with a trans-impedance amplifier (TIA) before acquisition. The input laser is tuned so that the spectral response goes from 1280 to 1340 nm with a step of 2 pm to have adequate resolution on the resonance peaks. The resonant wavelength closest to 1310 nm without heating is extracted for each of the 4 heater powers, and a linear fit yields the tuning efficiency. A total of 15 samples are measured for each cavity on the same wafer to reduce the variability inherent to the fabrication process.

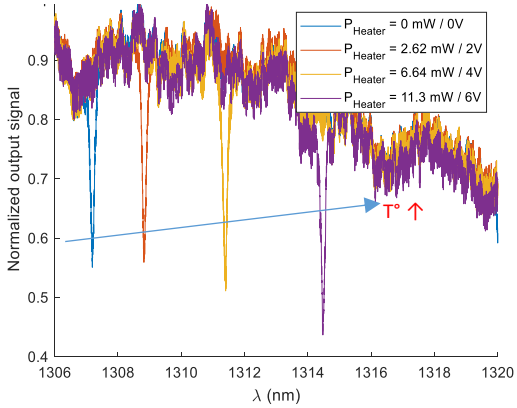


Figure 8: Evolution of the resonance peak with different applied heater powers of a 10-µm diameter RR with a 40-µm backside opening.

V. Results and Discussion

The impact of the cavities is deduced by comparing the tuning powers of the rings with different cavity diameters to a reference ring without cavity. Table 2 summarizes the average tuning power and their standard deviation for the different cavities and for the reference ring, as well as the relative improvement of the cavity on the tuning power compared to the reference ring.

Table 2: Tuning power and relative improvement for different cavity diameters

Cavity diameter	Tuning power (mW/nm) ± 1σ	Relative improvement over reference	Relative improvement (FEM)
Reference	5.76 ± 0.10	-	-
25 µm	1.88 ± 0.03	67%	57%
30 µm	1.74 ± 0.03	70%	60%
40 µm	1.61 ± 0.03	72%	65%

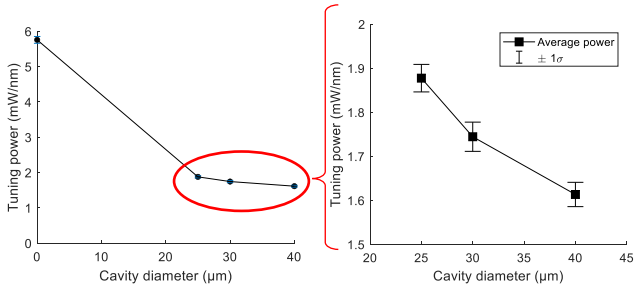


Figure 9: Tuning power evolution with cavity diameter

The measurements summarized in Figure 9 are in agreement with the simulations and show a vast reduction in the ring tuning power. For the 40 µm-cavity, the reduction is as important as 72%, while it is at 67% for the smaller 25 µm-cavity. This improvement can be attributed to a better heat confinement in the ring and lower heat losses via conduction from the substrate acting as a heatsink, as suggested by the FEM simulations.

On a complete optical network on chip architecture such as the one described in [5] with roughly 380 rings, the addition of backside cavities of diameter 40 µm can result in a power saving of several watts compared to an architecture without cavities. It also reduces the voltage needed to control the rings

Empirically, in order to maintain structural integrity of the substrate, two cavities must be separated by at least one diameter, e.g. two cavities with 40-µm diameter must be separated by 40 µm. The choice of the cavity diameter is therefore a compromise between performance (large diameter) and compactness of the final design (small diameter). Such compromise will need to be evaluated case by case by the designers.

VI. Dynamic Behavior of the Ring Resonators

In this part, the dynamic behavior of the ring will be studied. In particular, the impact of the cavity on the response time of the wavelength shift will be studied. The dynamic behavior is critical in applications were the RR are tuned dynamically to different wavelengths, such as in [2]. The switching frequency will therefore be limited by the delay taken by the ring to switch from one wavelength to another. The better heat confinement caused by the cavity helps reducing the static power consumption. The laser source is tuned to a specific wavelength, while a square signal is applied to the heater, creating cycles of heating and cooling. The voltage at the output of the TIA and photodiode is monitored using an oscilloscope. By setting the laser on the cold resonance wavelength, the heating will shift the resonance peak to the right, and the TIA voltage will shift from a low value corresponding to a resonant state to a higher voltage, corresponding to a non-resonant state. The time needed to shift from one state to the other is dictated by the heat diffusion phenomena, and is modified by the better heat trapping of the backside cavity.

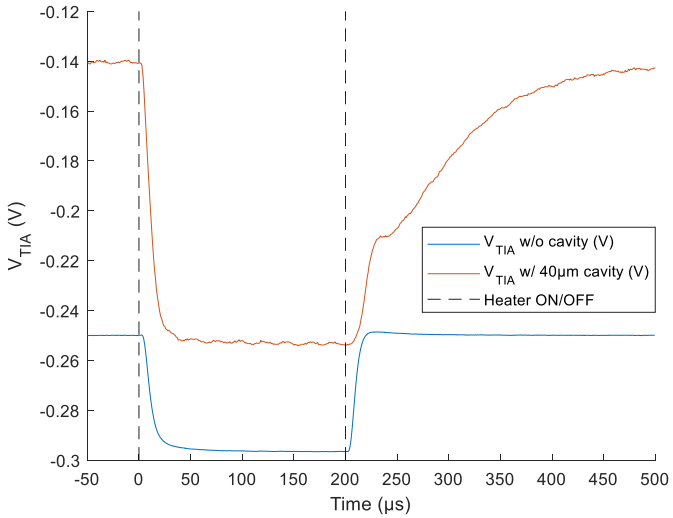


Figure 10: Time evolution of the RR output with and without cavity

Figure

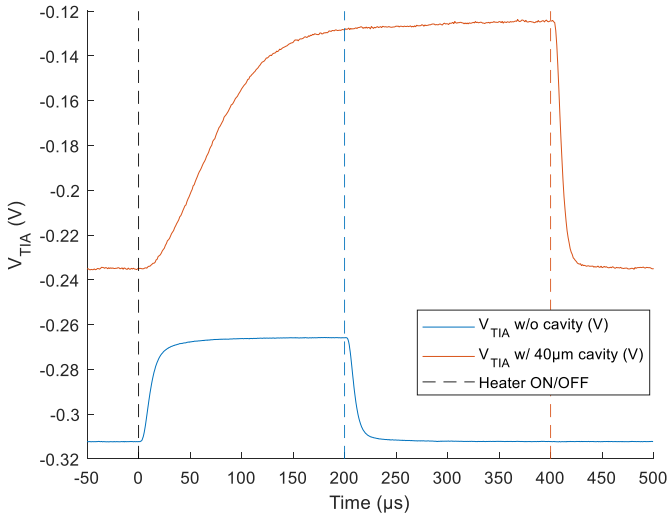


Figure 11: Time evolution of the RR output with and without cavity

VII. Conclusion

In this work, backside cavities have been successfully processed on silicon photonics wafers and evaluated. The developed process flow exhibits no incompatibly with a standard silicon photonics interposer process flow. These cavities allow to significantly lower power consumption for thermal tuning without undesirable changes in the ring behavior. It is shown that a 100 µm deep, 25 µm diameter cavity on a 10 µm ring reduces the tuning power needed by 67%, without changing the behavior of the ring, while a 40 µm cavity reduces the tuning power by 72%.

The Si/SiO_2 selectivity of the etching process allows multiple cavity diameters to be etched in a single step, allowing flexibility in the design of the photonic front end and minimal engineering for the realization of the backside cavity.

The cavities also introduce a longer cooling time, reducing thermal switching frequencies and must be taken into consideration for some applications.

Acknowledgement

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VIII. References

[1] M. Rakowski *et al.*, « A 4x20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver », in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, USA, févr. 2015, p. 1-3, doi: 10.1109/ISSCC.2015.7063099.

[2] Y. Thonnart *et al.*, « A 10Gb/s Si-photonic transceiver with 150µW 120µs-lock-time digitally supervised analog microring wavelength stabilization for 1Tb/s/mm ^{2} Die-to-Die Optical Networks », in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, févr. 2018, p. 350-352, doi: 10.1109/ISSCC.2018.8310328.

[3] F. Boeuf *et al.*, « A Silicon Photonics Technology for 400 Gbit/s Applications », p. 4.

[4] P. Tissier, J. Charbonnier, et R. Vélard, « Co-integration of TSV mid process and optical devices for Silicon photonics interposers », p. 5.

[5] Y. Thonnart *et al.*, « POPSTAR: a Robust Modular Optical NoC Architecture for Chiplet-based 3D Integrated Systems », p. 6.