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Backside cavities for thermal tuning optimization of silicon ring resonators

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Abstract— Silicon ring resonators on SOI substrates are well known and widely studied devices for silicon photonics-based systems. They are commonly used in datacom and high-performance computing for wavelength multiplexing, modulation and spectral filters. They can be tuned to the desired frequency with resistive heaters, which is the primary power budget of the device. In this work, backside cavities have been successfully etched in the bulk of the SOI substrate below ring resonators to improve heat trapping within the silicon rings. Simulations show that those backside cavities improve significantly heat confinement and minimizes locally heat losses due to conduction in the Si substrate. All the processes used in this study are compatible with the standard silicon photonics interposer process flow. A 72% power consumption reduction for a 10 μm diameter ring resonator on SOI has been achieved with a backside opening of 100 μm deep and 40 μm diameter, in good agreement with simulation results. Most importantly, the cavities opening did not impact the optical performances of the ring. Dynamic behavior of the rings was also studied, and show that the presence of cavities increases the thermal switching time of the rings.

Keywords— Silicon photonics, Three-dimensional integrated circuits, Optical resonators, Thermal management

I. INTRODUCTION

More and more data is being produced and transmitted all over the globe in bigger and bigger datacenters. Within these datacenters, optical links are used for their higher bandwidths compared to electrical links, as well as their better power efficiency, especially on longer distances [1].

Within the optical link chain, the endpoints need to convert the optical signal to electrical signal to be processed by integrated circuits, with standard silicon CMOS technology. Integrated silicon photonics propose an interesting path for increasing bandwidths for high speed communications in datacenter and high-performance computing applications.

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This technology can leverage the technical know-how of traditional CMOS foundries to make performant and reliable systems. Moreover they can be integrated more densely with the other integrated circuits also made of silicon [2].

An innovative technique to increase the bandwidth in the field of silicon photonics is to use wavelength multiplexing in transceivers and optical networks on chips (ONoC) communication. In this approach, multiple wavelengths of infrared light are injected in a single waveguide to carry parallelized signals to achieve high bandwidths, currently up to 400 Gbps. The different wavelengths must be separated in the point of use using specialized filters, for example ring resonators (RR). These filters can select with accuracy specific wavelengths corresponding to a specific data channel. A schematic view of a ring resonator is shown in Fig 1.

An accurate tuning of RR is needed to grant data transmission. This tuning is generally performed using thermo-optic effect in silicon, which links a change in refractive index of the silicon with temperature. In the case of silicon, this value is [3]:

$$dn/dT = 1.86 \cdot 10^{-4} K^{-1} \quad (1)$$

The change in refractive index caused by heating also affects the effective index, and finally the resonant wavelength of the ring λ_{res} , expressed as:

$$\lambda_{\text{res}} = \pi d n_{\text{eff}} / m \quad (2)$$

where d is the ring diameter, n_{eff} the effective index within the ring, and m an integer.

In order to heat the RRs, resistors within the silicon layer can be placed at the vicinity of the ring (similarly to [4]), or by using a metal film above the ring. Throughout this paper, the rings are designed with a radius of 10 μm . A schematic

drawing of the RR with its doped silicon heaters is shown in Fig. 1.

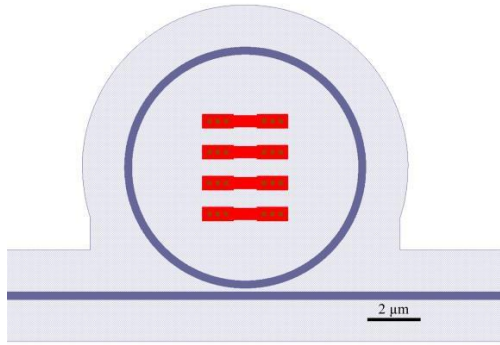


Fig. 1. Schematic view of the ring resonator (purple) and the silicon heaters (red)

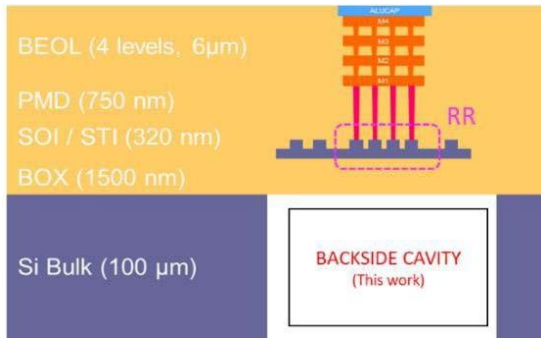


Fig. 2. Schematic cross section of the silicon photonic at the end of process (not to scale)

We define the “tuning power” of a ring resonator as follows:

$$\eta = \partial P / \partial \lambda \quad (3)$$

The tuning power η represents the power needed ∂P to shift the resonant wavelength by $\partial \lambda$ and will be expressed in mW/nm throughout this study. The smaller this quantity, the better as it represents a larger wavelength shift for the same amount of power.

As introduced in [5], the thermal tuning consumes half of the total power of the whole transceiver system. This work aims to reduce the thermal tuning power consumption by isolating the silicon ring resonator and to lower heat loss due to conduction in the bulk Si of SOI substrates. In this letter, simulations are first conducted to evaluate the impact of backside cavities on heaters power consumption, such as illustrated on Fig 2. In a second part, silicon photonics technology and cavity process flow are detailed to fabricate the micro-ring resonators. The testing methodology is then described. Finally, the impact of backside cavities on the tuning power and on the time-dependent properties are discussed.

II. FEM SIMULATIONS

In this part, the effect of a cavity on the backside of the substrate is studied. A 2D Axis-symmetry Finite Element

Method (FEM) solver is used to model the thermal behavior of a RR with appropriate dimensions (COMSOL Multiphysics). A power density is applied at the center of the ring such that the temperature inside the ring reaches 100°C (chosen arbitrarily) without insulating cavity, as shown in Fig. 3. This calculation is repeated in the presence of a backside cavity with three different diameters: 25, 30 and 40 μm . For each cavity diameter, the power density is adjusted to match the temperature of 100°C in the ring. This power density is finally converted to power by multiplying the power density by the volume of the heater element, represented in top view red in Fig. 1.

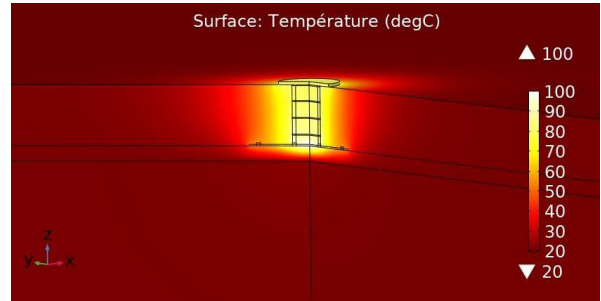


Fig. 3. Temperature gradient in the stack without backside cavity

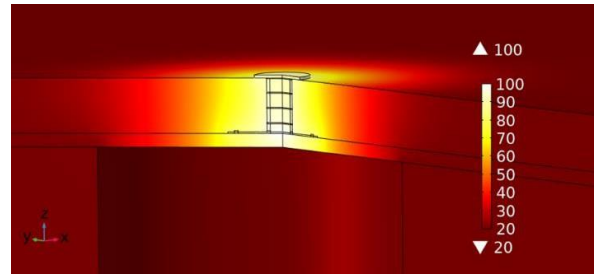


Fig. 4. Temperature gradient in the stack with a backside cavity

As shown on Fig. 3, the presence of the cavity changes the heat distribution, increasing the temperature laterally compared to the initial case without insulating cavity (Fig. 2). The temperature is thus more uniform in the ring region, and the heat diffuses farther away from the ring, as illustrated in Fig. 4, which shows the temperature along the ring radius. The temperature in the case of a ring without a backside cavity (in black) reaches equilibrium at 10 μm from the center (i.e. 2 times the ring radius), while backside cavities increase this distance up to 25 μm , or 5 times the ring radius. In most real-world designs, taking into account surrounding devices and electrical interconnects constraints, the rings are spaced out by more than 25 μm , therefore the thermal cross talk between adjacent rings should be negligible.

The computed power required to reach 100°C inside the ring for the three cavities and a reference without cavity is presented in Table 1. The simulations show that the power required to reach the 100°C target can be reduced significantly, from 57% for the smaller cavity to 65% for the larger cavity. The temperature has been taken as equal at the center of the ring, however it should be equal at the edge of the ring to have a direct comparison. Fig. 5 introduces the radial thermal profile from the ring center for each case. The kink at 5 μm is due to the material change between the silicon ring and SiO₂ cladding. This Fig. 5 shows that the temperature at the edge of the ring with cavities (or trenches), 5 μm from

the center, is around 80°C while it is only 60°C on the ring without cavity. This simulation therefore slightly overestimates the power consumption of such a device, as the heater in the ring with cavity needs to heat less the ring to reach the same edge temperature of 60°C.

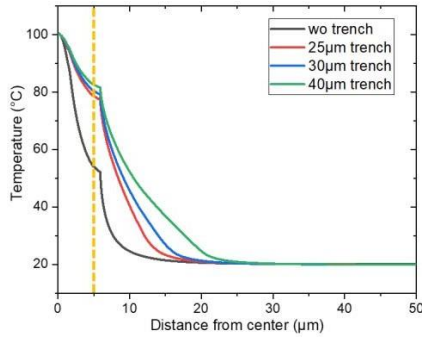


Fig. 5. Temperature profile along a ring radius (the dashed line represents the end of the RR) with 100°C boundary condition in the ring center.

TABLE I. POWER REQUIRED FOR 100°C INCREASE IN MODEL TEMPERATURE WITH DIFFERENT CAVITY SIZES

Cavity diameter	Power required for 100°C temperature increase (model) in mW	
Reference	5.65	-
25 μm	2.43	57%
30 μm	2.25	60%
40 μm	1.98	65%

III. FABRICATION PROCESSES

This work is based on STMicroelectronics 2nd generation Si-photonics process, using 300 mm SOI wafers with 1.5 μm buried oxide layer (BOX) [6]. The silicon RR of interest have a 10 μm diameter with heaters of doped silicon on the waveguide level, in the middle of the resonator. The heater module is composed of 4 strips of doped Si located on the waveguide level, as shown in the middle of the ring of Fig. 6, with 4 rows of 2 rectangular marks. By supplying them a direct current, these resistors will heat up thanks to Joule effect, increasing the temperature in their vicinity. The waveguides used in our rings are in deep-rib configuration with a 50 nm slab. The ring heaters are connected thanks to four metal levels and Al pads for testing.



Fig. 6. Optical top view of microring (purple and yellow) and etched cavities footprint to scale (green – 25 μm, red – 30 μm and blue – 40 μm)

After this standard photonic process (Fig. 7a), where waveguides, rings, photodiodes are realized, the front side of the wafers are bonded on carrier wafers with temporary glue (Fig. 7b), and thinned down to 100 μm. This thickness was chosen because it is compatible with the height of TSV-Mid process (10×100 μm) that will be integrated in similar wafers

in order to create photonic interposers. Interposers need to interconnect their front and back side, and use TSVs to realize this interconnection. The cavity patterning alignment is done on front side with marks embedded on the first metal layer thanks to a dedicated infrared Canon stepper. Marks have been chosen at Metal 1 level to ensure a strong infrared contrast through the thinned silicon substrate from the wafer backside. Our alignment approach grants an accuracy below 1 μm between the waveguide level and the backside cavity. An 8 μm thick TCIR (Tokyo Ohka Kogyo) has been selected for the backside cavity lithography thanks to its high etching selectivity with Si.

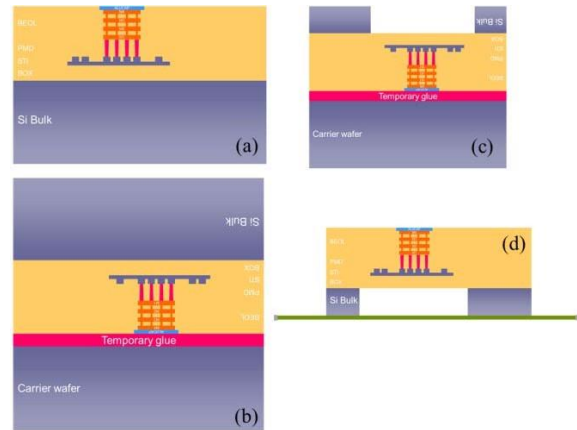


Fig. 7. Process flow of the backside cavity. (a) photonic front end and metal layers, (b) temporary bonding and grinding, (c) backside cavity etching, (d) debonding and testing

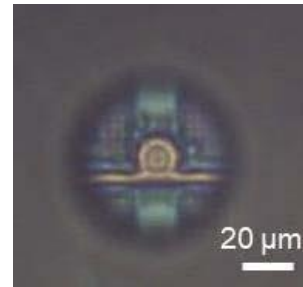


Fig. 8. Optical view of silicon microring resonator (yellow) through the backside cavity and BOX (from wafer backside)

Cavities with diameters ranging from 25 to 40 μm are then etched from the backside in the bulk silicon down to the BOX, using deep reactive ion etching (DRIE). DRIE Bosch process was chosen for its highly anisotropic etching, ideal for high aspect ratio cavities. The selectivity of Si etching process over SiO₂ also allows an etch stop on the BOX layer, leaving the photonic front side undamaged by this etch.

On optical microscope observation, the RR is visible through the buried oxide layer from the backside of the wafer on Fig 8. This witnesses the quality of the alignment between the active photonics layer and the cavity.

Thanks to the high selectivity of the etching process between Si and SiO₂, it has been possible to perform only one single etching step for the 3 cavity diameters of 25, 30 and 40 μm despite the aspect ratio dependent etch effect. A cross section shown in Fig. 9 shows a 25 μm cavity below a ring

resonator, and shows no cracks or delamination in the dielectric layers, confirming the compatibility of the process.

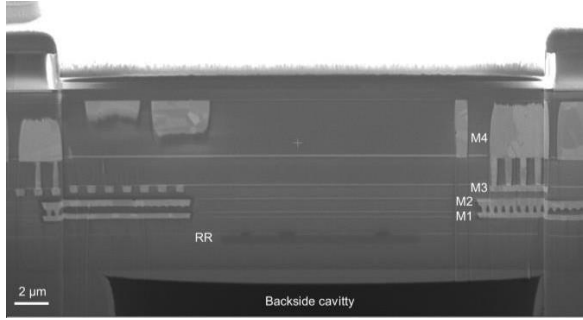


Fig. 9. SEM view of a cross section of a RR and the backside cavity.

After the backside etching (Fig. 7c), the thin wafer is debonded from its temporary carrier using an EVG850 tool to a handling tape and frame compatible with the prober station (Fig. 7d). In the case of TSV-mid process integration for photonic interposers [5, 6], processed wafers could follow the standard backside process route (backside redistribution layer, organic passivation and under ball metallization). However, in this study no TSVs are implemented in the tested wafers.

IV. TESTS

To measure the thermal tuning efficiency of the ring resonators, four test structures have been designed. Fig. 10 shows the layout of the test structure. RR structures are then processed with 25, 30 and 40 μm cavity diameter opening and one with no opening as reference. The tests are done using a Cascade Microtech prober, that is compatible with thin wafers on debonding tape and frame.

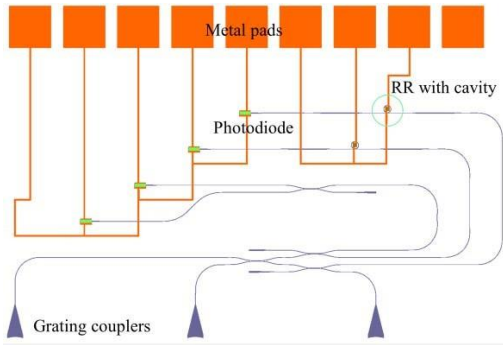


Fig. 10. Test structure layout of RR with cavity.

Optical fibers are placed on top of grating couplers to inject light in the optical circuit using the middle grating coupler. Fiber alignment is performed at each die to couple light into the photonic circuit using the rightmost grating coupler as an output. For this experiment, only the top row is of interest. Light passes through a ring resonator with (or without) backside cavities. The resonance peaks are due to destructive interferences, resulting in an extinction peak in the output spectral response. Output light is then collected and converted to electrical current using a germanium p-i-n photodiode. The output current from the photodiode is then amplified with a trans-impedance amplifier (TIA) before read-out. The input laser is tuned so that the spectral response goes from 1280 to 1340 nm with a step of 2 nm to have adequate resolution on the resonance peaks. The resonant wavelength

closest to 1310 nm is extracted for each of the 4 heater powers, and a linear fit yields the tuning efficiency. An example of resonance evolution is presented in Fig. 11. A total of 15 samples are measured for each cavity on the same wafer to reduce the variability inherent to the fabrication process.

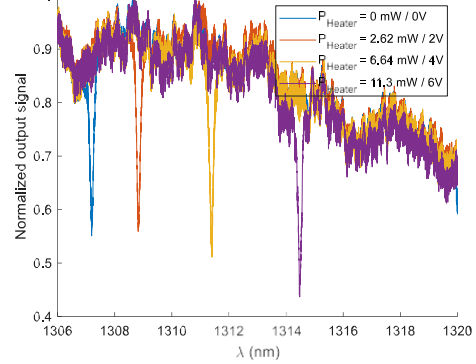


Fig. 11. Evolution of the resonance peak with different applied heater powers of a 10 μm diameter RR with a 40 μm backside opening. The peak shifts to the right as temperature increases.

V. RESULTS AND DISCUSSION

The impact of the cavities is deduced by comparing the tuning powers of the rings with different cavity diameters to a reference ring without cavity. Table 2 summarizes the average tuning power and their standard deviation for the different cavities and for the reference ring, as well as the relative improvement of the cavity on the tuning power compared to the reference ring and previous FEM simulations.

TABLE II. TUNING POWER AND RELATIVE IMPROVEMENT FOR DIFFERENT CAVITY DIAMETERS

Cavity diameter	Tuning power (mW/nm) $\pm 1\sigma$	Relative improvement over reference	Relative improvement (FEM section II)
Reference	5.76 \pm 0.10	-	-
25 μm	1.88 \pm 0.03	67%	57%
30 μm	1.74 \pm 0.03	70%	60%
40 μm	1.61 \pm 0.03	72%	65%

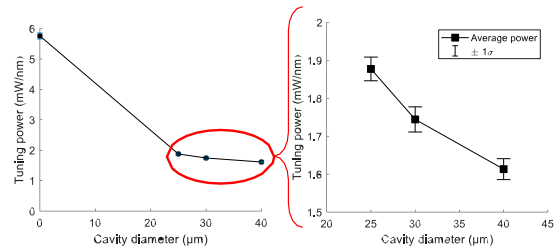


Fig. 12. Tuning power evolution with cavity diameter

The results shown in Fig. 12 are in agreement with the simulations and show a vast reduction in the ring tuning power. For the 40 μm -cavity, the reduction is as important as 72%, while it is at 67% for the smaller 25 μm -cavity. This improvement can be attributed to a better heat confinement in the ring and lower heat losses via conduction from the substrate acting as a heatsink, as suggested by the FEM simulations.

On a complete optical network on chip architecture such as the one described in [9] with roughly 380 rings, the addition of backside cavities of diameter 40 μm can result in a power saving of several watts compared to an architecture without cavities. This saving can scale to several tens of watts as many of these transceivers can be used in the same datacenter rack. It also reduces the voltage needed to control the rings, which simplifies the design of the control electronics.

Empirically, in order to maintain structural integrity of the substrate, two cavities must be separated by at least one diameter, e.g. two cavities with 40- μm diameter must be also separated by 40 μm . The choice of the cavity diameter is therefore a compromise between performance (large diameter) and floor plan density of the final design (small diameter). Such compromise will need to be evaluated case by case by the designers depending on the application.

VI. DYNAMIC BEHAVIOR OF THE RING RESONATORS

In this part, the dynamic behavior of the ring will be studied. In particular, the impact of the cavity on the response time of the wavelength shift will be detailed. The dynamic behavior is critical in applications where the RR are tuned dynamically to different wavelengths, such as in [5]. The switching frequency will therefore be limited by the delay taken by the ring to switch from one wavelength to another.

The experimental setup is similar to the one described above. The laser source is tuned to a specific wavelength, while a square signal is applied to the heater, creating cycles of heating and cooling. The voltage at the output of the TIA and photodiode is monitored using an oscilloscope. By setting the laser on the cold resonance wavelength, the heating will shift the resonance peak to the right (towards higher wavelengths), and the TIA voltage will shift from a low value corresponding to a resonant state to a higher voltage, corresponding to a non-resonant state. Similarly, by setting the laser wavelength to the “hot” resonant wavelength, the TIA voltage will shift from a high value corresponding to the non-resonant state to the resonant state at a low voltage. Fig. 13 illustrates the wavelength shift caused by the heating. When the laser is set to the “cold” state (blue dashed line), the heating will enable us to observe the left-hand-side of the peak (zone (a) on Fig. 13), and the laser at the “hot” state will enable us to observe the right-hand-side of the peak (zone (b) on Fig. 13).

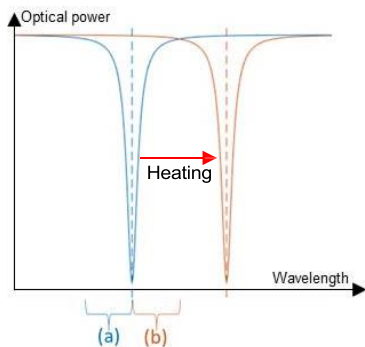


Fig. 13. Schematic spectral responses of a RR at cold state (blue) and hot state (orange).

The time needed to shift from one state to the other is limited by the heat diffusion phenomena, and is modified by the increased heat insulation of the backside cavity.

Fig. 14 shows the evolution of the output voltage from the photodiode TIA when heating is applied from 0 to 200 μs on the horizontal axis. The laser wavelength is set so that when heated, the ring will be in the resonant state. The vertical offset observed between the reference RR and the RR with a cavity can be explained by a difference in fabrication process and quality factor of the ring. The switching time between two states is determined when the signal reaches 95% of the steady-state value. When heating to a resonant state as illustrated on Fig. 14, both rings behave similarly, with a switching time around 30 μs . However, when cooling the ring, the two rings have significantly different behaviors. The reference ring has a cooling time comparable to its heating time, while the RR with cavity reaches equilibrium in 230 μs , ten times its heating time constant.

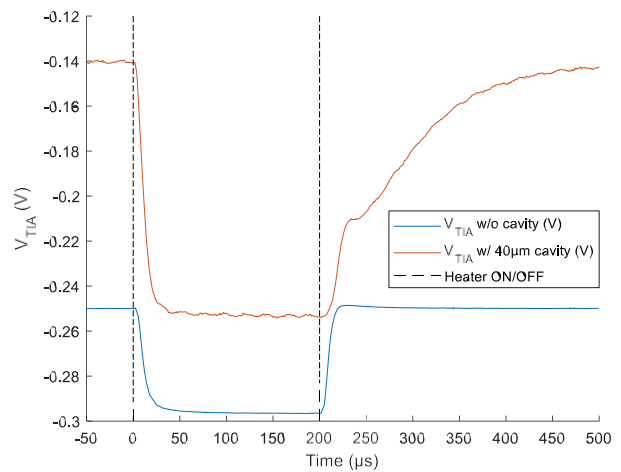


Fig. 14. Time evolution of the RR output with and without cavity at hot resonant wavelength. Dashed lines represent the ON/OFF switching of the heater.

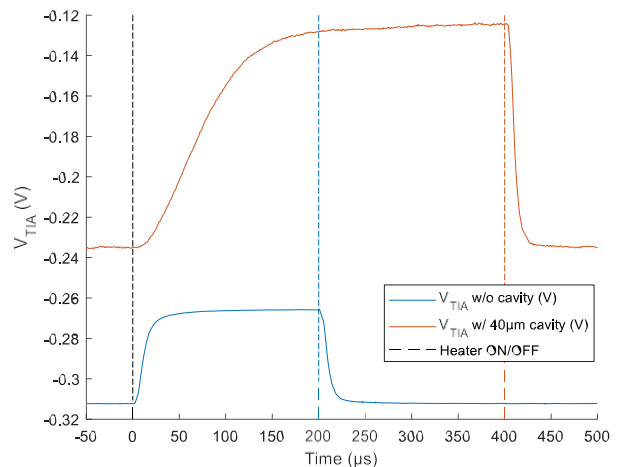


Fig. 15. Time evolution of the RR output with and without cavity at cold resonant wavelength. Switching ON/OFF of heater (blue dot line for w/o cavity, red dot line for w/40 μm cavity).

Fig. 15 is similar to Fig. 14, except that the laser wavelength is now tuned to the resonant frequency of the ring

when not heated. Here, because the RR with cavity takes longer than 200 μs to reach equilibrium when heated, the heating time has been increased to 400 μs (until the orange vertical dashed line), while the reference RR was heated for 200 μs (until the blue vertical dashed line). Here the reference ring keeps the same time constants for heating and cooling, while the RR with cavity takes 170 μs to reach equilibrium while heating. However, the cooling takes 25 μs , similar to the reference RR at 23 μs . All the time constants are summarized in Table 3.

These results indicate a change in behavior of the RR with cavity, where going from a resonant state to a non-resonant state requires a longer transition time (5 to 10 times) than an identical ring with no cavity. This behavior is indeed similar no matter whether heating (Fig. 14) or cooling (Fig. 13) is applied. Further characterizations are ongoing to fully understand this asymmetric behavior, especially in the case of heating illustrated in Fig. 15.

If we consider a typical response time of 200 μs , the switching frequency of the ring with cavity decreases to 5 kHz, compared to the 10 kHz described on [5]. This asymmetric behavior evidenced in this study has therefore to be taken into account when controlling the ring dynamically. However, it is not problematic when the rings are used in a static environment or with slow switching frequencies, such as in dense wavelength division multiplexing (DWDM) where rings are tuned to a single wavelength for the whole lifetime of the system.

TABLE III. TIME CONSTANTS FOR RR THERMAL SHIFTING

		Without cavity	With cavity
Laser at hot resonance (Fig. 13 & 12b)	Heating	32.5 μs	28 μs
	Cooling	17.5 μs	232 μs
Laser at cold resonance (Fig. 14 & 12a)	Heating	44 μs	171 μs
	Cooling	23 μs	25.5 μs

VII. CONCLUSION

In this work, backside cavities have been processed on silicon photonics wafers and successfully evaluated. The developed process flow exhibits full compatibility with a standard silicon photonics interposer process flow. These cavities allow to significantly lower power consumption for thermal tuning without undesirable changes in the ring behavior. It is shown that a 100 μm deep, 25 μm diameter cavity on a 10 μm ring reduces the tuning power needed by 67%, without changing the behavior of the ring, while a 40 μm cavity reduces the tuning power by 72%.

The Si/SiO₂ selectivity of the etching process enables multiple cavity diameters to be etched in a single step, with minimal process engineering. The DRIE process allows high aspect ratios etchings, and can be done on full-thickness wafers, albeit with a larger cavity diameter (80 μm for a standard 12" wafer and an aspect ratio of 1:10).

The cavities also introduce a longer thermal switching time, reducing switching frequencies and must be taken into consideration for applications with dynamic thermal tuning of ring resonators. However, for applications such as DWDM, the switching times do not need to be taken into account as the rings are operated in a static manner and are not switched at a high enough frequency to be impacted by the cavity. The

different behavior of the ring with cavity compared to a reference ring is not yet fully understood and more studies are ongoing to grasp a better understanding

Finally, this work demonstrates the realization of an innovative approach, enabling significant power savings for thermal tuning, while having high flexibility for ring resonator-based systems. This approach is especially interesting for ONoC systems and is implemented in our current prototype.

REFERENCES

- [1] CISCO global cloud index; <http://www.cisco.com>,
- [2] F. Boeuf *et al.*, "Silicon Photonics R&D and Manufacturing on 300-mm Wafer Platform," in *Journal of Lightwave Technology*, vol. 34, no. 2, pp. 286-295, 15 Jan. 15, 2016, doi: 10.1109/JLT.2015.2481602.
- [3] G. T. Reed and A. P. Knights, *Silicon photonics: an introduction*. Chichester ; Hoboken, NJ: John Wiley, 2004.
- [4] M. Rakowski *et al.*, "A 4x20Gb/s WDM ring-based hybrid CMOS silicon photonics transceiver," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2015, pp. 1–3, doi: 10.1109/ISSCC.2015.7063099.
- [5] Y. Thonnart *et al.*, "A 10Gb/s Si-photonics transceiver with 150 μW 120 μs -lock-time digitally supervised analog microring wavelength stabilization for 1Tb/s/mm² Die-to-Die Optical Networks," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, Feb. 2018, pp. 350–352, doi: 10.1109/ISSCC.2018.8310328.
- [6] F. Boeuf *et al.*, "A Silicon Photonics Technology for 400 Gbit/s Applications", *2019 IEEE International Electron Devices Meeting (IEDM)*, pp. 33.1.1-33.1.4, Dec. 2019.
- [7] P. Tissier *et al.*, "Co-integration of TSV mid process and optical devices for Silicon photonics interposers," in *Electronics System-Integration Technology Conference (ESTC) 2020 IEEE 8th*, pp. 1-5, 2020
- [8] P. Tissier *et al.*, "Stress analysis and compensation for large silicon photonic interposers," in *Materials for Advanced Metallizations Conference (MAM) 2020, unpublished*
- [9] Y. Thonnart *et al.*, "POPSTAR: a Robust Modular Optical NoC Architecture for Chiplet-based 3D Integrated Systems," *Proc. DATE*, 2020, p. 6.