Electro-Thermal Investigation of SiGe HBTs: A Review

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Abstract— **This paper presents a review on the electro-thermal investigation of SiGe HBT technologies. After introducing a simple method of measuring thermal resistance (R_{TH}), analytical studies on the calculation of R_{TH} is discussed and subsequently the contribution of the back-end-of-line metal lines is estimated. Based on this analysis, strategies for the optimum emitter finger placements while designing a power amplifier cell are investigated. Finally, the thermal impedance measurement and modelling aspects are discussed.**

***Index Terms*— SiGe HBTs, R_{TH}, self-heating, pulsed measurements, heat transfer equation, electro-thermal compact modelling, thermal impedance, low frequency S-parameter, mutual heating, PA-cell design, BEOL: Back-end-Of-Line; FEOL: Front-end-Of-Line**

I. INTRODUCTION

For all applications demanding high RF performance, mixed-signal capabilities, reduced dimensions, relatively low cost and mass production, BiCMOS is the technology of choice. Typical commercial applications are high-data rate wireless communications, optoelectronic data links and next-generation automotive radar sensors. In order to achieve very high frequency performance in SiGe HBT, aggressive scaling (in particular vertical, but also lateral) is carried out combined with innovative architectures (in particular for low base resistance and reduced base-collector capacitance). Consequently, the devices are operating at extremely high current densities (up to 30 mA/µm^2 which corresponds to an incredible 30 thousand Amps/mm^2!). Thus it is not surprising that the heat inside the device becomes an issue.

This paper reviews different aspects of this electro-thermal heating problem inside the device and aims to respond to the following research questions with respect to the thermal resistance (R_{TH}) and thermal impedance (Z_{TH}):

1. Within the purview of steady state thermal behavior, we shall reflect on (i) finding the most appropriate method for measuring R_{TH}, (ii) suitable theoretical approach that allows us to obtain appropriate analytical expression for R_{TH} satisfying the scaling requirements and (iii) designing a power amplifier (PA) cell in terms of emitter finger configuration, spacing and layout in order to minimize self-heating and mutual thermal coupling effects.
2. On the other hand, from the perspectives of transient and/or AC thermal behavior, we shall discuss on (i) the procedure of measuring Z_{TH}, (ii) analytical modeling of Z_{TH} from the fundamental heat transfer equation and (iii) finding a SPICE compatible Z_{TH}-model.

II. STEADY STATE THERMAL BEHAVIOR

A. Finding the most appropriate method for measuring R_{TH}

A wide collection of the extraction techniques for junction temperature estimation is available in the literature [Rei92, Wald92, Bovo98, Mars00, Rieh05]. A detailed review of all these techniques is available in [Russo-9]. Here we shall focus on a measurement technique that is easy to set-up, simple to implement and yields reliable results. The basic idea was first introduced by J. Berkner [Ber07]. Further investigations concerning scaling, and its ability to extract the temperature dependent R_{TH} are presented in [Suresh17]. The recent work of [Hus21] improves the intersection method considering the R_{TH}-dependence on ambient temperature and power.

The method requires the measurement of the Gummel-characteristics at two different ambient temperatures ($T_{amb,1}$ and $T_{amb,2}$) and at two different V_{CE} ($V_{CE,1}$ and $V_{CE,2}$) as show in Fig 1. From the intersection point of these two curves one obtains R_{TH} as

$$R_{TH} = \frac{T_{amb,2} - T_{amb,1}}{P_{diss,1} - P_{diss,2}} \qquad (1)$$

where $P_{diss,1/2} = I_C V_{CE,1/2}$ at the intersection point. Formulation (1) assumes that Early and avalanche effects are negligible and the intersection point lies below high current effect region.

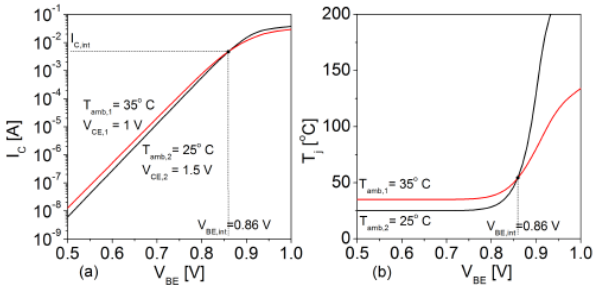

Fig. 1: Simulation results of forward Gummel behaviour of a 0.2x5 µm^2 device at two different T_{amb} and V_{CE}. The intersection point is denoted as ($V_{BE;int}$; $I_{C;int}$), [Suresh17]

To fully assess the accuracy of the method, simulations have been carried out with the model card of $W_E x L_E$= 0.2x5µm^2 SiGe HBT structure at eight different T_{amb} from 25°Cto 95°C. Fig. 2(a) compares the junction temperature (T_j) dependent R_{TH} results extracted following the approach of [Pfost03], [Russo6], and the intersection technique. Although R_{TH} for small values of T_j shows reasonable accuracy for all these methods, the temperature dependence of R_{TH} is extracted accurately only using the intersection method.

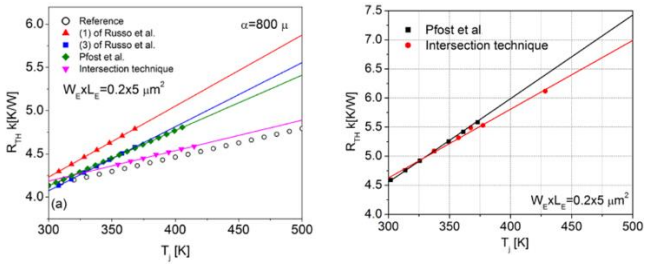

Fig. 2: Junction temperature dependent thermal resistance. (left simulation study, right: $R_{TH}(T_j)$ extracted from measurements for a 0.2x5 µm² SiGe HBT [Suresh17]

Fig. 2b shows the $R_{TH}(T_j)$ extracted from the measurements using the method of [Pfost03] and the intersection technique. Although R_{TH} values extracted from both these methods are comparable at low T_j, the results of [Pfost03] deviate with a higher slope compared to that of the intersection technique at higher T_j. Thus a significant overestimate of R_{TH} is observed at high temperatures because of the additional temperature dependent effects from emitter and collector resistances. The differential approach of the intersection method eliminates any such effect of temperature from the parameters other than R_{TH}, thereby accurately estimating its temperature dependence.

B. Towards a scalable analytical expression for R_{TH}

An accurate estimation of R_{TH} is essential from the perspectives of both device design and compact modeling [Schr10]. Especially for power amplifier (PA) design, it must be ensured that the device stays in the safe operating area during its operation. Like other circuits, PA design relies on a physics-based geometry scalable compact model.

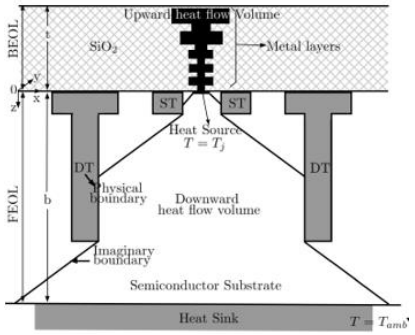

Fig. 3: Illustration of the heat flow volume in a simple vertical bipolar structure considering the BEOL metal layers and its equivalent thermal network representation. Note that the heat source is assumed to be at the metal–semiconductor junction. b and t denote the distance from the heat source to the substrate and BEOL metal layers, respectively. [Sur17]

Fig. 3 represents a cross section view of a typical HBT structure including shallow trench and deep trench isolation. The structure clearly depicts the front-end-of-line (FEOL) and the back-end-of-line (BEOL) portions. Each of these parts has its own thermal character resulting in two separate thermal resistances $R_{TH,s}$ (for FEOL) and $R_{TH,m}$ (for BEOL), connected in parallel to the heat source located at the base-collector junction of the device (below the surface of the BEOL). The effective R_{TH}, therefore, can be expressed as

$$\frac{1}{R_{TH}} = \frac{1}{R_{TH,s}} + \frac{1}{R_{TH,m}} \tag{2}$$

For the BEOL part, no general analytical formula exists in the literature. This is mainly due to the fact that the BEOL stack is not universally defined. In fact, the connection of the metal stacks to the device is dependent on circuit design and differs in various designs. Moreover, the surface temperature is not exactly known and the assumption that the surface is at ambient temperature is questionable.

On the other hand, for the FEOL, the calculation of $R_{TH,s}$ is possible [Sur17] and needs to consider (i) the complicated geometry for the heat flux and (ii) temperature dependence of thermal conductivity of the material. The physics based relation for $R_{TH,s}$ reads

$$R_{TH,s} = \int_0^b \frac{dz}{\kappa_s(T) A_s(x,y,z)} \tag{3}$$

where b, $A_s(x, y, z)$, and $\kappa_s(T(z))$ are, respectively, the Si-film thickness, position-dependent area of the heat-flow section and positional temperature-dependent thermal conductivity of the Si-film. Since κ_s is temperature-dependent and in turn this temperature is position-dependent, it is not possible to calculate the integral straightforwardly. However, it can be done using the Kirchhoff transformation as described in [Wal02] or by introducing an average thermal conductivity introduced in [Sur17]. In the latter approach, one starts from the temperature dependent κ_s of silicon described by

$$\kappa_s(T) = \frac{\beta}{T^\alpha} \tag{4}$$

where $\beta = 3.09 \times 10^5$ WK$^{\alpha-1}$/m and $\alpha = 1.34$ for intrinsic silicon. An average thermal conductivity for the entire downward heat diffusion in the semiconductor can be obtained as

$$\kappa_{s,avg} = \frac{1}{T_j - T_{amb}} \int_{T_{amb}}^{T_j} \frac{\beta}{T^\alpha} dT = \frac{\beta}{1-\alpha} \left(\frac{T_j^{1-\alpha} - T_{amb}^{1-\alpha}}{T_j - T_{amb}} \right) \tag{5}$$

With this position-independent $\kappa_{s,avg.}$ $R_{TH,s}$ in (3) can be integrated to obtain

$$R_{TH,s} = \frac{1}{\kappa_{s,avg}} f(G_s) \tag{6}$$

where $f(G_s)$ is a function of the heat flow geometry and can be obtained following e.g. [Gao91]. Substituting (5) in (6), and introducing the rise in temperature $\Delta T = T_j - T_{amb}$, we obtain

$$\Delta T = \sqrt[1-\alpha]{T_{amb}^{1-\alpha} + P_{diss} \frac{(1-\alpha) f(G)}{\beta}} - T_{amb} \tag{7}$$

and subsequently the $R_{TH,s}$ is calculated as $\Delta T / P_{\text{diss.}}$ The values of α and β depend on doping and material combinations (e.g., SiGe) and therefore should be extracted for a practical device [Ales16]. The result in (7) is identical to the one reported in [Wal02, eq. (14)], which is achieved by performing the Kirchhoff transformation on the steady-state heat conduction equation. Eventually, we can now calculate $R_{TH,s}$ analytically and it is made scalable through the factor $f(G_s)$.

Once, we calculated the value of $R_{TH,s}$ corresponding to the FEOL-part and extracted a value of the total R_{TH} using e.g. the method presented in section II-A, we can estimate the contribution of the BEOL ($R_{TH,m}$) using (2) or following the

analytical framework from [Nid22] which takes in addition into account the temperature dependence of $R_{TH,m}$. We present the results from transistors with different emitter lengths (L_E) at a fixed W_E of 0.27 µm corresponding to STMicroelectronics B9MW process [Chan10]. Fig 4 compares the different contributions of the FEOL and BEOL parts to the overall R_{TH} for different emitter lengths.

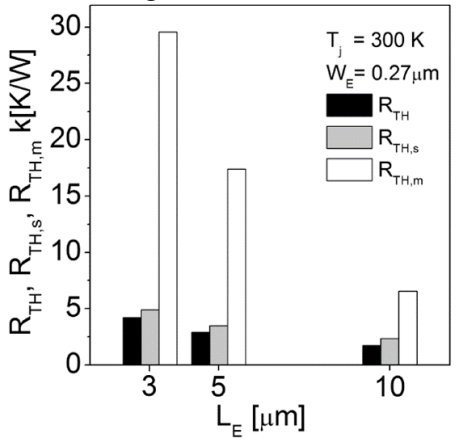

Fig. 4: Comparison of RTH, RTH,s and RTH,m for different values of LE at a fixed We of 0.27µm. [Sur17]

From this data we can calculate the percentage contribution of the BEOL part with respect to the total R_{TH}. The results are presented in Table 1 below.

Table 1: Percentage contribution of the BEOL part with respect to the total R_{TH} for different emitter lengths L_E

W_E=0.27µm, L_E (µm)	3	5	10
BEOL-contribution (%)	14	17	26

We recognize that the contribution of $R_{TH,m}$ increases with emitter lengths and achieves for this given technology more than 25% in case of the longest emitter. This represents a significant value. A way to reduce this value is to add metal emitter stacks to enhance the cooling performance [Esp17].

C. PA cell design

Typically, in SiGe-HBT based output stages, the transistor layout consists of many emitter stripes connected in parallel. Due to the heat dissipated in the transistor and thermal coupling effect, the central emitter fingers will have higher local temperature than those on the periphery. Higher temperature results in higher current that leads to additional heat and further increase in current entailing thermal runaway in certain devices. The temperature increases due to self-heating and coupling between the emitter fingers can be described by

$$\Delta T_i = \Delta T_{ii} + \sum_{j=1,j\neq i}^{n} \Delta T_{ij} = P_{d,i} R_{TH,ii} + \sum_{j=i,j\neq i}^{n} c_{ij} P_{d,j} R_{TH,jj} \quad (8)$$

where the first term indicates the self-heating at i^{th} finger and the second term accounts for the thermal coupling on i^{th} finger from all other fingers. $P_{d,i}$ ($P_{d,j}$) and $R_{th,ii}$ ($R_{th,jj}$) are, respectively, the electrical power dissipation and thermal resistance corresponding to the i^{th} (j^{th}) finger. Static thermal coupling coefficient (c_{ij}) quantifies the amount of mutual thermal coupling over finger-*i* due to the heat source at finger-*j* and is defined as:

$$c_{ij} = \frac{\Delta T_{ij}}{\Delta T_{jj}} \quad (9)$$

A particularly interesting work reported in [Goh16] attempted to model the thermal coupling from the isothermal contours in GaAs multifinger HBTs. Although the work provides an important insight that the coupling effect can be predicted from the modeling framework of self-heating, the application of the approach is limited only to structures without any trench isolation. Besides, the model does not consider the temperature dependent thermal conductivity. Nonetheless, starting from [Goh16], we provided a physics-based formulation to find out the coupling factors in a multifinger structure including shallow- and deep-trench isolation [Gup20].

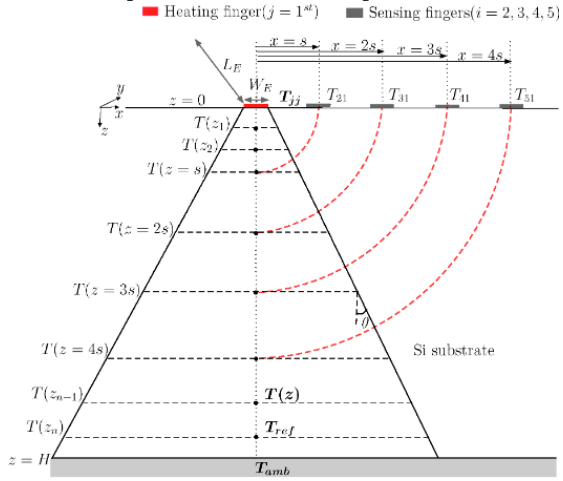

Fig. 5: Schematic cross-section of a multifinger transistor structure with finger spacing s. Heat source is located at z=0. The isotherms linking the heating finger and the sensing fingers are systematically shown. [Gup20]

Observing Fig. 5, where a schematic cross-section of a multifinger transistor structure with finger spacing *s* is sketched, we recognize that the temperature rise at the heating finger affects the operating temperature of the neighboring fingers through thermal coupling. Following [Goh16], we assume circular isotherms for this structure having no-trench isolation resulting into identical temperature profile in the vertical (z-) and lateral (x-) directions, i.e., $T_{nt}(z)=T_{nt}(x)$. Therefore, temperature rise at the sensing finger-*i* due to the heat source at finger-*j* can be estimated directly from the z-dependent temperature profile of finger-*j*. Finally, the thermal coupling factor between finger-*i* and finger-*j* for the multifinger structure with no-trench ($c_{ij,nt}$) can be obtained using (9). Thanks to this theoretical framework it is now possible to optimize the spacing in order to achieve quasi-uniform temperature dependence for the different emitter stripes as shown on Fig. 6 [Gup22]. Fig. 7 compares the true finger temperature T_i obtained from the theoretical framework mentioned above for a five-finger transistor. The two sets of data with blue and orange lines correspond to the 5-finger structures with uniform spacing (s = 2.5 µm) and optimized spacing, respectively. After optimizing the spacing, we notice that the three inner transistors have more or less the same temperature avoiding electrical performance degradation and possible electro-thermal instability such as snapback and

thermal runaway.

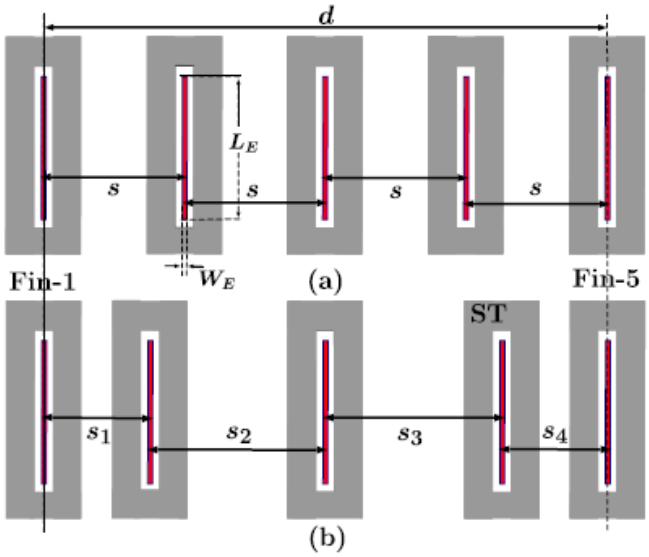

Fig. 6: Top views of the ST isolated five-finger structures with (a) uniform spacing (of s) and (b) nonuniform spacing. [Gup22]

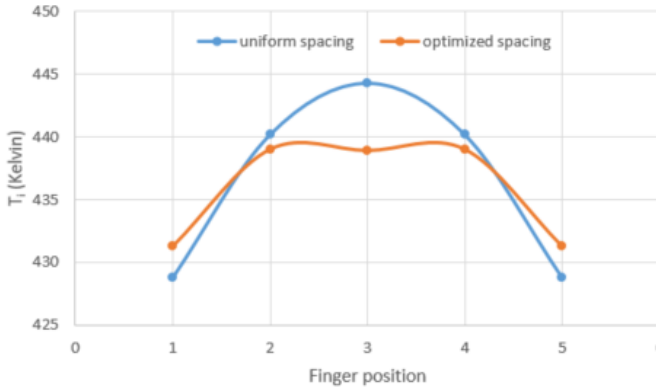

Fig. 7: Comparison of total temperature distribution. Data points in orange and blue result from structures with uniform and optimized spacing, respectively.

In [Wal02b] the problem of prediction of thermal resistance of a multifinger structure taking into account device geometry and spacing was reduced to the prediction of a thermal coupling factor. However, only an empirical approach was presented and a formal derivation of the factor is not given. The standard procedure to balance the temperature distribution is the use of ballast transistors at the emitter or base terminals, where base ballasting has been found to be more effective [Ales21]. The downside of this approach is the deterioration of the frequency performance of the device, in particular the maximum oscillation frequency f_{max}, when base ballast resistors are employed.

Another route for stabilizing the electro-thermal behavior of PA multifinger cells involves considering alternative topologies as shown in Fig. 8 [Esp16]. In fact, the test structures HL1, HL2, and HL3 aim at a more uniform temperature distribution across the emitter fingers using different strategies as described below. In test structure HL1, the three central fingers are designed shorter than the two side ones. In this way, the thermal dissipation in the center of the structure is lower than in the sides. In test structures HL2 and HL3, the length of finger-1 and finger-5, is kept the same (5 µm), but the length of fingers 2–4 is reduced to 3.91 µm, to ensure less power dissipation and thus a lower temperature in the center of the structure. In the case of HL3, this reduction has been realized with emitter segmentation. VM3 is the reference structure.

Fig. 8: Finger layout of the test structures. The DTI is shown in orange, whereas the five drawn emitter windows are colored in blue. [Esp16]. The emitter surfaces are: HL1 / VM3=4.5µm², HL2 / HL3=3.38µm²

In Fig. 9, we compare the measured current density J_C as a function of V_{CE}. For the bias point (V_{CE} = 1.42 V and V_{BE} = 0.875 V), around 18% reduction in J_C is observed from structure VM3 to HL1. At high power densities, the structures HL2 and HL3 drain an even lower J_C, and so, they seem to be favored from an electro-thermal point of view despite the fact that because of their reduced area compared to VM3, they should have a higher R_{TH}.

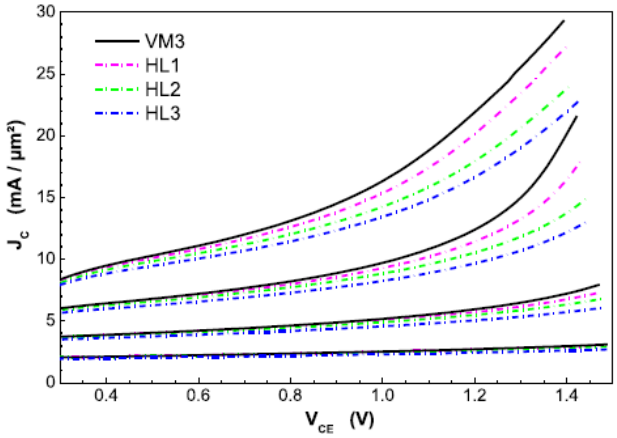

Fig. 9: Collector current density J_C for the test structures. The V_{BE} is swept from 0.825 to 0.9 V. [Esp16]

To wrap up this section, we would like to underline that non-equidistant spacing and new topologies may help to smooth the temperature distribution in PA multifinger cells. Finally, we

must mention that emitter stripe arrays are more thermally-robust if arranged in columns with an even number of unit cells [Ales21].

III. TRANSIENT AND/OR AC THERMAL BEHAVIOR

A. *Transient mode: pulsed measurements*

In order to characterize the temperature dependence of model parameters, isothermal data is desirable. This can be achieved by performing *I(V)* and *S*-parameter measurements in pulsed condition. Even if pulsed measurements may not completely eliminate self-heating, they do reduce the device temperature significantly and thus allow us *(i)* in achieving quasi-isothermal measurement data, *(ii)* in extracting an appropriate thermal resistance and capacitance network, and *(iii)* in extending the bias range towards higher voltages and current densities [Freg21]. The latter is necessary in order to verify the compact model and its extracted parameters under realistic conditions where the device characterization needs to go beyond the standard measurements. This is because most of the high-frequency applications require large signal operation, where currents and charges have to be modeled accurately over a sufficiently wide bias range. The downsides of this approach are that *(i)* the pulsed measurement setup (to obtain pulsed *I(V)* and pulsed *S*-parameters) is sufficiently complicated, *(ii)* all "parasitics" such as coaxial cables, bias-tees are required to be meticulously modeled, and *(iii)* the measurement windows have to be methodically chosen.

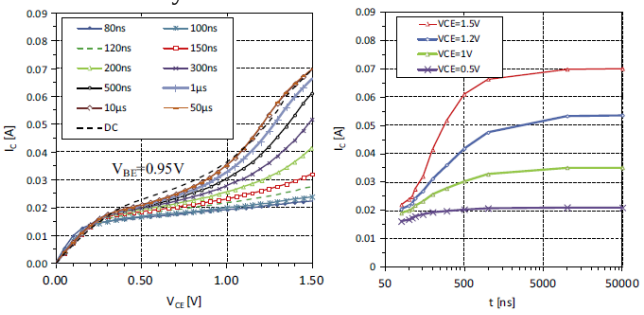

Fig. 10: Output characteristics for V_{BE} = 0.95 V measured with various pulse widths from 80 ns up to 50µs [Wei13]

Fig. 10 on the left shows pulsed output characteristic for a given V_{BE} and different pulse widths. In fact, choosing one V_{CE}, one can plot the increasing collector current with increasing pulse width (see Fig. 10 on the right). We recognize that even for the smallest pulse width (80ns), the current is already increasing (even shorter pulses are necessary to obtain isothermal behavior). However, here the impact of self-heating is limited (see the lowest curves in the characteristic on the left). Nonetheless, these data are extremely useful to obtain an appropriate R_{TH}-C_{TH} network.

B. *AC mode: small-signal S-parameter measurements and Z_{TH} extraction*

An alternative approach of characterizing the thermal impedance is the use of *S*-parameter measurements in the low frequency range (e.g. 30kHz to 3GHz). The measurement setup is straightforward and it is easy to obtain accurate results. In this frequency range only the thermal response of the HBT is playing a role provided that no traps are present, which is usually the case in matured SiGe HBT technologies. The theoretical framework linking *S*-parameter to Z_{TH} is well established [Rin01], where we can find the theoretical foundations for the frequency-domain thermal characterization of *RF* transistors from low-frequency y-parameters. In this method, a prior information on the value of R_{TH} is needed which can be obtained applying the method described in section II-A. Fig. 11 illustrates the obtained thermal impedance as a function of frequency for devices having different emitter dimensions. From these results, an electro-thermal model can be adapted, a scalable model can be developed and the R_{TH} consistency can be checked thanks to the concept of thermal penetration depth [Bal19].

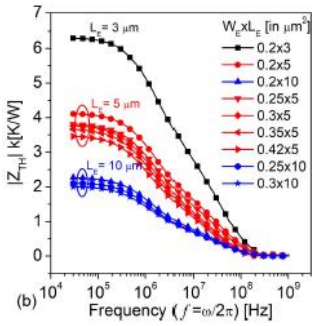

Fig. 11: $|Z_{TH}(\omega)|$ extracted from S-parameter measurements for devices with different emitter geometries [Bal19]

C. *Analytical and SPICE compatible models for Z_{TH} from the heat transfer equation*

In most of the commercial simulator models, the dynamic device temperature rise is incorporated using an electro-thermal equivalent circuit, where a current source (representing the dissipated power inside the transistor) is connected in parallel to a capacitor (C_{TH}) and a resistor (R_{TH}). The voltage across the current source reflects the temperature rise inside the transistor. The corresponding thermal impedance in Laplace domain is given by

$$Z_{TH}(p) = \frac{R_{TH}}{1 + pR_{TH}C_{TH}} \tag{10}$$

This model is a simplified form of the generalized thermal equivalent circuit composed by 'n' number of C_{TH}-R_{TH} pairs and is not very useful for modelling purposes due to the large number of nodes. A compact formulation has been proposed by solving the heat diffusion equation assuming a cylindrical symmetry - a rough approximation for long emitter strips - and it reads [Mni02]

$$Z_{TH}(p) = \frac{R_{TH}}{1 + \sqrt{p}\sqrt{R_{TH}C_{TH}}} \tag{11}$$

The $\sqrt{p}$ behavior is known as fractional model and these models are commonly approximated using electrical Foster or Cauer type networks. In order to accelerate the convergence and to minimize the number of parameters, recursive Cauer type network has been introduced as shown in Fig. 12 [Wei13]. Moreover, it permits to match the measured phase of the thermal impedance Z_{TH} [31].

Fig. 13 depicts the accuracy obtained from the recursive

network compared to that from a single C_{TH}-R_{TH} network. The recursive thermal network provides the better agreement not only in the frequency domain but also in the time domain (see [Wei13], not shown here). In general, three C_{TH}-R_{TH} pairs are sufficient to cover the frequency range to ensure accurate electro-thermal modelling of SiGe HBTs.

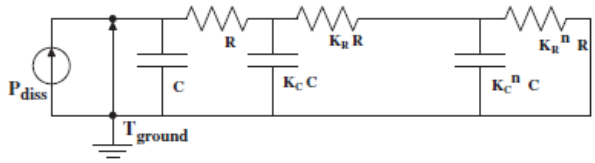

Fig. 12: n-cell recursive Cauer-type thermal network. [Wei13]

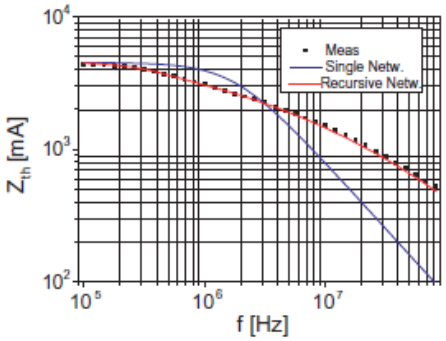

Fig. 13: Magnitude of the thermal impedance ZTH versus. frequency using single pole and recursive network. [Wei13]

IV. Conclusion

This paper reviewed some relevant topics for electro-thermal investigation of SiGe HBTs in static and dynamic regime. Thermal resistance determination has been discussed first, followed by its analytical description. Combining these results, the BEOL contribution could be estimated. Moreover, optimum emitter finger topologies for PA-cell design has been presented. Finally, the thermal impedance measurement using pulsed measurement equipment or *S*-parameter measurements have been discussed and modelling aspects have been reviewed.

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