

What causes the fluctuations in f_{\max} with respect to frequency?

T. Zimmer, T. Bouzar, J.D. Arnould, S. Fregonese



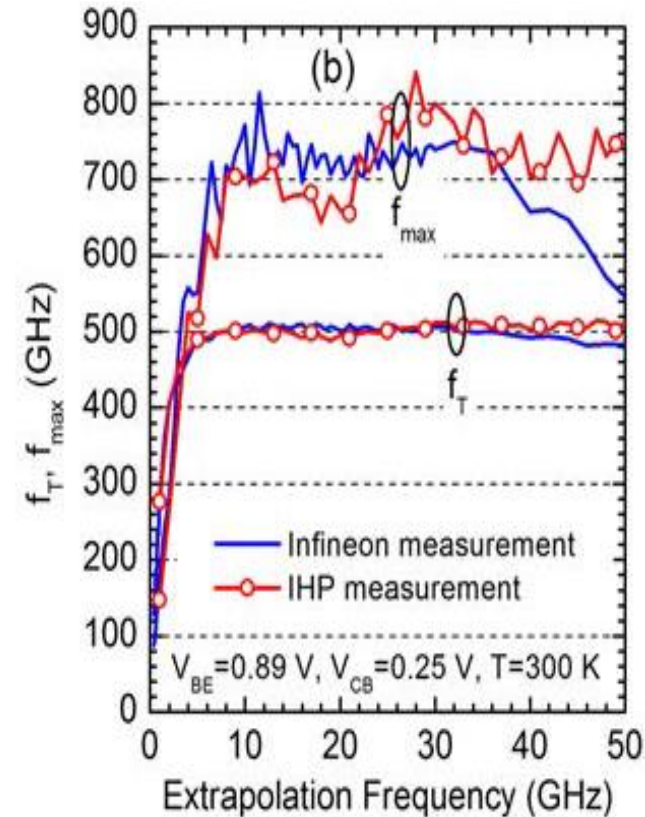
Laboratoire de l'Intégration du Matériau au Système

BipAK 2023

Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement

- ▶ f_{MAX} is a FOM that is difficult to measure : same device measured at IHP and Infineon

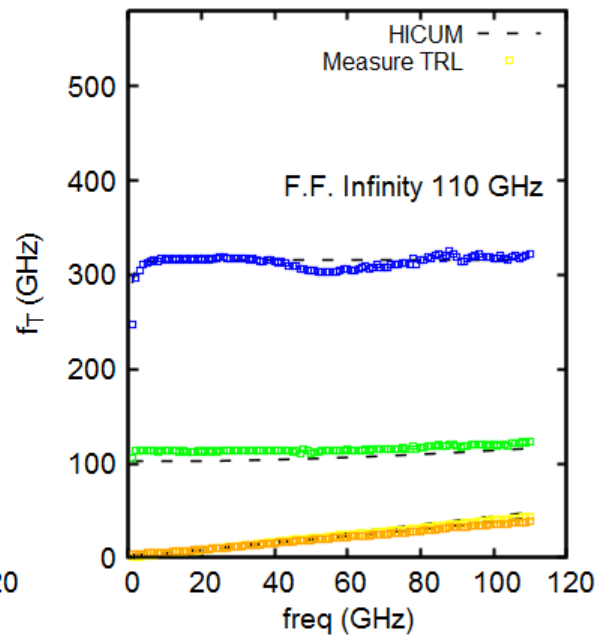
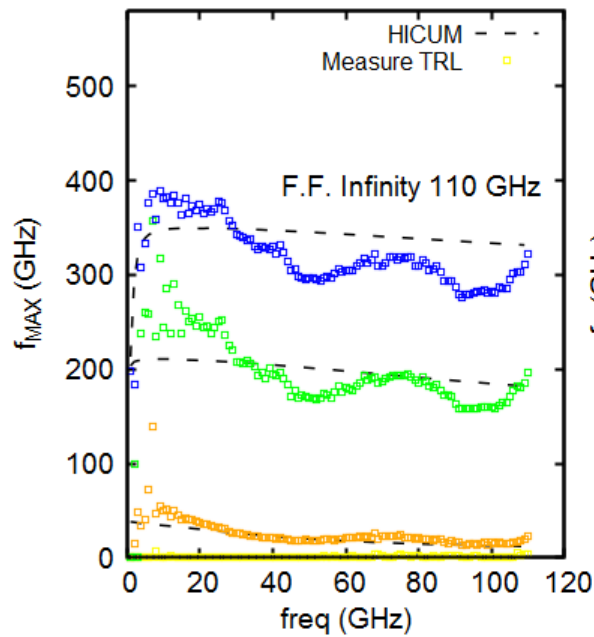


B. Heinemann *et al.*, « SiGe HBT with f_x/f_{max} of 505 GHz/720 GHz », in 2016 *IEEE IEDM*, déc. 2016

Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement

- ▶ f_{MAX} is a FOM that is difficult to measure : same device measured at IHP and Infineon
- ▶ What about our result on STMicroelectronics B55 technology

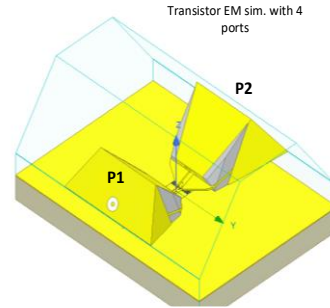
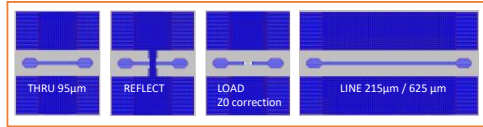


How to analyse the results ?

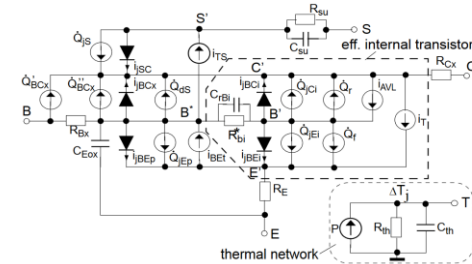
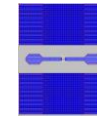
Impact of test structure and probes on calibration ?

Simulation methodology => reproduce the measurement procedure

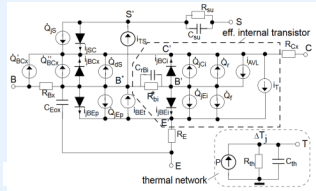
TRL



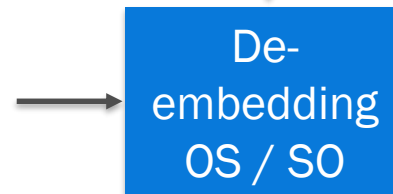
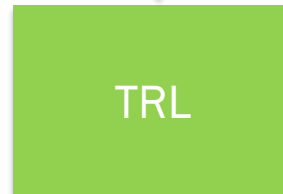
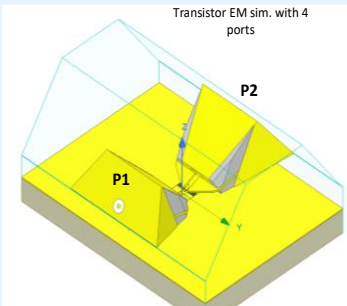
open / short



TRANSISTOR
EM sim. + SPICE
simulation



Transistor EM sim. with 4 ports

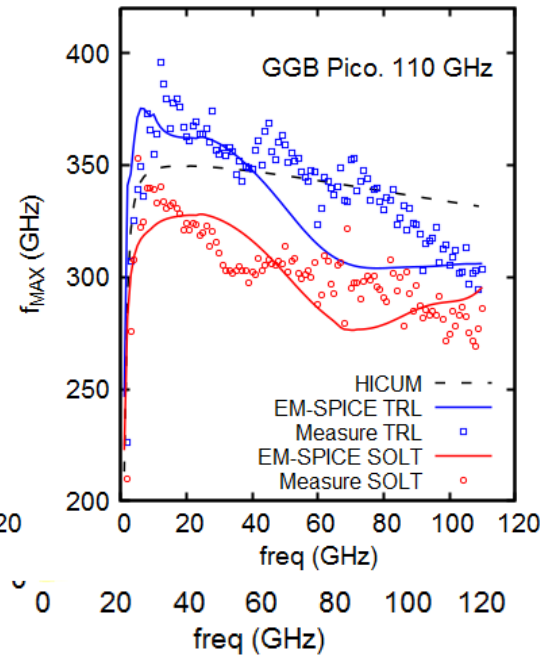
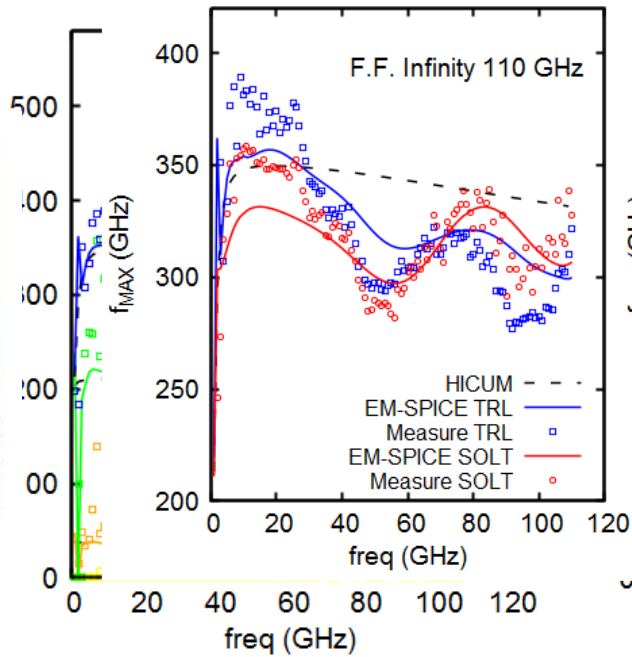


Does cal. + deemb. allows to recover intrinsic characteristics ?

Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement

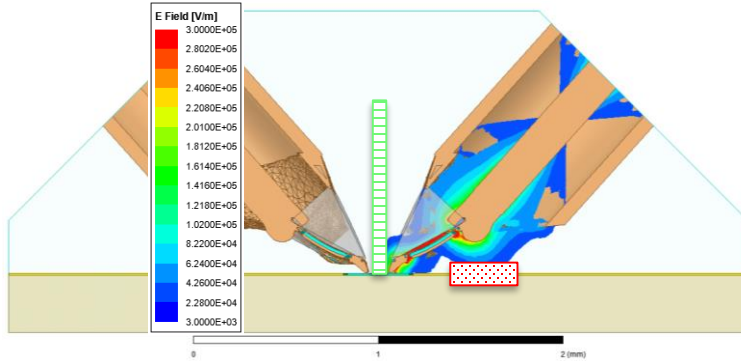
- ▶ f_{MAX} is a FOM that is sensitive to calibration accuracy
- ▶ Example of TRL calibration result on STMicroelectronics B55 technology



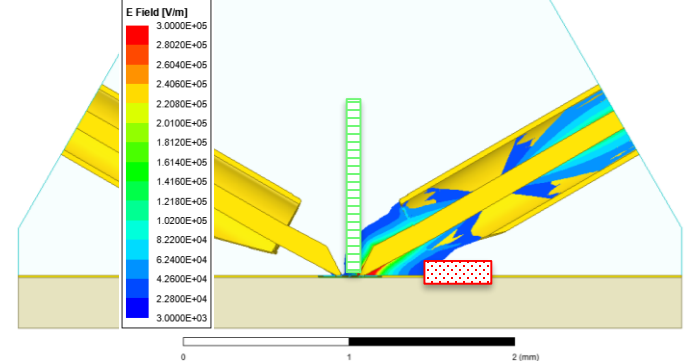
Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement

Example of probe crosstalk with inter-probe distance of $\sim 140\mu\text{m}$

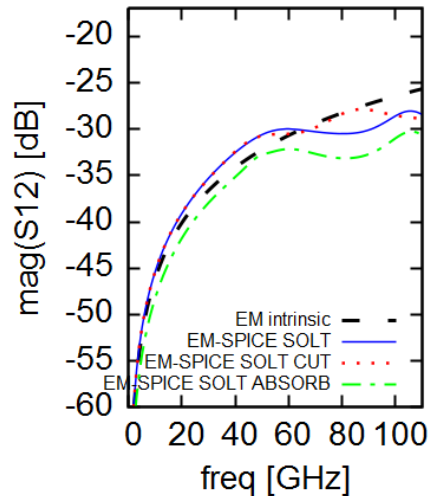


Infinity probe ($100\mu\text{m}$ pitch)
on a trans-open, freq = 60 GHz

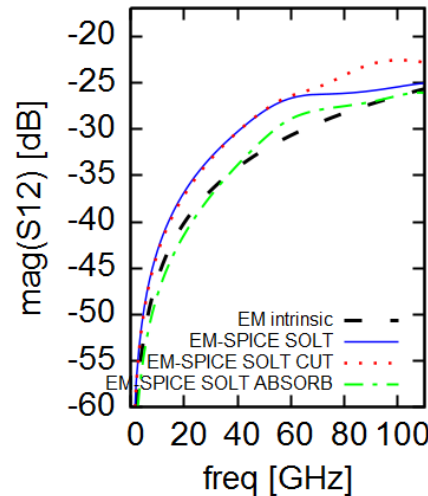


Pico-probe ($100\mu\text{m}$ pitch)
on a trans-open, freq = 60 GHz

F. F. Infinity 110 GHz



GGB Pico. 110 GHz



\Rightarrow probe couplings has a strong impact ! (not corrected by SOLT / TRL)



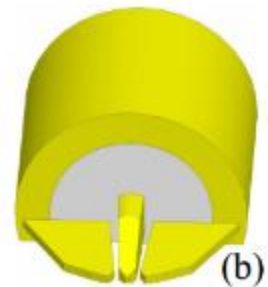
Where is the way out?

- All S-parameters above 40 to 50 GHz are unaccurate, that is to say, they are affected by not-corrected coupling
- How to solve the issue
 - New probes with appropriate test-structures
 - New calibration method with appropriate test-structures

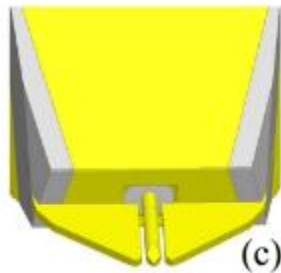
Impact of test structure and probes on calibration ?

Impact of calibration/probes on FOM measurement : measurement up to 500 GHz & discontinuities

- Advanced probe models are required to understand measurement imperfections

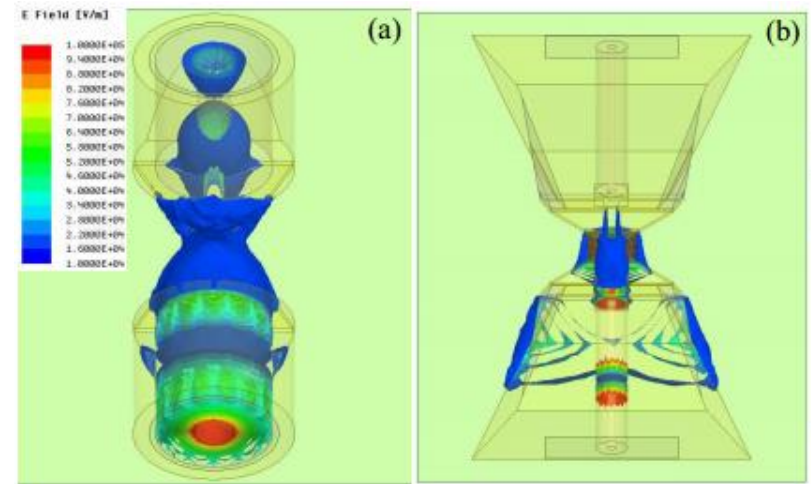
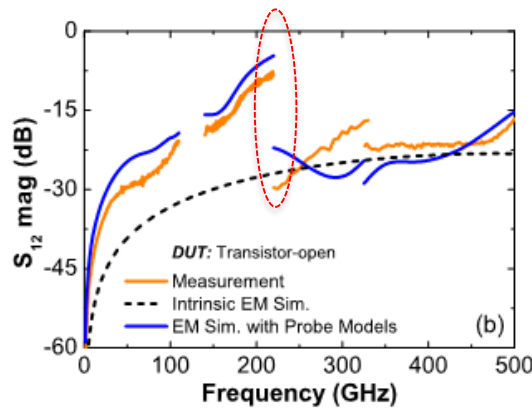


140-220 GHz



220-325 GHz

@ 220 GHz

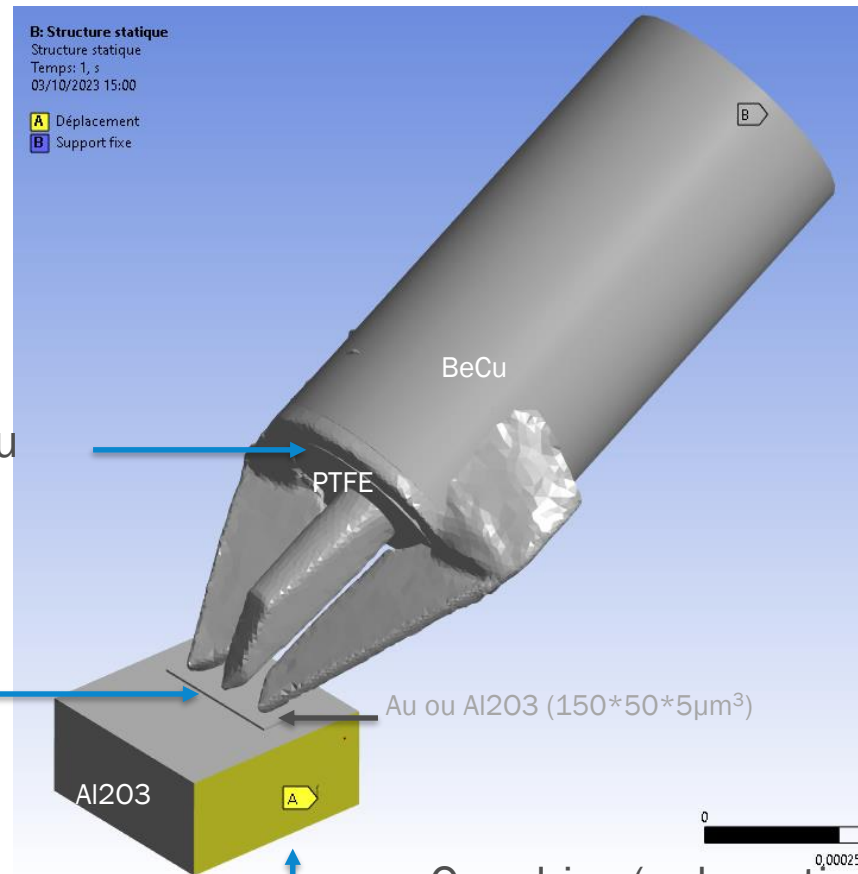


Electric field (E-field) distribution (top and side views) in the transistor-open at 220 GHz using two probe models



- Inter-pad distance needs to be increased
- Probes need to be downscaled to reduce the probe to substrate coupling

Ex: GGB pico 110 GHz



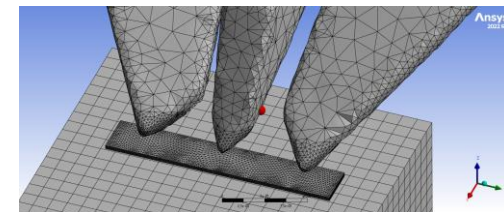
Materials

1- PTFE / BeCu

2- Au / Al2O3

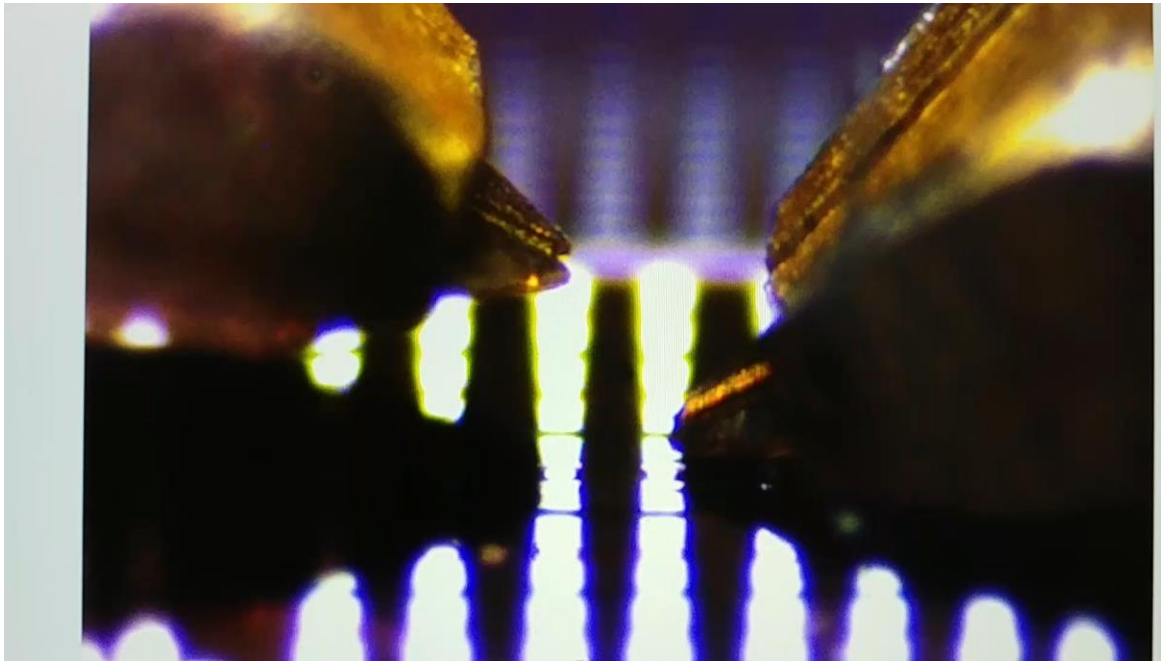
Sliding link between probe and Au

3D model



Overdrive (only vertical direction)

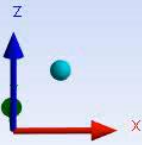
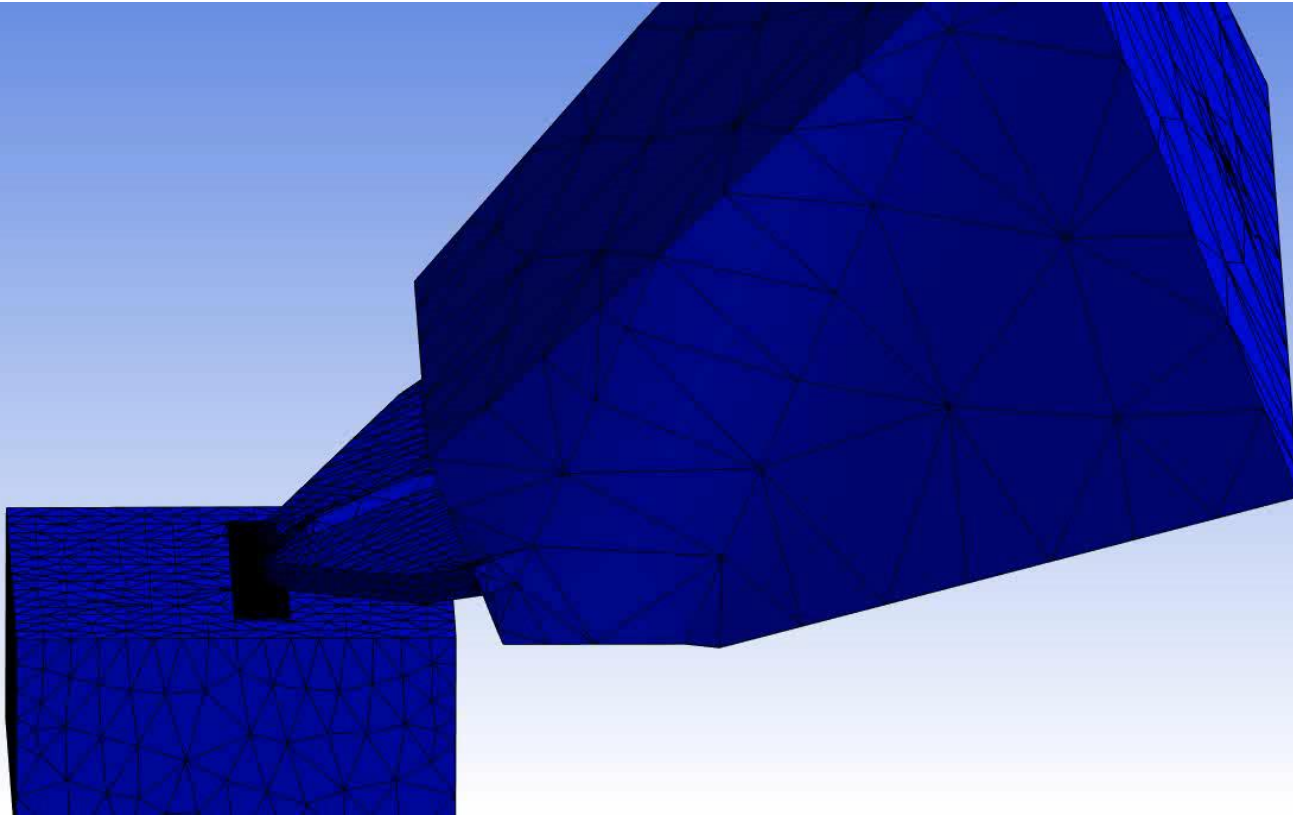
Side view movie showing skating and probe bending: GGB 325 GHz probe



Side view simulation showing skating and probe bending: GGB 325 GHz

Ansys
2022 R2

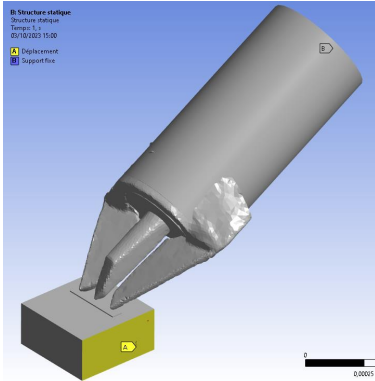
B: Structure statique
Déplacement directionnel 2
Type: Déplacement directionnel(Axe Z)
Unité: m
Système de coordonnées global
Temps: 1 s
09/10/2023 14:14



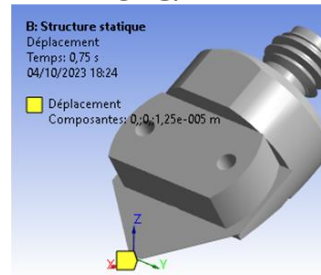
WP2: Mechanical simulation of our MEMs probe

Comparison to commercial probes (GGB)

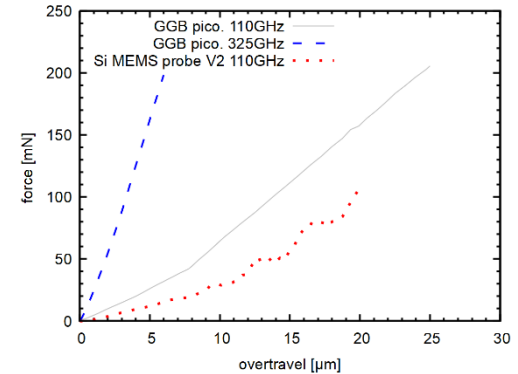
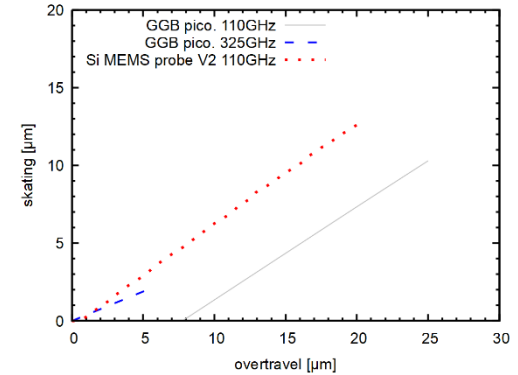
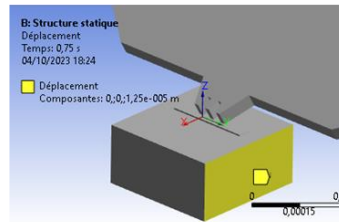
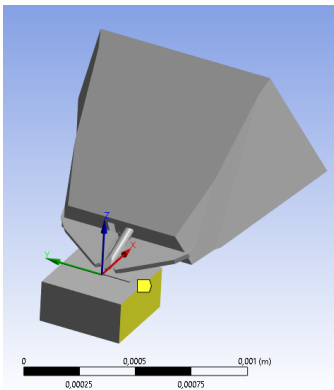
GGB Pico 110 GHz



Si MEMS probe V1 (ANR Precise) 110 GHz



GGB Pico 325 GHz

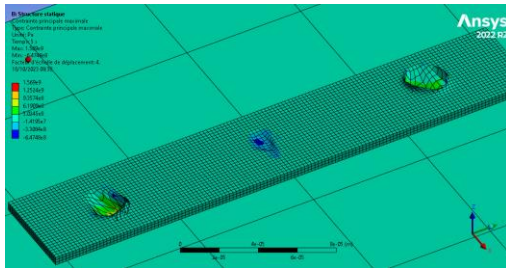


WP2: Mechanical simulation of our MEMs probe

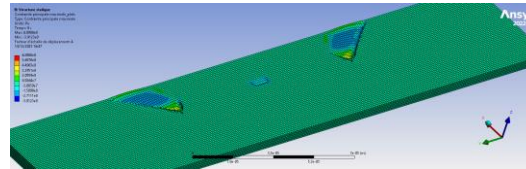
Evaluation of contact resistance through simulation

« Scratches » simulated using mechanical simulation

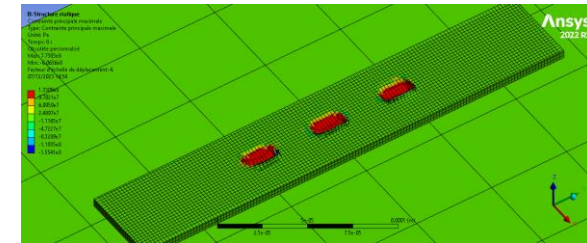
Trace créée par la sonde GGB Pico 110 GHz avec 25µm d'overtravel, agrandissement **x4 (simulation)**, pitch sonde =100µm



Trace créée par la sonde GGB Pico 325 GHz avec 6µm d'overtravel, agrandissement **x4 (simulation)**, pitch sonde =100µm

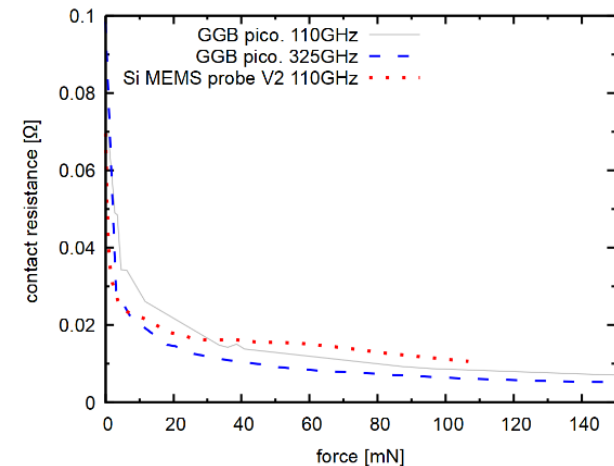


Trace créée par la sonde PRECISE V2 avec 20µm d'overtravel, agrandissement **x4 (simulation)**, pitch sonde =50µm



Using the surface of the scratches and a contact resistivity one can estimate contact resistance versus overtravel

- Simulation is consistent with analytical eq. $R = \rho \sqrt{\frac{\pi H}{4F}}$
 - H is hardness of Au pad
 - F is the applied force
 - ρ the resistivity



New probe design (ANR Precise)

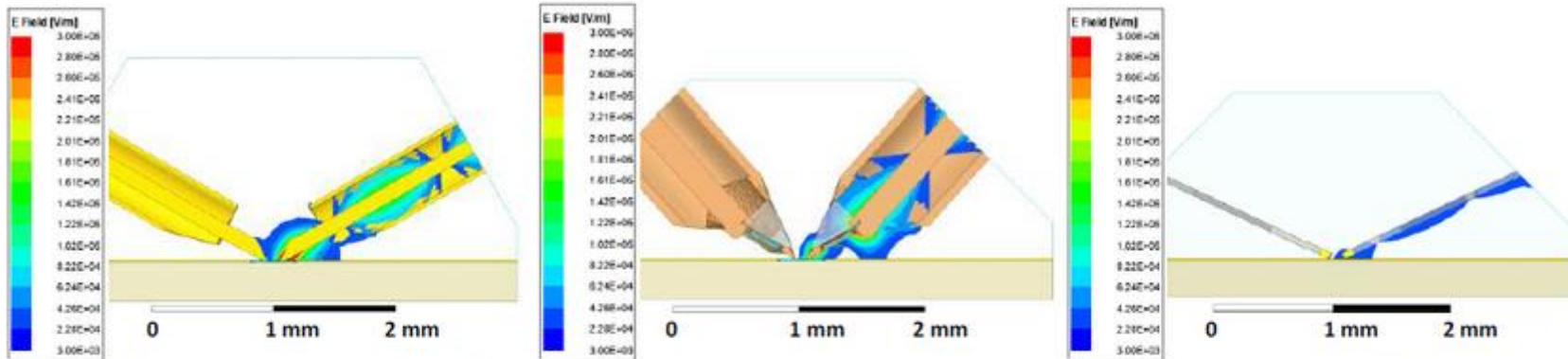


Fig. 6 Field distribution highlighting probe to substrate coupling @ 60 GHz (phase of Efield showing strongest coupling) on a load – same scale is used for each simulation (Picoprobe, Infinity, our solution).

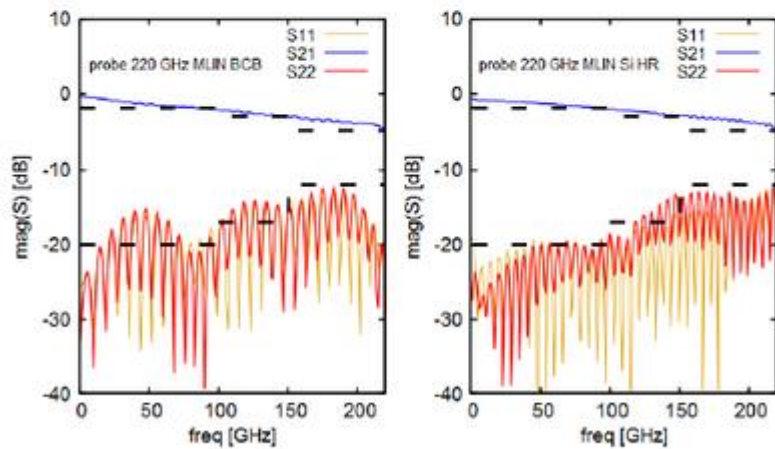


Fig. 7a : Simulation results of probe

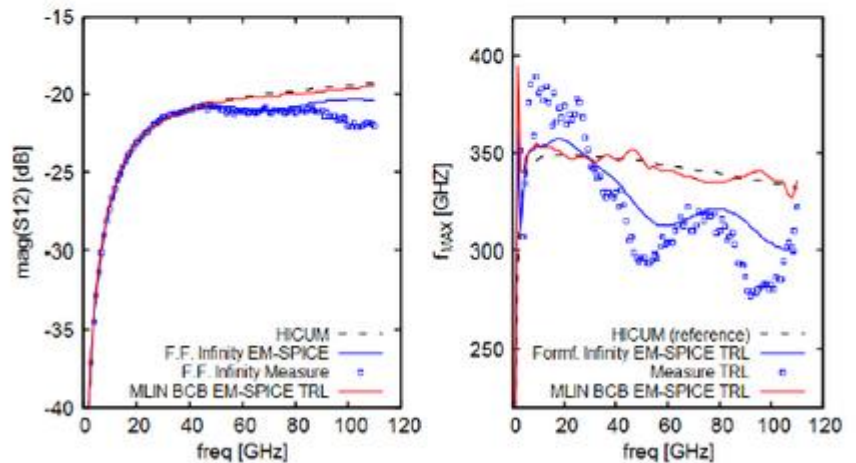
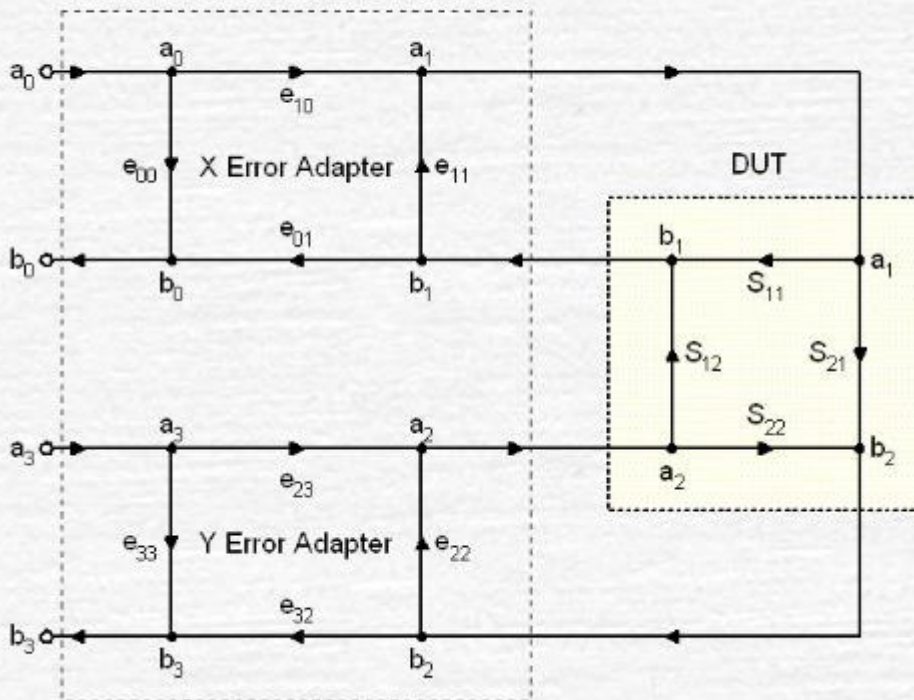


Fig. 7b: Emulation of measurement of a B55 transistor (BiCMOS 55nm) using Infinity probe and our probe

New calibration method? Revisite 16 terms

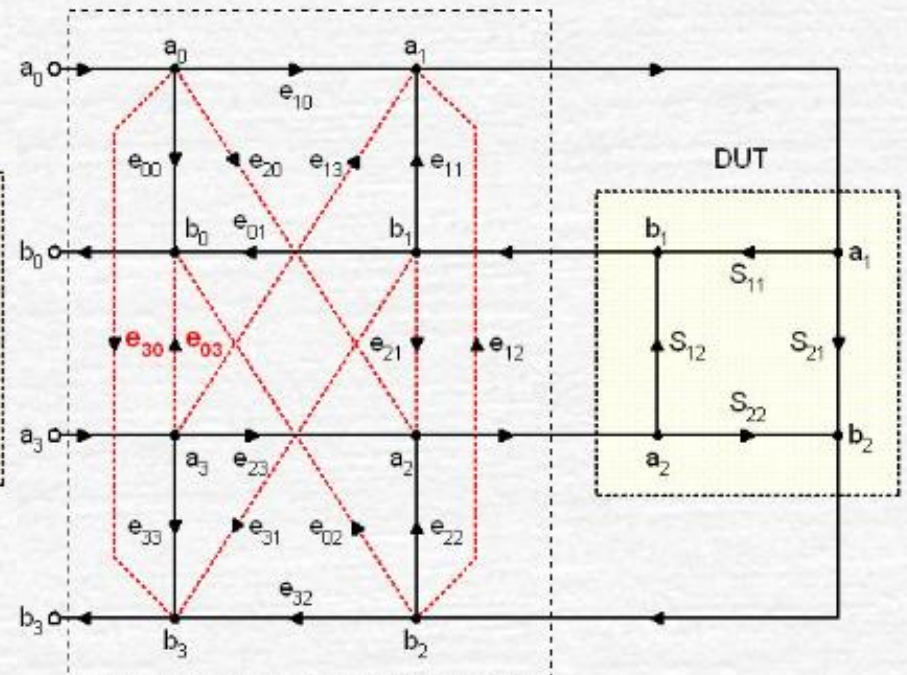
8 terms vs 16terms calibration

8-Term Error Model



One of the 8 error terms can be normalized to yield 7 error terms

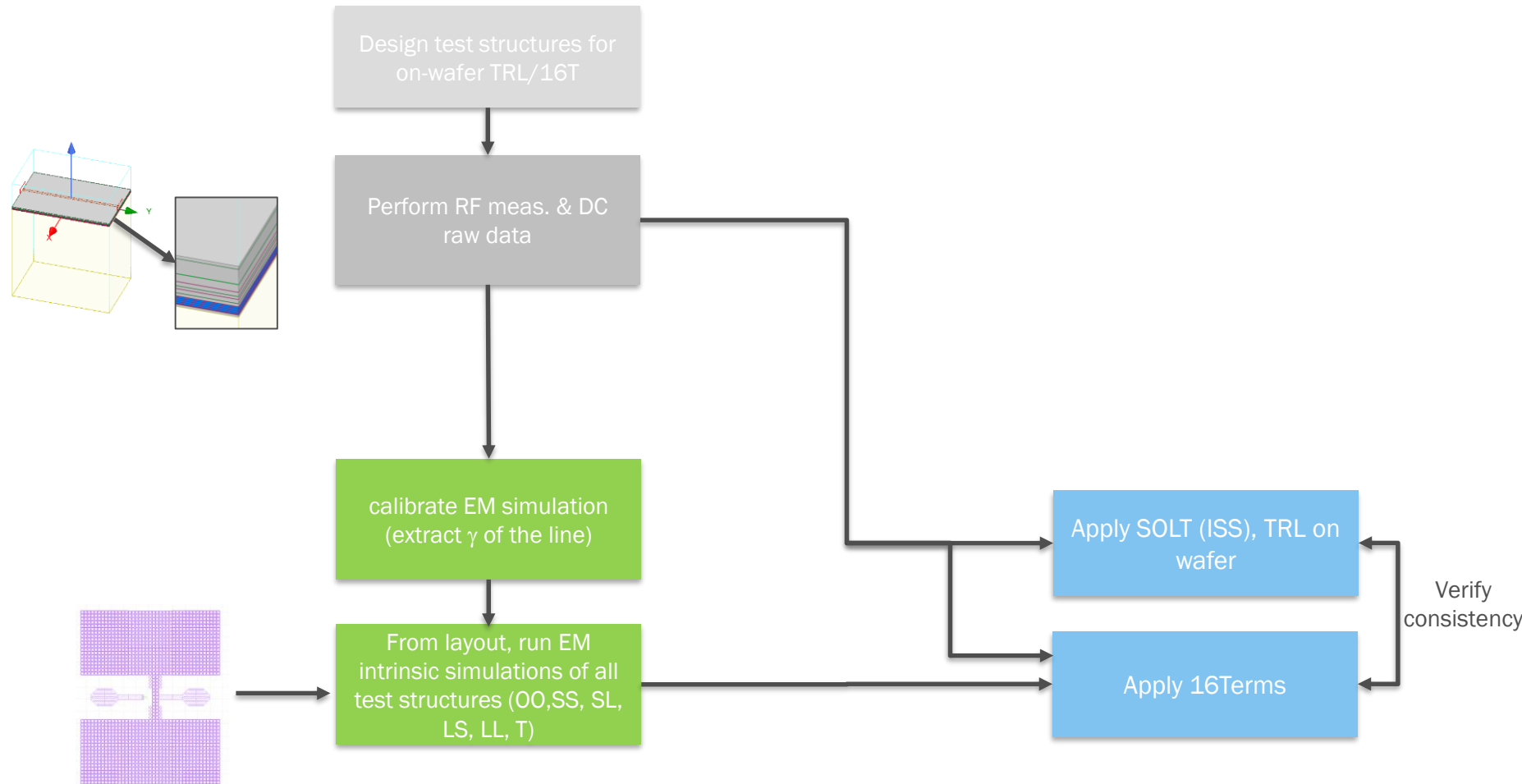
16-Term Error Mod



One of the 16 error terms can be normalized to yield 15 error terms

New calibration method? Revisit 16 terms

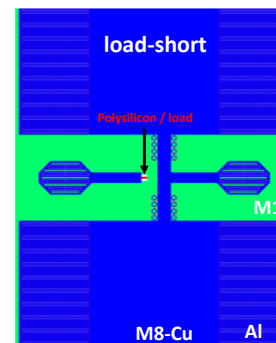
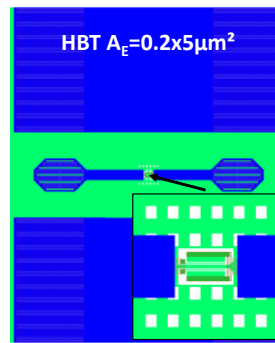
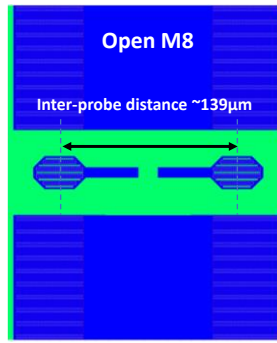
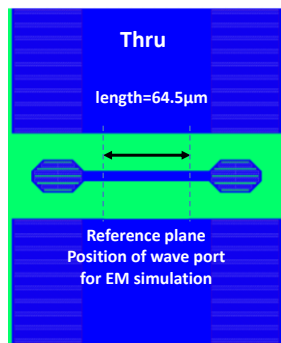
16T calibration methodology



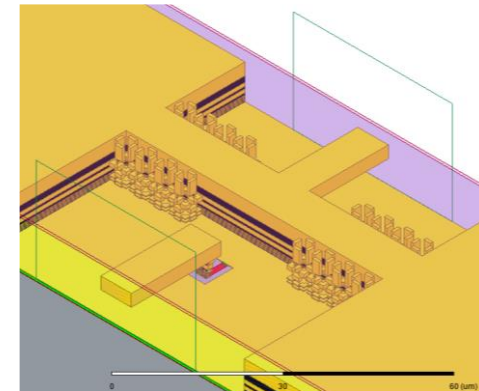
New calibration method? Revisite 16 terms

Test structures needed

- ▶ 6 Test structures are used for calibration
 - ▶ At least 5 test structures are needed and one calibration test structure needs to be asymmetric
 - ▶ Thru, load-load, open-open, short-short
 - ▶ Load-short , short-load

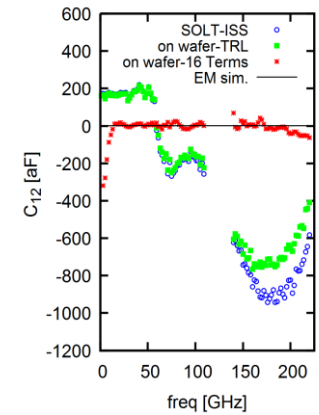
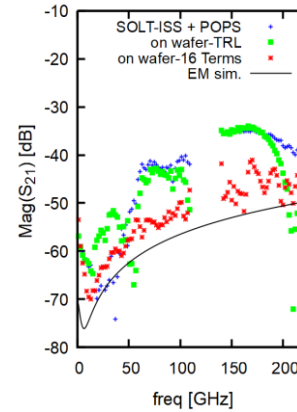
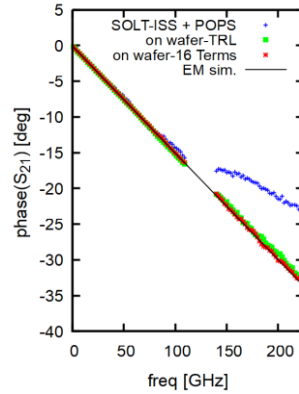
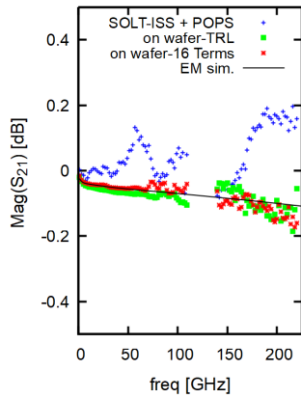
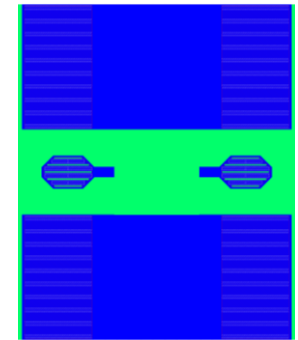
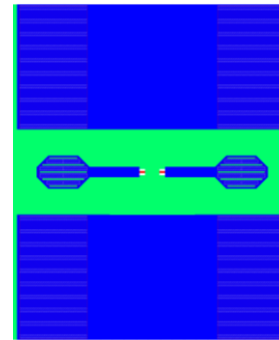
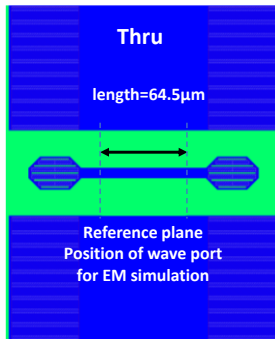


EM simulation of the load-short



New calibration method? Revisite 16 terms

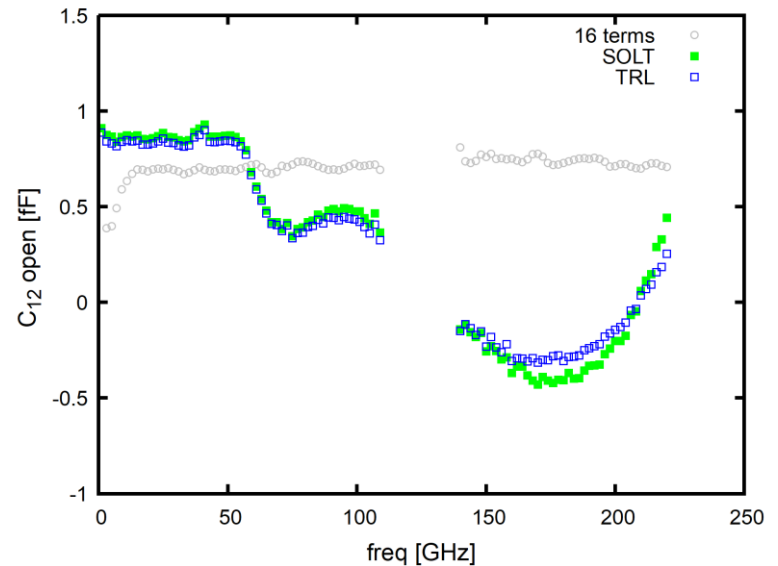
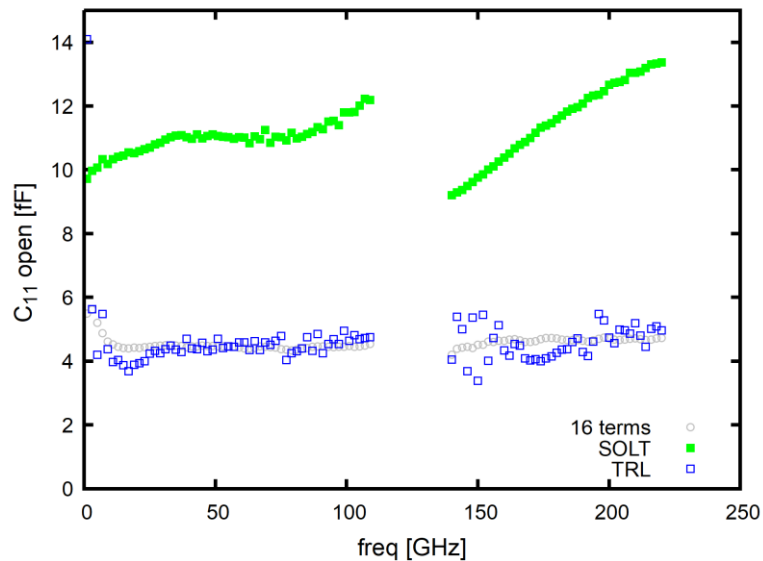
Verification of the standard measurements



16T results

Transistor-open

- ▶ Transistor open measurement:
 - ▶ SOLT ref. plane is at the tips
 - ▶ TRL and 16 terms have reference plane after the pads

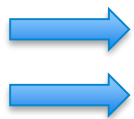
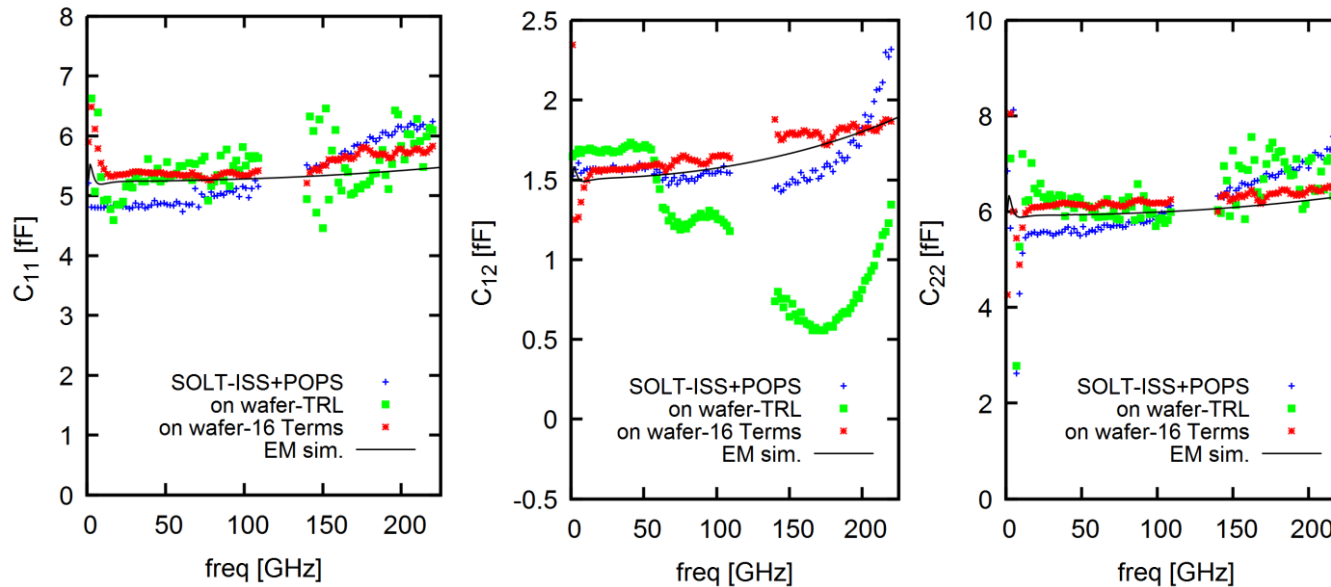


16T results

Transistor-open

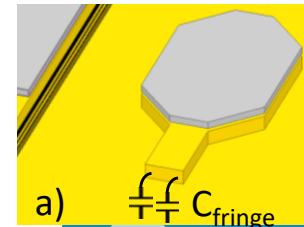
Transistor open measurement:

- Pad-open/Pad-Short is applied to SOLT data
- SOLT, TRL and 16 terms have reference plane after the pads



Pad-open/Pad-Short improves C_{12} accuracy (crosstalk is partially corrected)

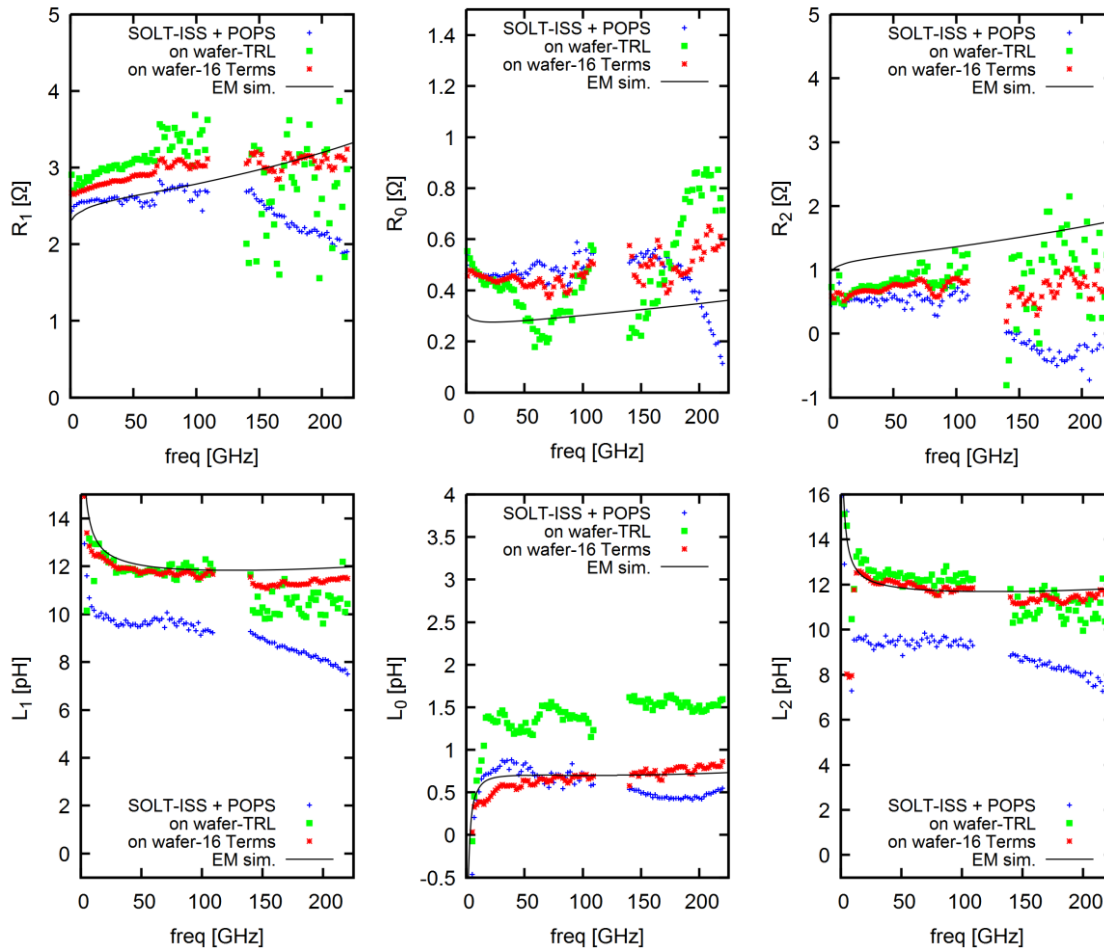
Pad-open/Pad-Short leads to over-dembedding on C_{11}/C_{22} due to fringe capacitance which does not exist when device is connected



16T results

Transistor-short

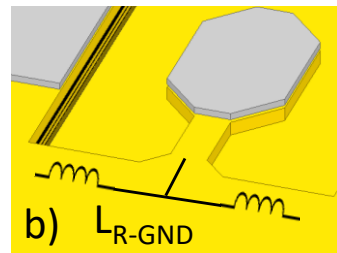
- Transistor short measurement:
 - SOLT, TRL and 16 terms have reference plane after the pads



Pad-open/Pad-Short improves LO accuracy



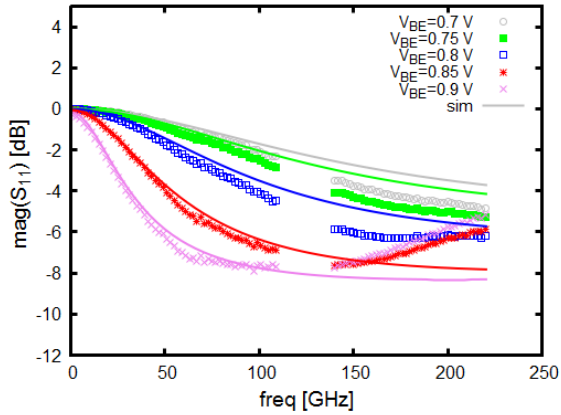
Pad-open/Pad-Short leads to over-dembedding on L1/L2 due to LR/GND which does not exist in transistor configuration



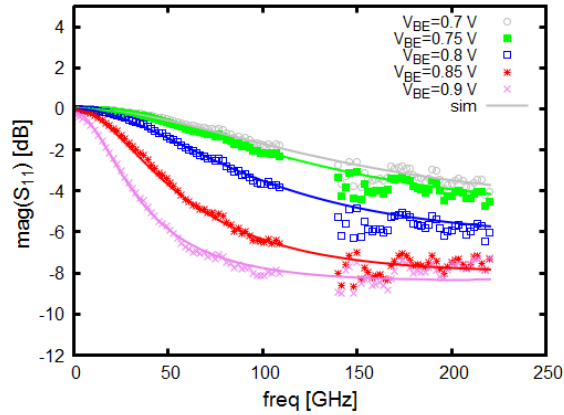
16T results

Transistor measurements

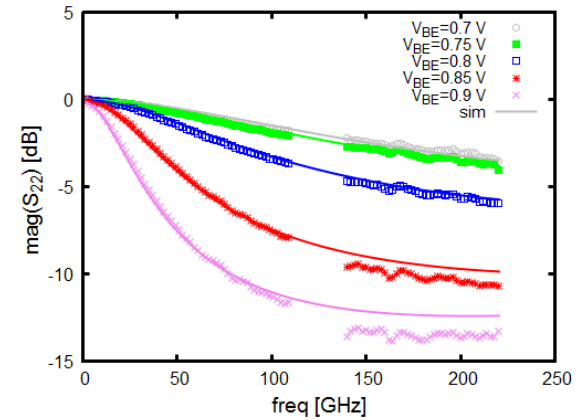
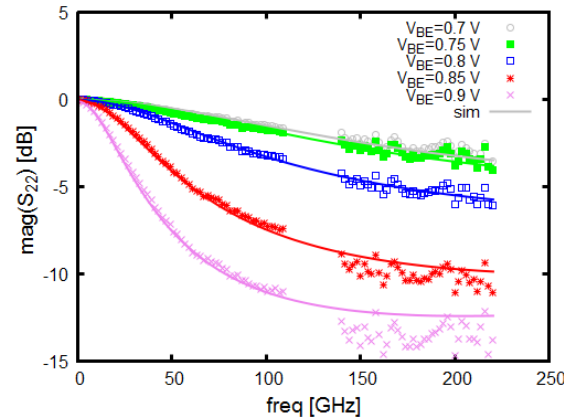
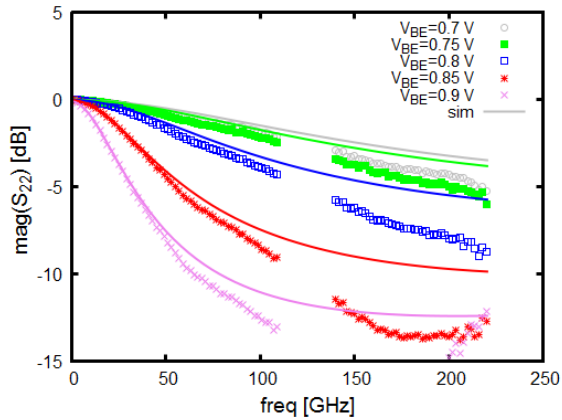
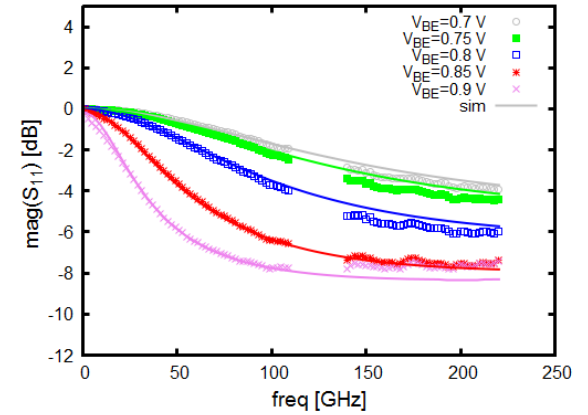
ISS SOLT calibration
+ OS deemb



On wafer TRL calibration
+ OS deemb



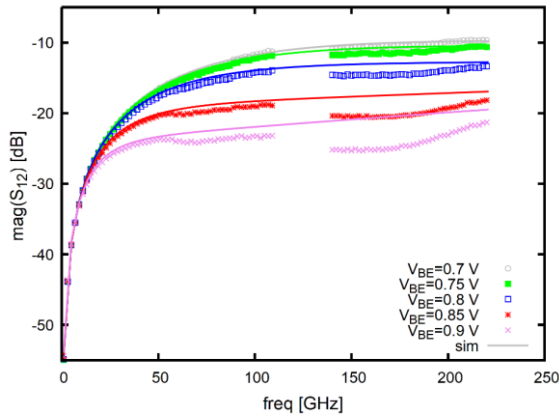
On wafer 16 terms calibration
+ OS deemb



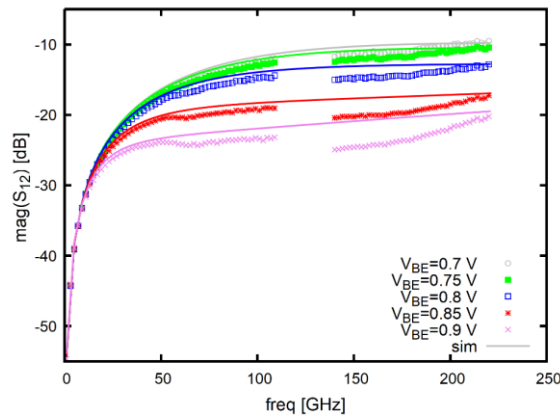
16T results

Transistor measurements

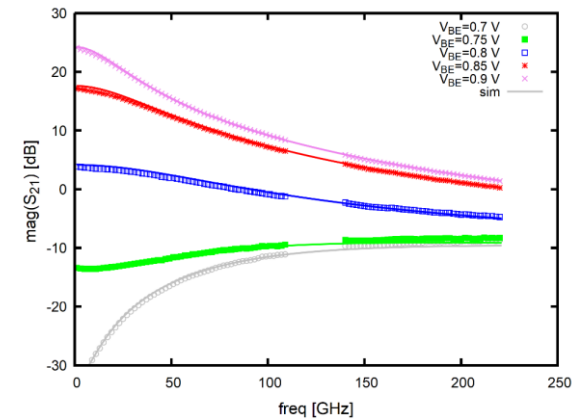
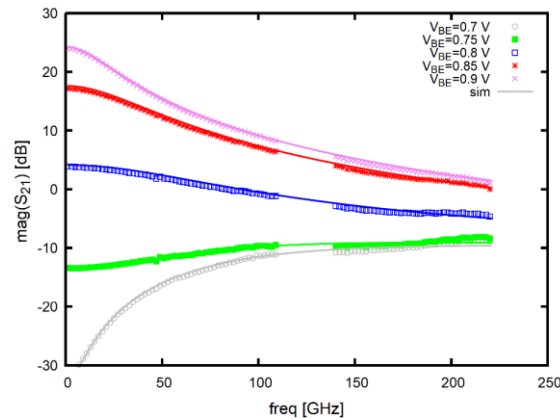
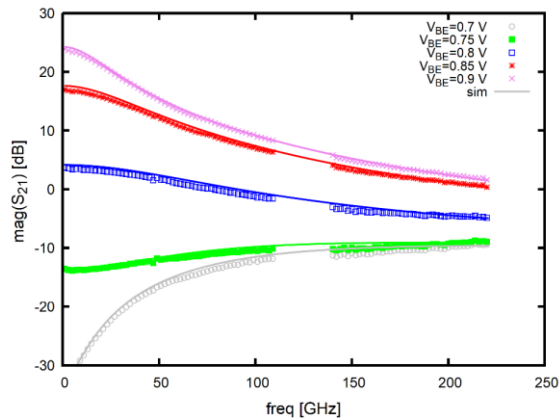
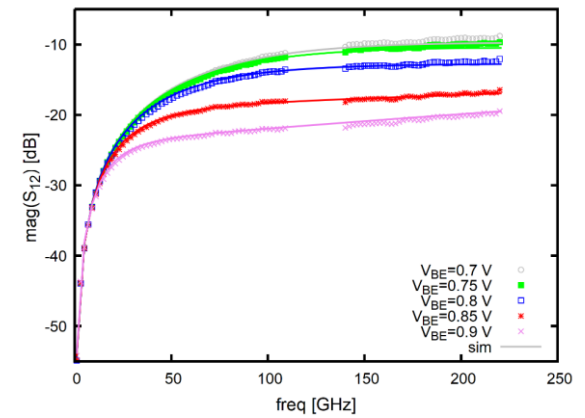
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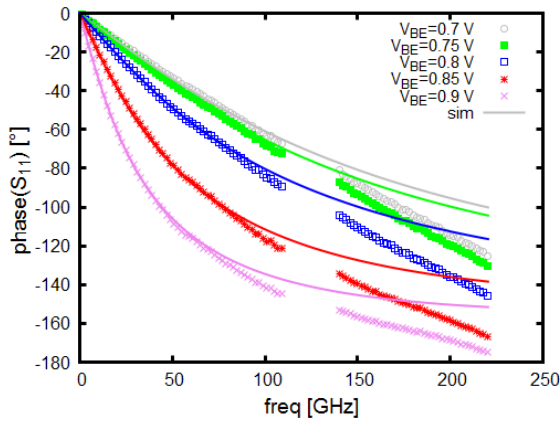
On wafer 16 terms calibration
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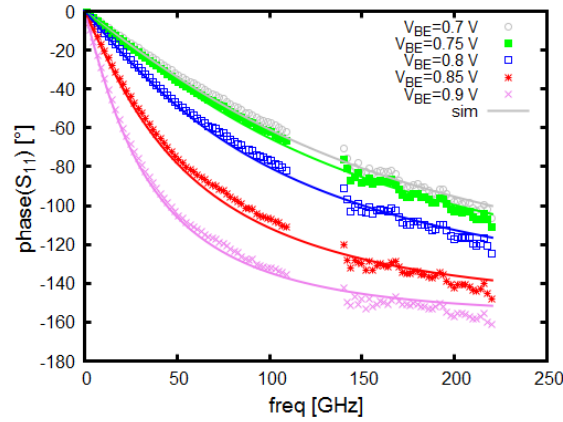
16T results

Transistor measurements

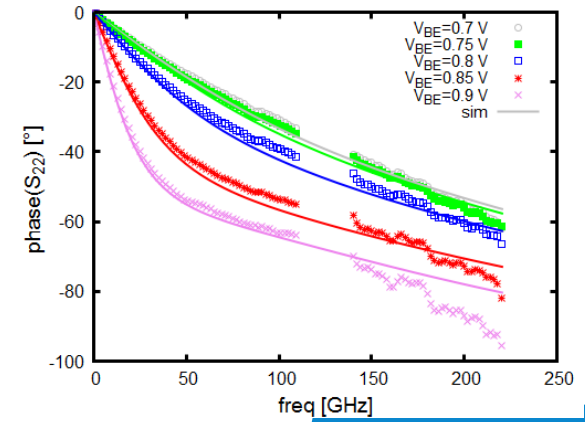
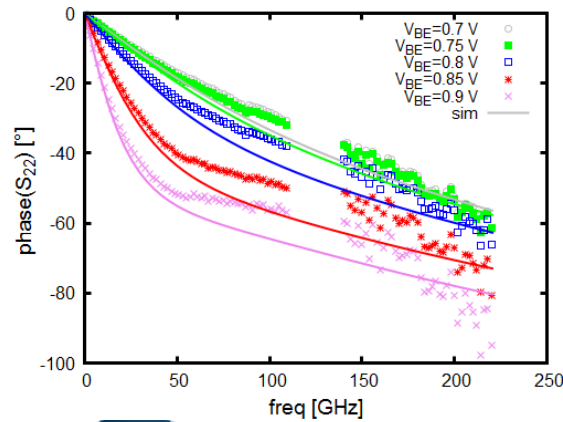
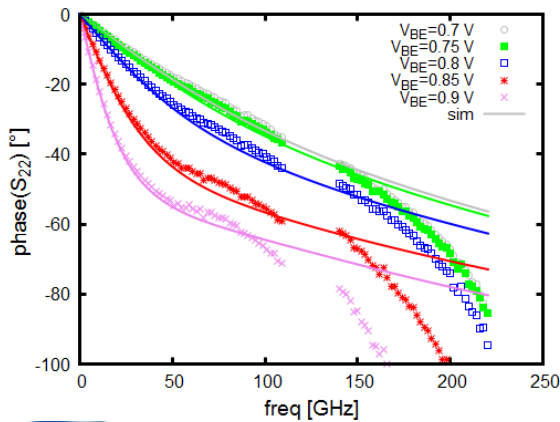
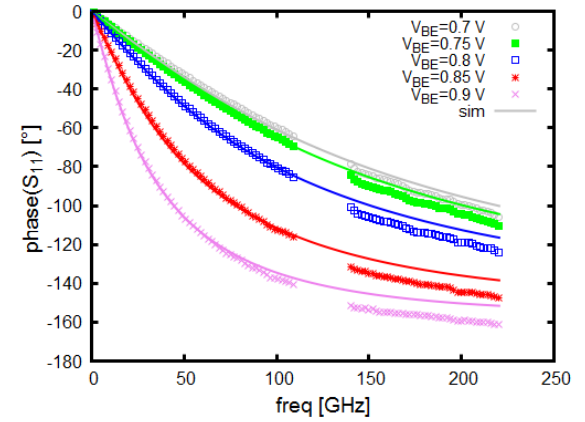
ISS SOLT calibration
+ OS deemb



On wafer TRL calibration
+ OS deemb

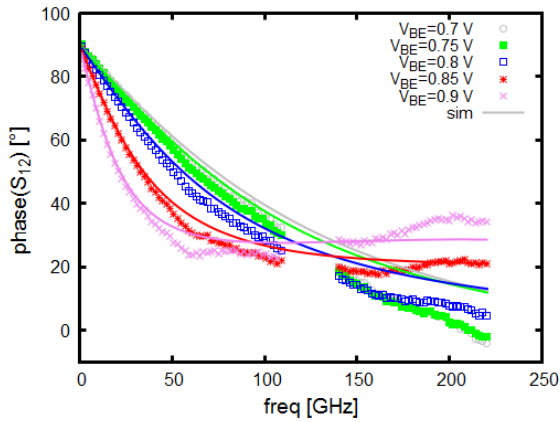


On wafer 16 terms calibration
+ OS deemb

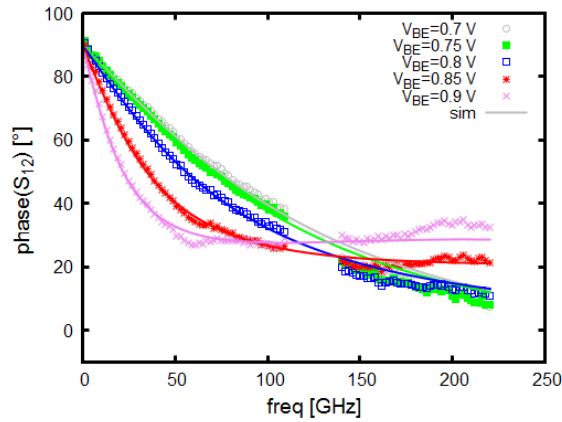


Transistor measurements

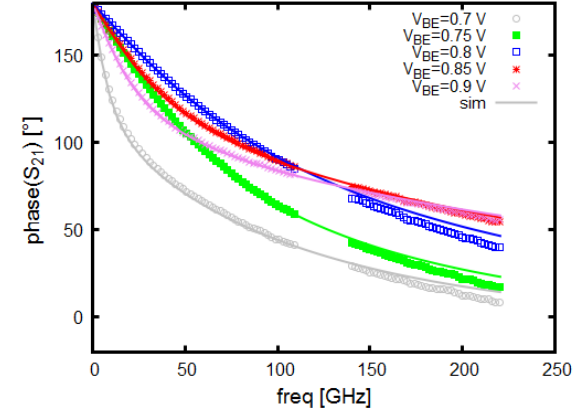
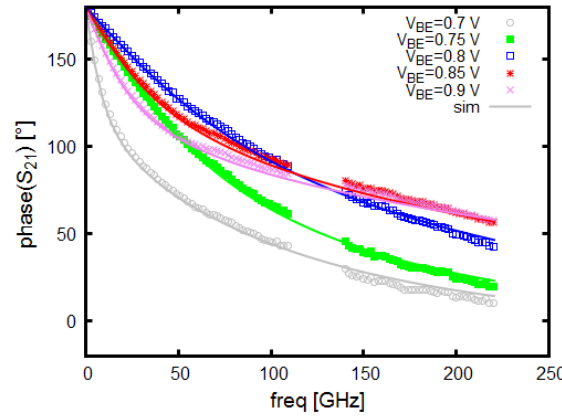
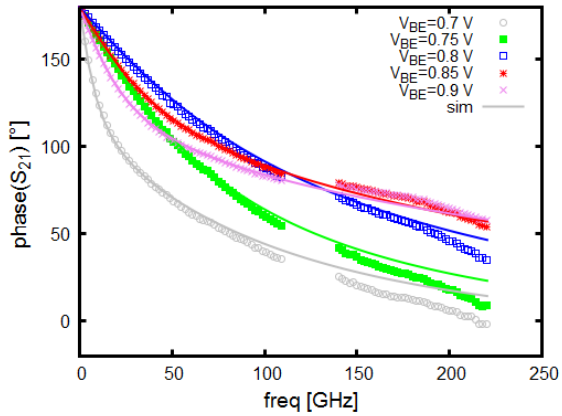
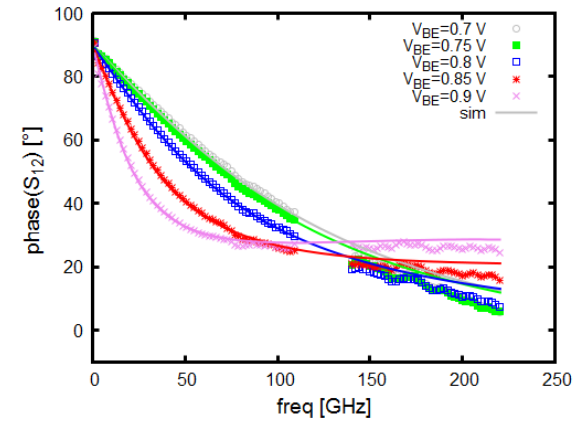
ISS SOLT calibration
+ OS deemb



On wafer TRL calibration
+ OS deemb

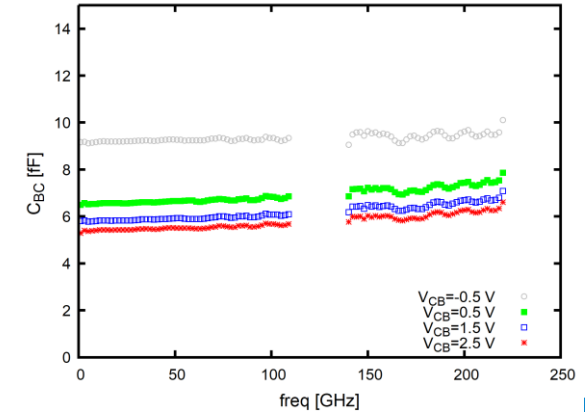
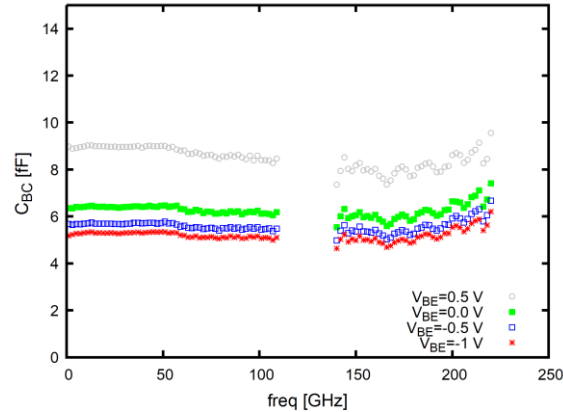
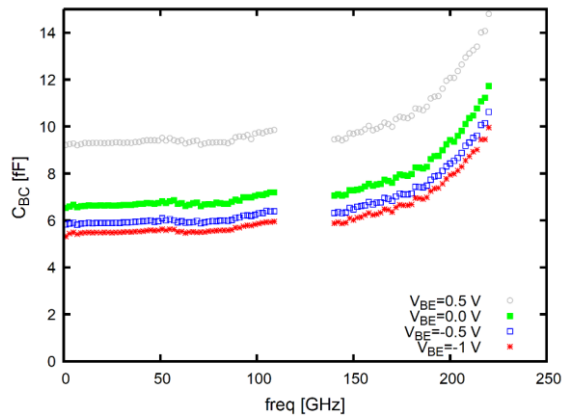
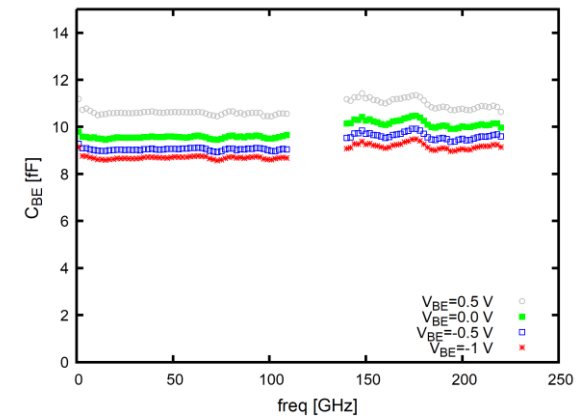
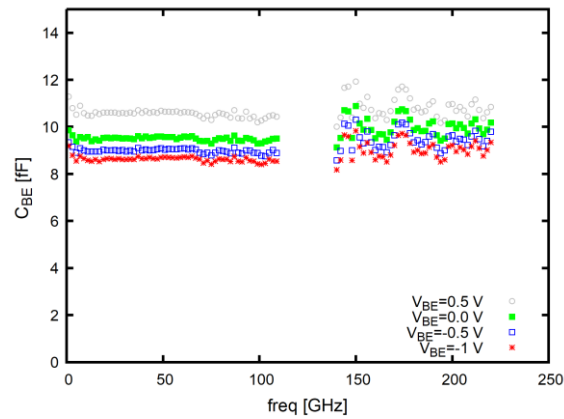
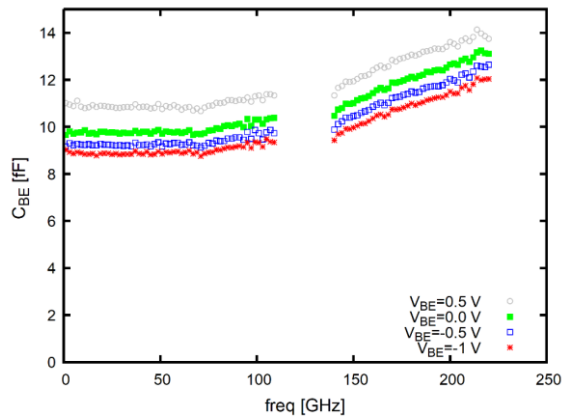


On wafer 16 terms calibration
+ OS deemb



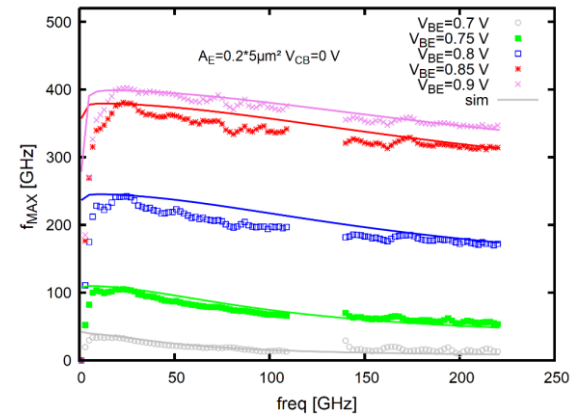
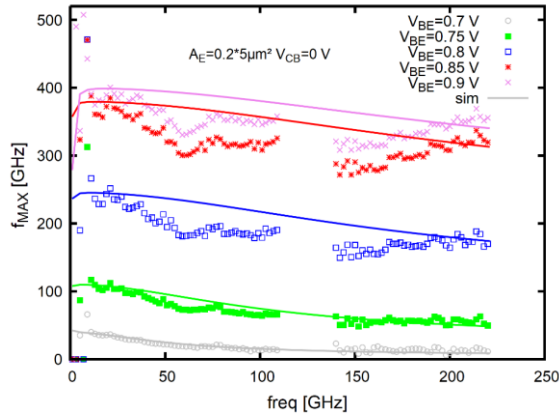
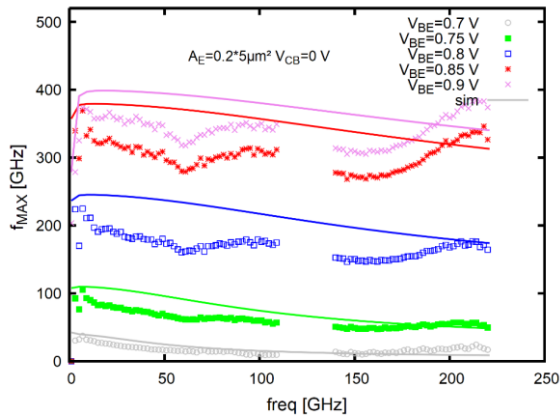
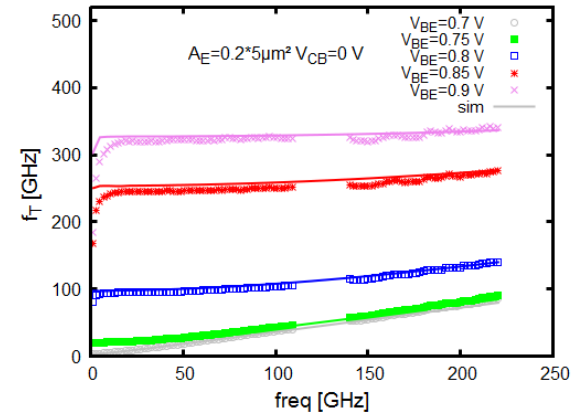
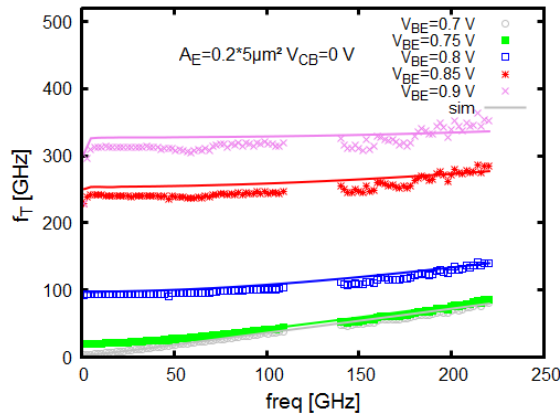
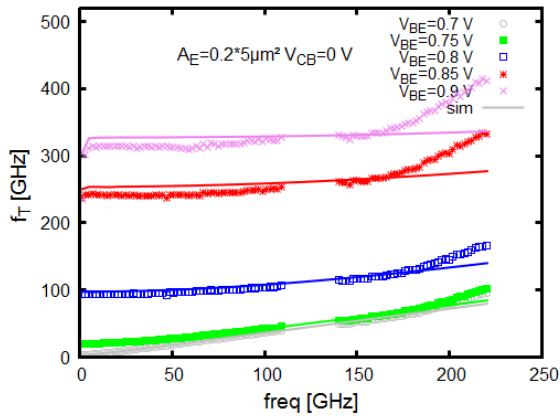
16T results

Capacitance from cold S parameters : SOLT + OS / TRL + OS / 16 terms + OS



16T results

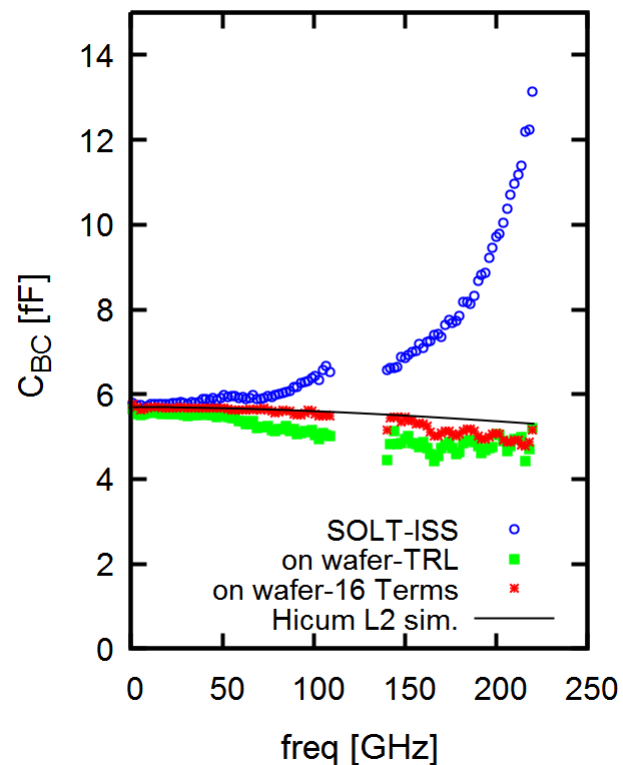
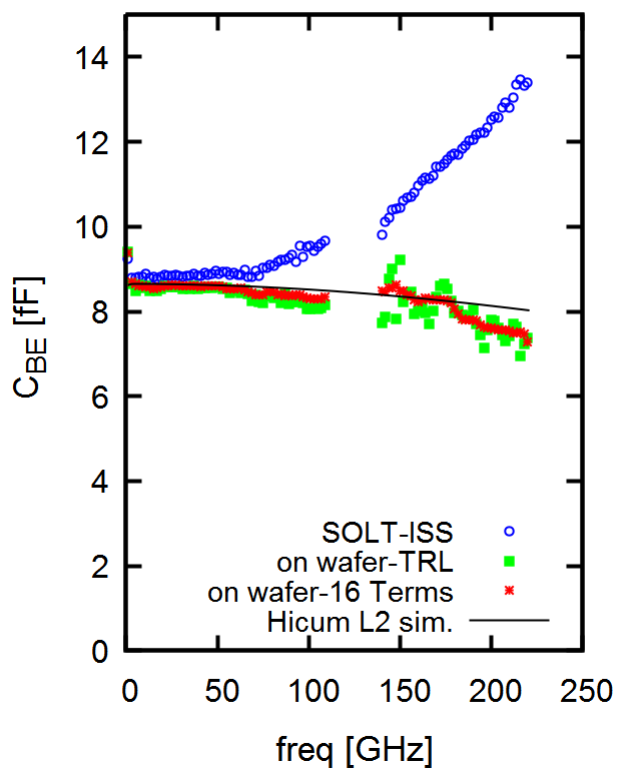
Transistor measurements



16T results

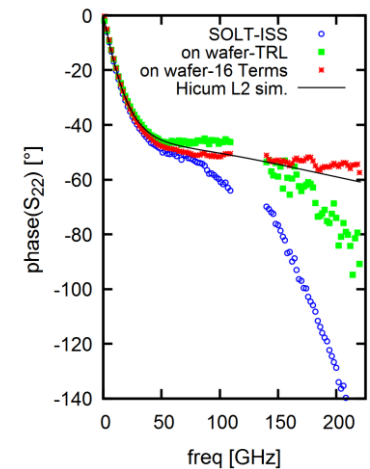
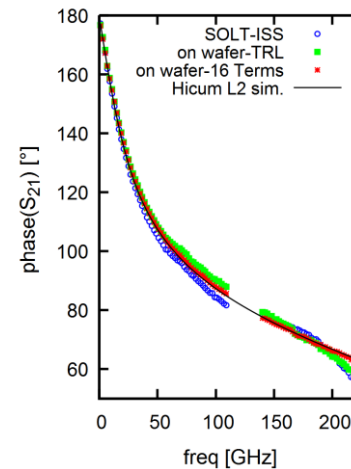
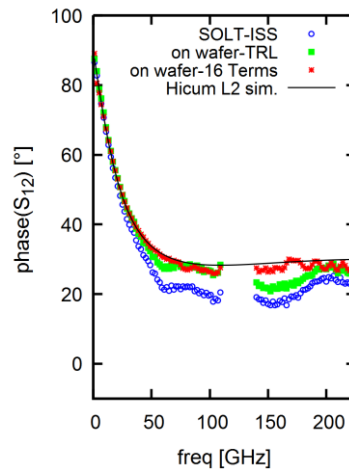
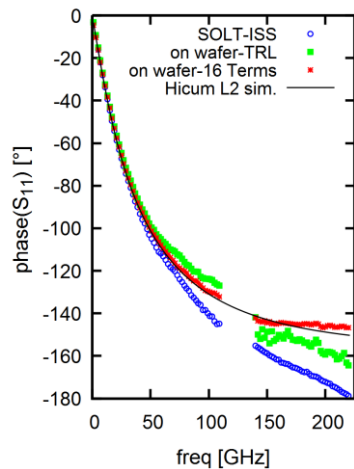
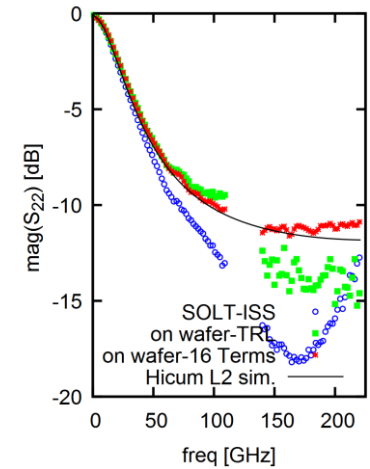
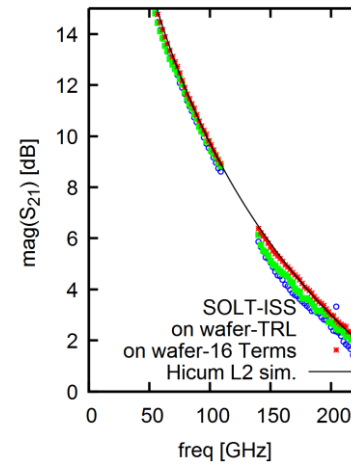
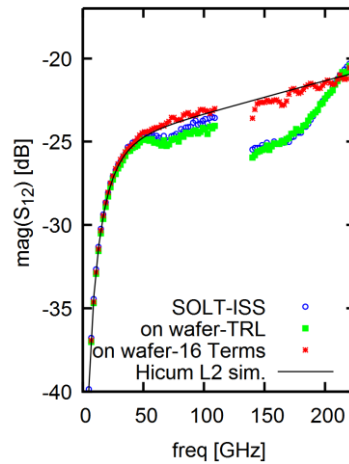
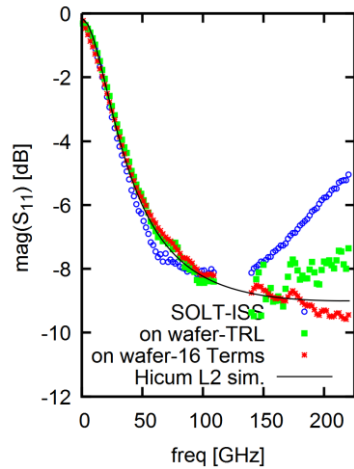
Capacitance from cold S parameters : SOLT + OS / TRL + **SO** /16 terms + **SO**

- ▶ If we change of de-embedding from open-short to short-open !



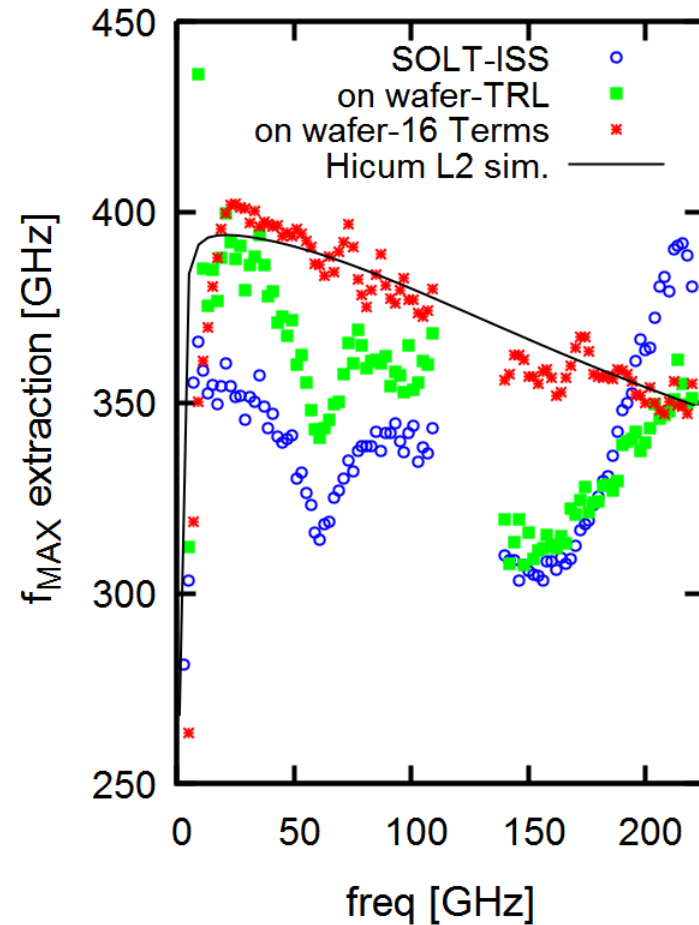
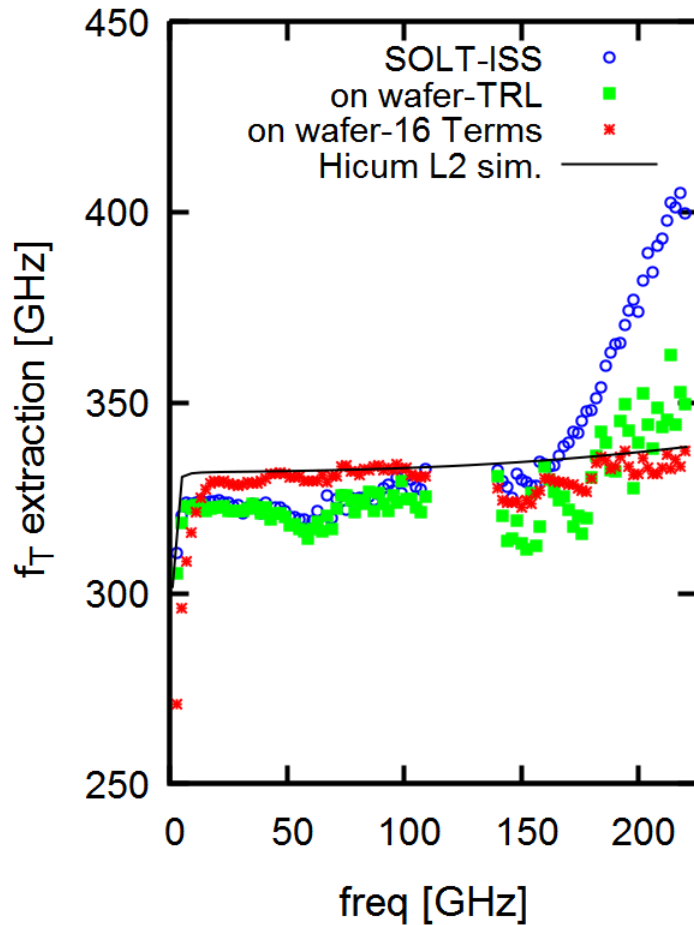
16T results

Forward S parameters ($V_{BE}=0.9V$ and $V_{CB}=0V$) (SOLT + OS / TRL + SO / 16 terms + SO)



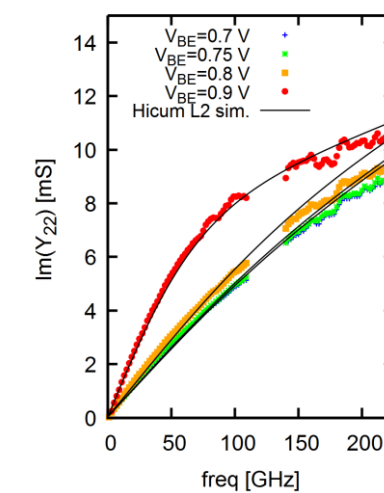
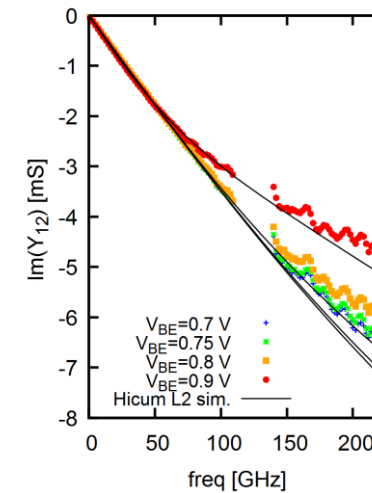
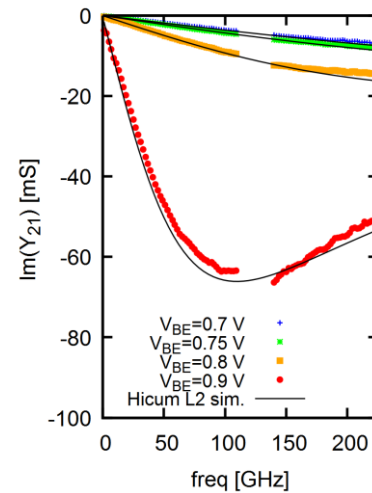
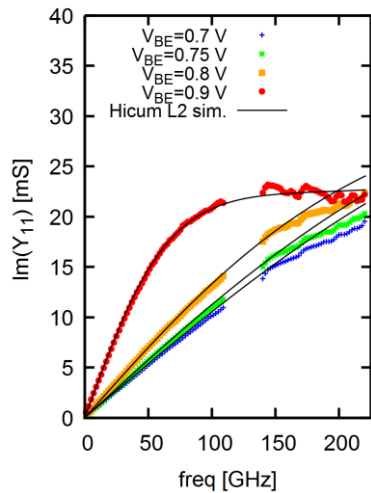
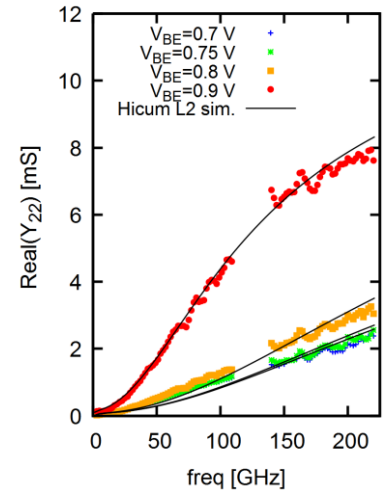
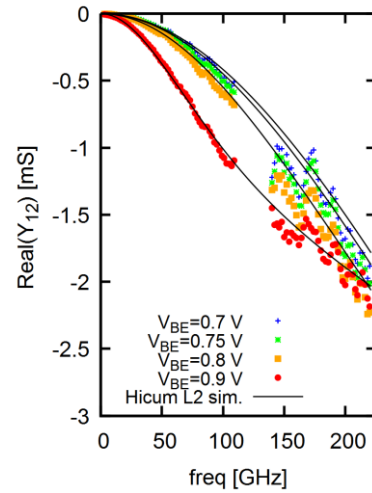
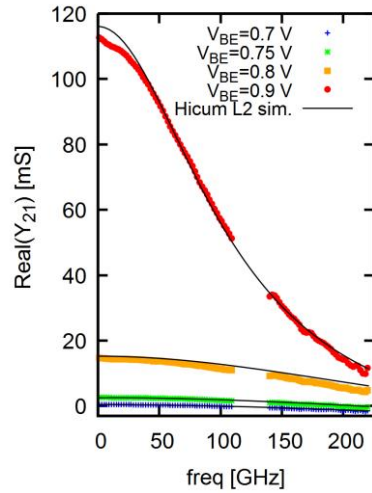
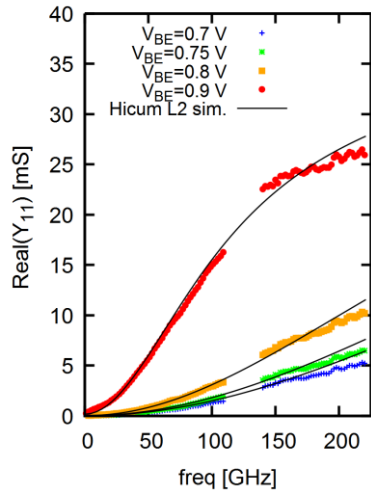
16T results

Forward S parameters ($V_{BE}=0.9V$ and $V_{CB}=0V$) (SOLT + OS / TRL + **SO** /16 terms + **SO**)



16T results

Forward Y parameters ($V_{BE}=0.9V$ and $V_{CB}=0V$) : 16 terms + SO



Conclusion

- Coupling is a show stopper for accurate S-parameter measurements
- Two types of coupling
 - Probe-to-probe
 - Probe-to-substrate
- Coupling can be decreased by appropriate test-structure design and layout
 - Chess-pattern of different structures on the chip
 - Appropriate distance between structures: not too dense
 - Appropriate distance between port 1 and port 2
 - etc.
- Invent new probe-tip with reduced coupling, work is on-going (results next year ?)
- Revisit 16 terms error-model: very promising results! => The solution

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- Acknowledgement to **ANR PRECISE (IMS, TIMA, IEMN, MC2 Technologies)**

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