

Effects of gate stack parasitic charge on current-voltage characteristics of high- κ /SiO₂/Ge-channel Double-Gate MOSFETs

D. Munteanu, M. Moreau, J.L. Aufran

IM2NP, CNRS (UMR 6242), Bât. IRPHE, 49 rue Joliot-Curie, BP 146,
F-13384 Marseille Cedex 13, France

1. INTRODUCTION

High mobility semiconductors, such as Ge, having higher hole and electron mobilities than in Si, are seriously envisaged for the MOSFET channel [1]. In the same time, SiO₂ is replaced in the gate stack by high- κ materials to prevent direct gate tunneling in very thin oxides [2], especially for low-power applications. Double-Gate (DG) architecture device provides enhanced electrostatic control and low short-channel effects compared to bulk MOSFETs. Then, combining Ge/high- κ /metal stack with DG MOSFETs could be seriously considered to reach predicted performances for future technological nodes. However, the introduction of high- κ dielectrics poses several problems, such as the presence of discrete fixed charges which could be incorporated in the gate stack, inducing lateral nonuniformities of surface potential. In this paper we investigate the effects of gate stack parasitic charges on the current-voltage characteristics of DG MOSFET with metal/high- κ /SiO₂/Ge-channel using two-dimensional (2D) quantum numerical simulation. We show that the charges trapped in the high- κ layer induce 2D potential fluctuations in the structure and degrades the subthreshold behavior of the drain current.

2. RESULTS

The DG MOSFET architecture simulated in this work is symmetric, with a double-layer gate stack (interfacial oxide+high- κ layer). 2D numerical simulations have been performed using a simulation code previously used for Si channels [3] and now extended for taken into account Ge channels. This code self-consistently solves the Schrödinger and Poisson equations on the entire device and couples the solution of this system with the drift-diffusion transport equation. The charge pattern examined in this study is inspired from the situation encountered in MOS devices with crystallized high permittivity materials. This modeling approach is summarized in Fig. 1a for a typical high permittivity/interfacial oxide bi-layer system. We model the high- κ layer as a juxtaposition of crystalline grains with vertical and charged grain boundaries. Introducing this particular charge pattern in the simulator, we evaluate its effect on the 2-D potential repartition and we quantify the induced surface potential fluctuations, as illustrated in Fig. 1a. We see that the charge localized at grains boundaries

significantly affects the potential repartition not only in the high permittivity layer, but also in the underlying oxide and semiconductor regions. This result is important because it shows that the microscopic structure of the layer could affect the electrical properties of the semiconductor surface. Our simulation results show that the 2D potential fluctuations, induced by the charged grain boundaries, considerably degrade the drain current-voltage characteristics, mainly increasing the subthreshold slope and the off-state current. This is shown in Fig. 1b where 1, 2 or 3 charged grains are considered in the upper high- κ layer. The case with no charge in the gate stack is also represented. Moreover, the subthreshold curve can be also deformed, because the front DG-channel is in conduction more rapidly than the back channel, creating a “hump” in the drain current (as visible in fig. 1b for the case when two charged grain are considered).

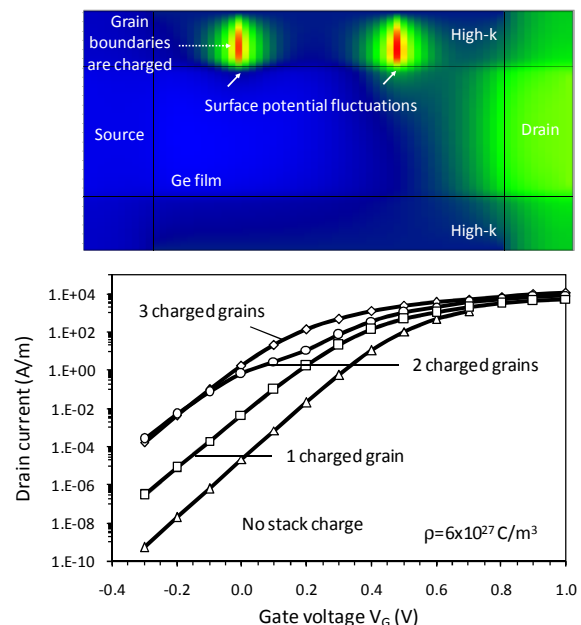


Figure 1: Modeling approach developed to take into account the fixed charge present at grain boundaries in the crystalline high- κ dielectric of a DG MOSFET.

REFERENCES

- [1] M. Moreau et al., J. Non-Cryst. Sol., 355, 1171-1175, (2009).
- [1] M. Houssa, M.M. Heyns, in High- κ Gate Dielectrics, IOP Publishing, Bristol, U. K., 2004.
- [3] D. Munteanu, J.L. Aufran, Solid-State Electron. 47, 1219, (2003).