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Electrical and Electrothermal 2D Simulations of a 4H-SiC High Voltage Current Limiting Device for Serial Protection Applications

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Abstract – The subject of this paper is a study of the ability of silicon carbide to be used for new solid state power device applications. By the way, a 4H-SiC current limiting device is studied. The device structure is a vertical power Mosfet like with a preformed N channel. Its electrothermal behavior is presented through simulations with ISE TCAD tools. The efficiency of such silicon device is estimated for comparison with SiC. A full simulation with two SiC devices inside a HSPICE modeled circuit is also proposed to study the ability of a bi-directional serial protection system.

Index terms: SiC, current limiting device, serial protection, temperature, 2D finite element simulation.

1. Introduction

Silicon carbide is well adapted for the power electronic needs. Already, many prototypes have been built and most of them show interesting abilities. In few years, it would be possible to translate in SiC technology most of the commercial silicon device and, therefore, to push away the limits of the semiconductor power device. For example, a 600V Schottky diode should be proposed commercially at the beginning of 2002. The silicon carbide properties ($E_g \approx 3$ eV, $E_c \approx 2$ MV.cm⁻¹, $\lambda_{300K} \approx 4.5$ W.K⁻¹.cm⁻¹) allow to study specific device design for new application fields.

This paper presents a silicon carbide high voltage current limiting device for 50 A/(300V to 600V) applications. Typically, this kind of device has to work under high temperature conditions without failure. A simulation study of the static I-V characteristics is proposed. Electrothermal 2D simulations have been performed to take into account self-heating during a current surge wave. A mixed mode simulation is proposed to study the ability of a bi-directional current limiting device, composed by two unidirectional devices,

in case of a short-circuit on a 50Hz/300V power supply. No oxide charges and no contact resistance have been considered. The parameters of the models used for the simulations [1] are:

Electron mobility model:

$\mu_{dop} = \mu_{min1} e^{\frac{E_c}{N_i}} + \frac{\mu_L \left(\frac{T}{300}\right)^{\xi} - \mu_{min2}}{1 + \left(\frac{N_i}{C_r}\right)^{\alpha}} - \frac{\mu_i}{1 + \left(\frac{C_s}{N_i}\right)^{\beta}}$	Parameter	4H-SiC
	μ_{min1} [cm ² /V.s]	20
	μ_{min2} [cm ² /V.s]	0
	μ_L [cm ² /V.s]	700
	ξ	3
	μ_i [cm ² /V.s]	0
	C_r [cm ⁻³]	4.5×10^{17}
	α	0.45
	C_s [cm ⁻³]	3.43×10^{20}
	β	2
P_c [cm ⁻³]	0	
$\mu(E) = \frac{\mu_{low}}{\sqrt{1 + \left(\frac{\mu_{low} E}{v_{sat}}\right)^2}}$	Parameter	4H-SiC
	v_{sat0} [cm/s]	2×10^7
	$v_{sat,exp}$	0.5
$v_{sat} = v_{sat0} \left(\frac{T}{T_0}\right)^{-v_{sat,exp}}$	Parameter	4H-SiC
	v_{sat0} [cm/s]	2×10^7

Impact ionization model:

$\alpha = \gamma a \exp\left(\frac{-\gamma b}{E}\right)$ <p>with</p> $\gamma = \frac{\tanh\left(\frac{h\omega}{600k}\right)}{\tanh\left(\frac{h\omega}{2kT}\right)}$	Parameter	4H-SiC
	$a_{n,p}$	3.09×10^6 cm ⁻¹
	$b_{n,p}$	1.8×10^7 V/cm
	E_0	4×10^5 V/cm
	$\hbar\omega$	0.09 eV

Thermal conductivity:

$\lambda(T) = \frac{1}{a}$	Parameter	4H-SiC
	a	0.01 K.cm/W

	λ	b	6×10^{-4} cm/W
		c	6×10^{-7} cm/W.K
	C		3 J/K.cm ³

2. Device structure.

Figure 1 shows the device structure. The design looks like a vertical power MOSFET with a gate-source short-circuit and a preformed N channel. The epitaxial layer is optimized to withstand 600V. The region between the P buried layer [2] and the SiC/oxide interface defines the channel. The peripheral protection is realized by guard rings. They are integrated in the process flow of the active region. The device is normally on. The current conduction is bidirectional but the current limiting behavior is available only for positive drain to source bias voltage. The current limiting effect is produced by a JFET effect in the channel region due to the enlargement of the space charge region inside the channel. The space charge of the reverse biased P⁺/N_{channel} junction spreads as the drain-to-source voltage increases.

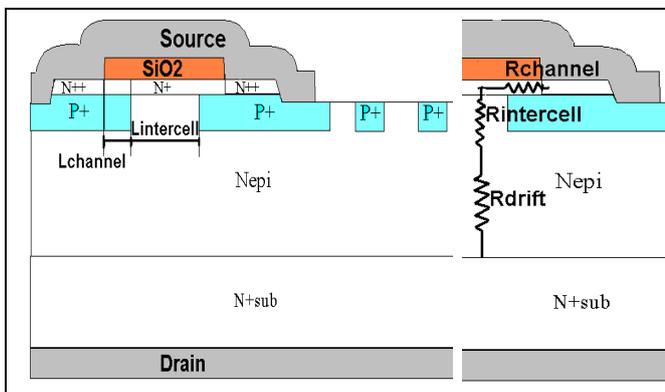


Fig. 1: Vertical cross section of the device and its guard rings peripheral protection (the channel length ‘Lchannel’ and the intercell length ‘Lintercell’ are noted).

3. i - v static characteristics

3.1. Static characteristic

A typical I-V curve of a current limiting device is shown on the Figure 2. The channel design controls the limitation current $I_{SATURATION}$ and the on-resistance R_{ON} . The breakdown voltage (V_{br}) is withstood by the adjusted N epilayer for 600V capability ($6 \mu\text{m}/10^{16}\text{cm}^{-3}$). Therefore, the R_{ON} value is the addition of $R_{channel}$, R_{drift} and $R_{intercell}$ (Fig. 2).

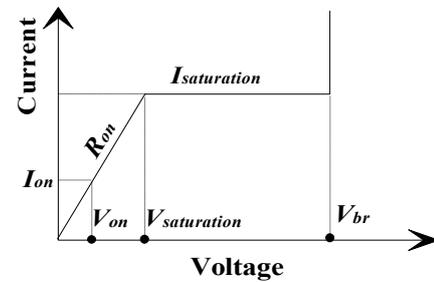


Fig. 2: Typical I-V characteristic of a current limiting device.

For $0 < V_{DS} < V_{SATURATION}$, the current increases linearly with V_{DS} . When V_{DS} is over $V_{SATURATION}$, the reverse space charge region due to the P⁺/N_{channel} junction is wide enough to pinch off the channel. Then, the current can not increase more, and, remains equal to $I_{SATURATION}$. 2D process simulation and 2D electrical simulations with the tool package ISE TCAD [3] allow studying the electrical behavior the device. The figure 3 shows a simulated characteristic with a current saturation of 1500 A/cm² and a specific on-resistance equals to 10 mΩ.cm² (compared to a silicon 600V structure $45 \mu\text{m}/10^{14} \text{cm}^{-3}$, only $R_{drift} = W_{epi}/(qn\mu_n) \approx 250 \text{m}\Omega.\text{cm}^2$).

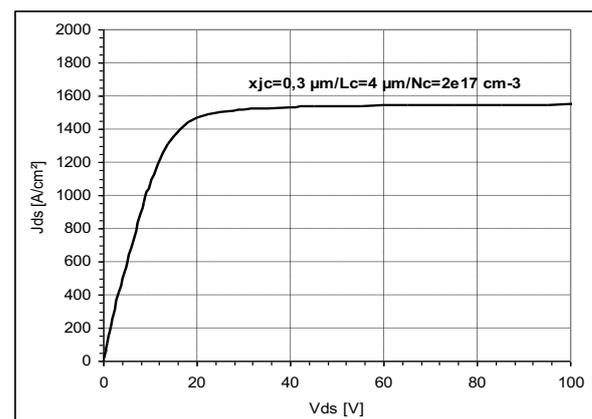


Fig. 3: I-V curve at T=300K (channel depth=0.3 μm; channel length=4 μm; channel doping level=2×10¹⁷ cm⁻³, Lintercell=10 μm)

3.2. Simple analytical model

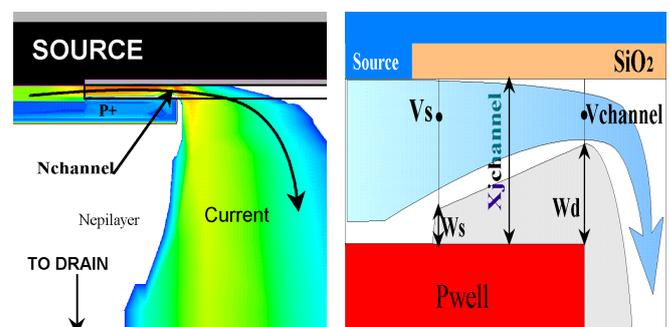


Fig. 4: Left picture: 2D mapping of the current inside the device near the channel region. Right picture: simplified current path in the channel.

As is shown on figure 4 (left picture), the current flow crosses the channel horizontally, and then goes down through the intercell region and the epilayer. 2D simulations are needed to evaluate the parasitic effects of the intercell JFET and SiC/oxide interface charge. However a simple analytical model can be extracted from 2D simulations. The saturation effect can be described by the JFET equation [4] with $V_{GS}=0V$ (figure 4, right picture).

The built-in voltage and pinch-off voltage expressions are given by:

$$V_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_{channel}}{n_i^2} \right)$$

$$V_p = \frac{X_{jchannel}^2 q N_{channel}}{2\epsilon}$$

The space charge width expressions for both edges of the channel as defined on fig. 4 are as follows:

$$W_D = \sqrt{\frac{2\epsilon(V_{Channel} + V_{bi})}{qN_{Channel}}} \quad \text{and} \quad W_S = \sqrt{\frac{2\epsilon V_{bi}}{qN_{Channel}}}$$

The current versus voltage expression is:

$$I_{Channel}(V_{Channel}) = \frac{W}{L_{Channel}} \frac{\mu_{Nchannel} q^2 N_{Channel}^2}{\epsilon} gg(V_{Channel})$$

where W is the third dimension of the channel and with

$$gg(V_{Channel}) = X_{jchannel} \frac{W_D^2 - W_S^2}{2} - \frac{W_D^3 - W_S^3}{3}$$

The saturation current is given when $W_D=X_{jchannel}$. This model is used to roughly evaluate the range of each channel parameter, before running the necessary 2D numerical simulations for the device optimization.

3.3. With a gate control

It could be necessary to add a third contact to drive the device. The device stays normally-on, and it can be switched off with a negative gate-to-source voltage. In case of surge, the device could limit the current and open the line. The static disjunction function could, therefore, be realized. Fig. 5 shows different IV characteristics $I_{DS}=f(V_{GS})$ for $V_{DS}=500V$. For many designs of the channel, a V_{GS} of less than -15V seems enough to switch off the device. The structures simulated Fig. 5 are designed with different channel depths (0.15 μm and 0.2 μm) and channel doping levels ($2 \times 10^{17} \text{ cm}^{-3}$ and $3 \times 10^{17} \text{ cm}^{-3}$).

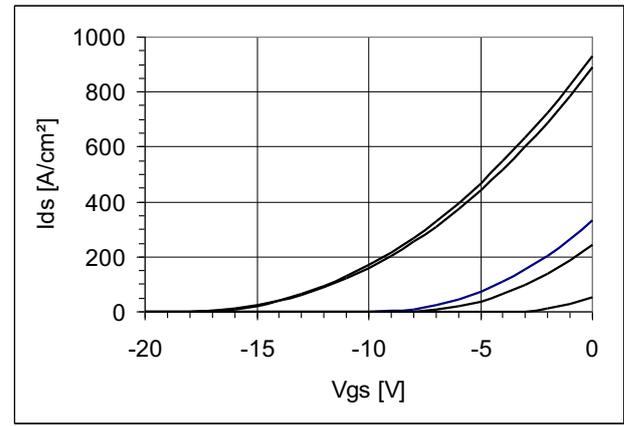


Fig. 5 Static characteristics $I_{DS}=f(V_{GS})$ at $V_{DS}=500V$ for different channel designs.

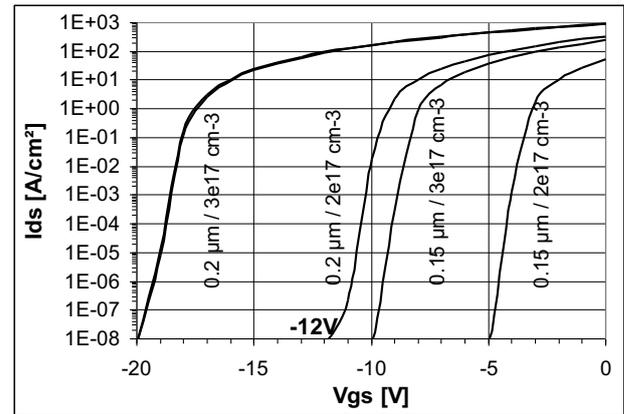


Fig. 6: Static characteristics $I_{DS}=f(V_{GS})$ at $V_{DS}=500V$ and $T=300K$ in logarithmic scale for different channel designs.

Figure 6 shows a good ability of the device to be used as a switch. For channel depth of 0.2 μm and a channel doping level of $2 \times 10^{17} \text{ cm}^{-3}$, a gate-to-source of -12V can switch off the device with a low leakage current.

4. Electrothermal simulation

In case of current surge, the current limiting device has to operate under current and high voltage simultaneously. Therefore, the self-heating of the device generates high temperature spot and could start up a thermal run away failure. Electrothermal 2D simulations have been performed to take into account the effects of the temperature on carrier mobility [5,6], carrier concentration, thermal conductivity [7,8] and ionization coefficient [9]. The carrier mobility model [10,11] used is also a doping and electric field dependent model.

To verify the current limiting ability during a current surge, some electrothermal simulations have been performed with a copper layer (1mm) added to the backside. In this case, the thermal conductivity and the thermal capacitance of the heat sink are considered. Figures 7,8 and 9 show the simulation results. The V_{DS} waveform is a 500V/1ms ramp during the first 1ms and then a constant (500V). The maximal temperature stabilizes close to 900 K and the device keeps working. The considered structure is designed for a 1000 A/cm² saturation current density (figure 7).

Figure 8 shows the average current density versus time and the corresponding maximal temperature inside the device. When the temperature increases, the carrier mobility starts to decrease and leads the current to do the same. The hot spot is located at the end of the channel, close to SiC/oxide interface (Fig. 10). The stress of the oxide layer is quite important: high electric field (≈ 5 MV/cm) and high temperature. Therefore the real temperature limit of the device is determined by the oxide thermal behavior and not by SiC. Figure 9 shows the average power losses in the device versus time under the same conditions as figure 8. The power reached after 1ms is closed to 70 kW/cm² and then saturates as the current decreases.

The device keeps a good behavior even under such high temperature conditions. The current level through the device essentially depends on the channel parameters and the electron mobility. The device structure allows considering a good mobility value in the channel contrary to the classical SiC-MOSFET in which the inversion layer mobility is reduced by the SiC/oxide interface quality [12]. Then, the current versus temperature dependence should be the same that the one adopted for the mobility behavior.

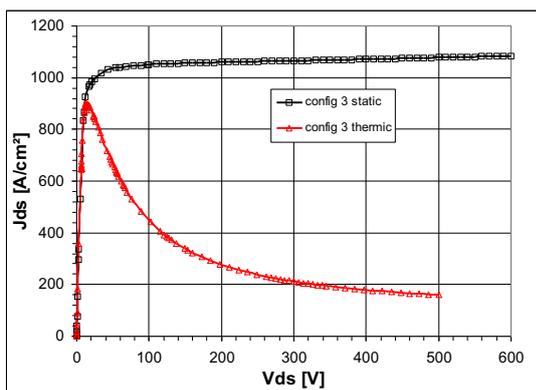


Fig. 7: Comparison of the static I-V characteristic at T=300K and electrothermal transient behavior. The structure is designed for a 1000A/cm² saturation current. simulations have been performed with a copper layer (1mm) added to the backside as a thermal boundary.

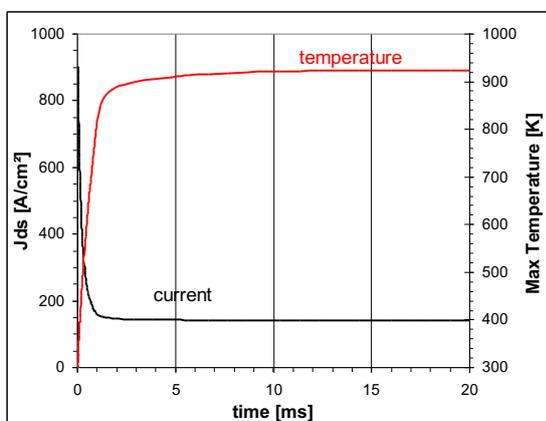


Fig. 8: Electrothermal behavior in case of >10ms current surge. The V_{DS} waveform is a 500V/1ms ramp during the first 1ms and then a constant (500V). simulations have been performed with a copper layer (1mm) added to the backside as a thermal boundary.

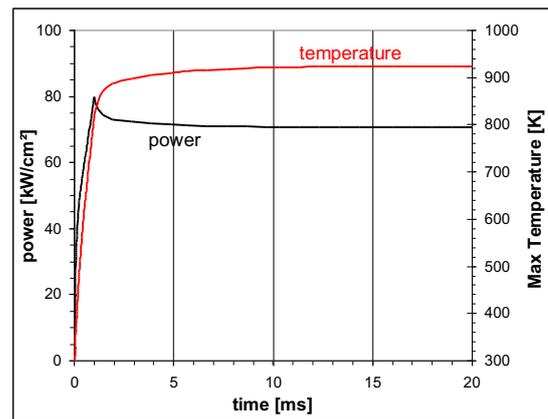


Fig. 9: Average power versus time (Same conditions as figure 8).

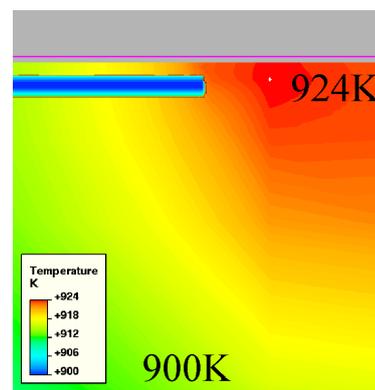


Fig. 10: Temperature 2D mapping inside the SiC device (Fig. 8) at V_{DS}=500V and t=20ms. The max temperature point is located very close to the SiO₂/SiC interface.

For comparison with the silicon case, we studied a similar structure, as there is no commercial silicon current limiting device acting in the range of 50A/600V. The silicon device is a power MOSFET with an implanted channel [13] (Fig. 11); the low doped region is optimized for 600V ($45 \mu\text{m}/10^{14} \text{cm}^{-3}$). The same thermal boundary condition as for the SiC device is used for the silicon device. The resulting saturation current is 60 A/cm² and the on-resistance is 600 mΩ.cm² (figure 12). Contrary to the SiC structure, after 0.9ms, the temperature inside is so high (intrinsic carrier level is enough) that a thermal run-away occurs and destroys the silicon device (figure 12).

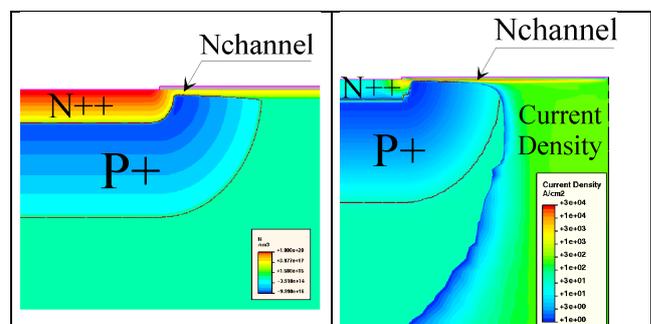


Fig. 11: Left picture: 2D mapping of the doping inside the silicon device near the channel region. Right picture: current density 2D mapping close to the channel at V_{DS}=50V.

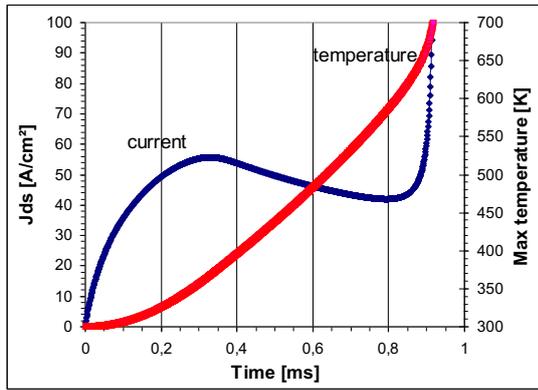


Fig. 12: Thermal run-away of a silicon current limiting device (same V_{DS} wave shape and thermal boundary conditions as for the SiC device figure 8).

	SiC	Silicon
$J_{SATURATION}$	1000 A/cm ²	60 A/cm ²
R_{ON}	8 m Ω .cm ²	600 m Ω .cm ²
$V_{SATURATION}$	8V	36V
Max temperature reached	900K	650K (before run-away)
Time without run-away	At least 20ms	0.9 ms

Table 1: Ratings of both SiC and silicon device.

The silicon device is not adapted for this kind of application; the current density range and the specific on-state resistance lead to build device with surface of 1 cm² almost for a saturation current of 60A ($R_{ON} \approx 0.6 \Omega$). To avoid the thermal run-away of the silicon device during at least 10ms, the saturation current density should be reduced and then the surface should be increased. Silicon carbide is well adapted (Table 1), can work with low surface (6 mm² for $I_{SAT} = 60A$ and $R_{ON} \approx 0.1 \Omega$) and with a thermal boundary of 1 mm copper layer.

5. Mixed mode electrothermal simulation

The simulation mixed mode means that the different components of a circuit are modeled either with HSPICE, either with finite 2D element. The circuit used for the mixed mode simulation is composed by two 2D finite element current limiting SiC devices CDL1 and CDL2 (Fig. 13), and hspice N-mosfet and pn-diode [14]. The model used for the hspice mosfet is the mos3 model [15] adapted to describe the IRF 740 power mosfet. The aim of this simulation is to study the behavior of the protection device in case of short-circuit; the power supply is a 50Hz/300V voltage. The load is chosen to have 6A for the nominal current. The short-circuits are controlled either by the mosfet M1 driven by V_{gs1} , either by the one driven by V_{gs2} (M2) (Fig. 13). No line inductance has been added to the circuit, therefore, there is no di/dt limitation; this is the worst working case of the current limiting devices. Fig. 14 sums up the simulation results with the voltage wave shape, the current wave shape and the temperature inside both the devices versus time.

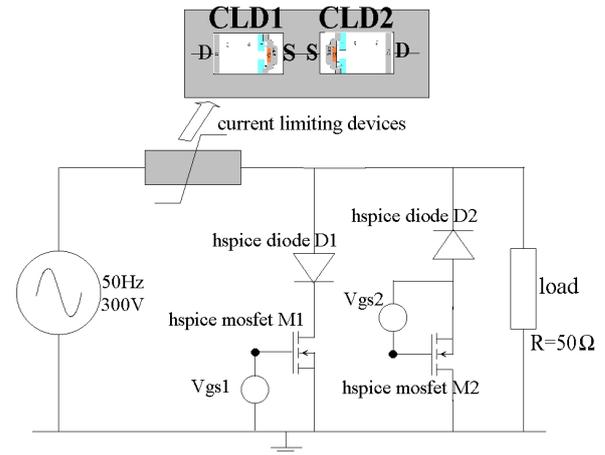
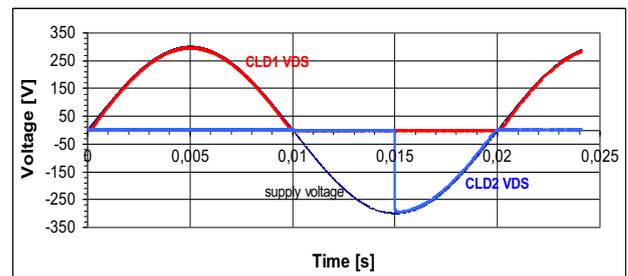


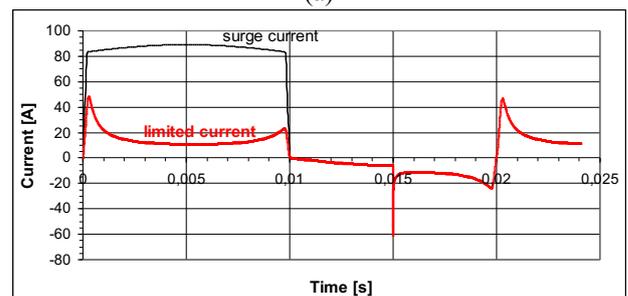
Fig. 13: simulated mixed mode circuit. The short-circuits are generated by M1 (V_{GS1}) or M2 (V_{GS2}).

The supposed surge current is around 80 A and the current limiting devices are designed for a 60A saturation current.

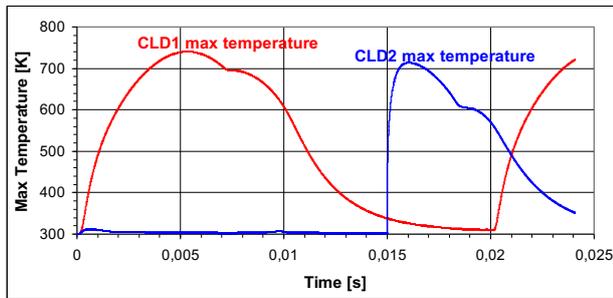
In the present experiment, a load short-circuit appears at the very beginning of the positive side, due to the M1 switching on. The uncontrolled current growth is avoided and the voltage supported by the SiC CLD1 device follows the power supply (Fig. 14 (a)). The Fig. 14 (b) shows the current wave shape with and without current limiting device, the considered current is the one who flows through the SiC current limiting devices CLD1 and CLD2. The current is limited efficiently to 10 A by the CLD1 device. The maximal temperature inside the CLD1 device reaches 750K (Fig. 14 (c)). When the voltage supply negative side occurs, the current is flowing through CLD1, CLD2 and the resistive load till the switching on of M2 causing a second short-circuit at $t = 15ms$, when the voltage supply equals $-300V$. The SiC protection device acts immediately (CLD1 and CLD2) even with a high dv/dt ($\approx 300V/10ns$). The diodes D1 and D2 avoid the conduction of the mosfets due to their integrated pn-diode in case of negative value of drain-to-source voltage.



(a)



(b)



(c)

Fig. 14: Simulations results obtained with the circuit Fig. 13. The short-circuits are controlled by the hspice mosfet M1 and M2. The pictures (a), (b) and (c) show the wave shape of the voltage, current and temperature versus time, respectively. The CLD1 and CLD2 structures and thermal boundary conditions are those used for the previous results shown at Fig. 10. Therefore, the on-resistance of each device is 0.1Ω .

6. Conclusion

According to our simulation study, silicon carbide seems very attractive for current limiting application. The concept presented here can be applied to a large range of currents and voltages. The breakdown voltage could be improved without dramatically increase the on-resistance value ($1500\text{V} - 10\mu\text{m}/5 \times 10^{15} \text{ cm}^{-3}$). The device could even be controlled with a gate electrode for the switching off. It could be useful not only for serial protection but also for other applications, as for example, the motor starting phase. The use of two devices could also be possible for a bi-directional efficiency with a low on-resistance (0.2Ω) for the complete serial protection device.

Acknowledgment

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References

- [1] F. Nallet, D. Planson, K. Isoird, M.L. Locatelli, J.P. Chante, "Comparison of Static, Switching and Thermal Behavior between a 1500V Silicon and SiC Bipolar Diodes", CAS'99 Proceedings, pp. 195-198, October 1999.
- [2] P.M. Shenoy, B.J. Baliga, "High Voltage Planar 6H-SiC ACCUFET", Materials Science Forum Vols. 264-268 (1998) pp. 993-996, Trans Tech Publications, Switzerland.
- [3] ISE Integrated Systems Engineering AG, Zurich/CH (1998)
- [4] S.M. Sze, "Physics of Semiconductor Devices", 2nd Edition, John Wiley & Sons, Inc, ISBN 0-471-09837-X
- [5] Pensl G. et al. , "Electrical And Optical Characterisation of SiC", Physica B 185 (1993), pp 265-273.
- [6] T. Troffer, M. Schadt, T. Frank, H. Itoh, G. Pensl, "Doping of SiC by Implantation of Boron and Aluminum", Phys. Stat. Sol. (a) 162, 277 (1997).
- [7] St.G. Müller, R. Eckstein, "Experimental and Theoretical Analysis of the High Temperature Thermal Conductivity of Monocrystalline SiC", ICSCIII'97 Sweden.
- [8] Glen A. Slack, " Thermal Conductivity of Pure and Impure Silicon, SiC, and Diamond ", *J. Apply. Phys.* 35 (12), pp. 3460-66, Dec 1964.
- [9] R. Raghunathan, B. J. Baliga, "Temperature Dependence of Hole Impact Ionization Coefficients in 4H and 6H-SiC", Solid State Electronics, vol 43, pp. 199-211, 1999.
- [10] D. M. Caughey and R. E. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Electric Field", *Proc. IEEE*, pp. 2192-93, Dec. 1967.
- [11] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and Hole Drift Velocity Measurements in Silicon and their Empirical Relation to Electric Field and Temperature", *IEEE Trans. on Elect. Dev.*, Vol. ED-22, pp. 1045-47, 1975.
- [12] T. Ouisse, "Electron Transport at the SiC/SiO₂ Interface", *phys. Stat. Sol (a)* 162, 339 (1997).
- [13] J.L. Sanchez, Ph. Leturcq, P. Austin, "Design and Fabrication of New Silicon High Voltage Current Limiting Devices", 8th Int. Symp. on Power Semi. Devices and ICs (ISPSD'96), Hawaii (USA), 20-23 Mai 1996, pp.201-205.
- [14] Ron M. Keilkowski, "Inside Spice", Second Editon, McGraw-Nill ,New york, 1999
- [15] A. Vladimirescu and S. Lui, "The Simulation of MOS Integrated Circuit Using Spice2", ERL Memo N° ERL M80/7, Electronics Research Laboratory, University of California, Berkeley, October 1980