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# Complementary Inverter Based on C60 and Pentacene Doped CVD Graphene Field Effect Transistors on SiO<sub>2</sub>

Jacopo Oswald, Davide Beretta, Michael Stiefel, Roman Furrer, Dominique Vuillaume and Michel Calame

**Abstract**—The rapid expansion of the Internet of Things (IoT) has fueled the exploration of novel materials and device architectures to meet the demands of applications such as smart wearables, environmental sensors, and flexible displays. In this context, graphene has emerged as a remarkable candidate due to its exceptional electronic and mechanical properties that are suitable for the development of flexible electronic devices. This work investigates the potential of C60- and Pentacene-doped Graphene Field Effect Transistors (GFETs) as building blocks for complementary inverters in digital and/or analog flexible electronic circuits. The fabricated complementary inverters use doped graphene as the channel material for both the  $n$ - and the  $p$ -type transistors. The channel length of the GFETs spans the range from  $5\ \mu\text{m}$  to  $100\ \mu\text{m}$  and does not affect the measured transfer characteristic of the inverters, which is obtained by operating the transistors between their respective Dirac points. While the GFET-based inverters show a voltage gain of about  $2 \times 10^{-2}$  and a bandwidth up to 10 kHz, circuit simulations indicate that by integrating the GFETs and by carefully designing the chip metal interconnects, the inverter could reach operating frequencies in the GHz regime. Additionally, scaling the graphene channel length allows to tune the cut-off frequency and static power dissipation of the inverter, potentially meeting the requirements of specific applications.

## I. INTRODUCTION

Graphene-based devices have attracted significant attention due to their high mobility, flexibility and ability to conform to various surfaces [1]. The recent advancements in both the growth of large area graphene using Chemical Vapour Deposition (CVD) and the techniques for transferring graphene onto a wide variety of substrates have paved the way for the development of flexible graphene-based electronic devices [2], which overcome some inherent limitations of traditional Silicon-based electronics. Further research on graphene-based digital and/or analog circuits is

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still needed to enable communications and data processing functions, and thus, to fully exploit graphene's potential for applications in smart wearables, environmental sensors and flexible displays [3], [4]. In this context, different methods to induce  $n$ - and  $p$ -type behavior in Graphene Field Effect Transistors (GFETs) have been developed [5], [6], [7] and implemented to fabricate electronic components such as the graphene complementary inverter, which is a fundamental building block for digital circuits that produces an output signal that is the complement of its input signal [8], [9]. Here, the exceptional charge carrier mobility in graphene is attractive for electronic devices requiring high frequency operation on flexible and/or transparent substrates. In addition, the techniques used for the lithography of graphene and for the deposition of organic thin films are compatible with existing electronic manufacturing workflows, making the integration of the graphene-based inverters possible and cost-effective.

In this work, we show that  $n$ - and  $p$ -type Graphene Field Effect Transistors (GFETs), obtained by doping CVD graphene with thin films of C60 and Pentacene [5], can be assembled into working complementary inverters. The inverters were assembled with pairs of GFETs with fixed channel width  $W = 5\ \mu\text{m}$  and length  $L = 5, 10, 20, 50, 100\ \mu\text{m}$ , which were fabricated on separate chips. The output and transfer characteristics of the inverters were measured by operating the graphene transistors between their Dirac points under vacuum ( $1 \times 10^{-6}$  mbar) at room temperature (293 K). The inverter voltage gain ( $2 \times 10^{-2}$ ) and static power dissipation as a function of the graphene channels lengths were extrapolated from the current vs voltage (IV) measurements, while the dynamic response was obtained by applying digital signals (up to 10 kHz) to the devices input. The circuit simulations indicate that the fabrication of functional inverters, operating in the GHz frequency regime, should be possible by integrating the GFETs, reducing the dielectric thickness, and optimizing the metal interconnects.

## II. RESULTS AND DISCUSSION

Fig. 1a shows the complementary inverter assembled with pairs of  $n$ - and  $p$ -type Graphene Field Effect Transistor (GFET) fabricated on separate chips. The electrical probes were used to (i) supply  $V_{DD} = 1\ \text{V}$  to the source electrode of the  $p$ -type GFET, (ii) connect the source electrode of the  $n$ -type GFET to ground, and (iii) join the drain electrodes of the two GFETs and measure the output voltage  $V_{OUT} = V_{DD}/(1 + R_p/R_n)$ , where  $R_{n,p}(V_{IN})$  are the resistances of the  $n$ - and  $p$ -type graphene channels, respectively. The input voltage  $V_{IN}$  was provided by the

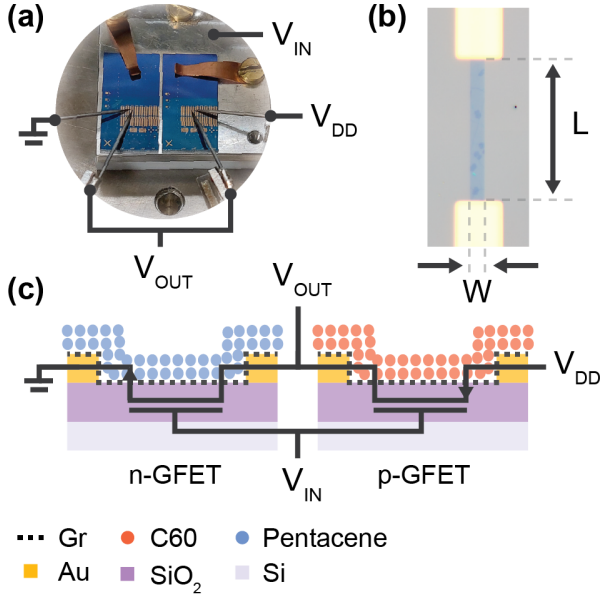


Fig. 1. (a) Photograph of the *n*- (left) and *p*-doped (right) Graphene Field Effect Transistor (GFET) chips assembled into one complementary inverter. (b) Optical microscope image of a representative GFET. The channel length  $L$  and width  $W$  of this device are  $50 \mu\text{m}$  and  $5 \mu\text{m}$ , respectively. (c) Electrical schematic of the assembled complementary inverter (not to scale). The cross-section shows the heavily *p*-doped Si Gate (G), the  $\text{SiO}_2$  dielectric (300 nm), the Ti/Au source/drain (5 nm/50 nm) and the *p*- and *n*-type Gr channels coated with thin films of C60 and Pentacene molecules, respectively.

metallic support which is in direct contact with the heavily *p*-doped Si substrate. Fig. 1b shows an optical microscope image of a representative GFET with graphene channel dimensions  $L = 50 \mu\text{m}$  and  $W = 5 \mu\text{m}$ . The CVD graphene was transferred on top of the lateral Ti/Au electrodes and subsequently patterned by ebeam lithography. Fig. 1c shows the electrical schematic and cross-section of two GFETs used to assemble a complementary inverter. The *n*- and *p*-type GFETs were obtained by thermal evaporation of thin films of Pentacene (blue circles) and C60 (red circles) on graphene (dashed black line), as previously reported [5].

Fig. 2 shows the transfer resistances  $R_n = V_{OUT}/I$  in blue, and  $R_p = (V_{DD} - V_{OUT})/I$  in red, as a function of the input voltage  $V_{IN}$ , for a fixed  $V_{DD}$  voltage of 1 V. The Dirac points of the *n*- and *p*-doped graphene were found at approximately  $-5 \text{ V}$  and  $28 \text{ V}$ . We note that the two GFETs operate as a complementary inverter in the grey shaded region between the Dirac points. In this region, the C60 and Pentacene doped GFETs show *p*- and *n*-type behavior, respectively. Their resistances at the respective Dirac points are  $R_n \approx 13 \text{ k}\Omega$  and  $R_p \approx 16 \text{ k}\Omega$  and the resistances ratio is  $R_p/R_n \approx 0.4$  at  $-5 \text{ V}$ , while it is  $R_p/R_n \approx 2.4$  at  $28 \text{ V}$ . The field-effect mobility, i.e.  $\mu = Lg_m/WC_{GS}V_{DS}$ , was extrapolated using the maximum of the transconductance  $g_m = \max(dI_{DS}/dV_{GS})$  [5]. The electron and hole mobilities were approximately  $\mu_e \approx 1000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  and  $\mu_h \approx 2000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  for the *n*-type and *p*-type transistors, respectively. This relatively high carrier mobility, combined with the mechanical prop-

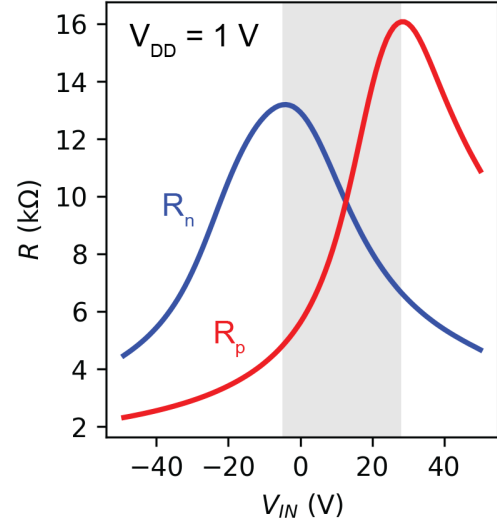


Fig. 2. Resistance  $R$  vs. input voltage  $V_{IN}$  measured on a representative complementary inverter consisting of two GFETs with  $L = 20 \mu\text{m}$ .  $R_n$  (blue) and  $R_p$  (red) are the resistances of the *n*- (left) and *p*-doped (right) GFETs, respectively. Complementary behavior is shown by the grey shaded area between the Dirac points of the two transistors. The Dirac points of  $R_n$  and  $R_p$  are approximately  $-5 \text{ V}$  and  $28 \text{ V}$ , respectively.

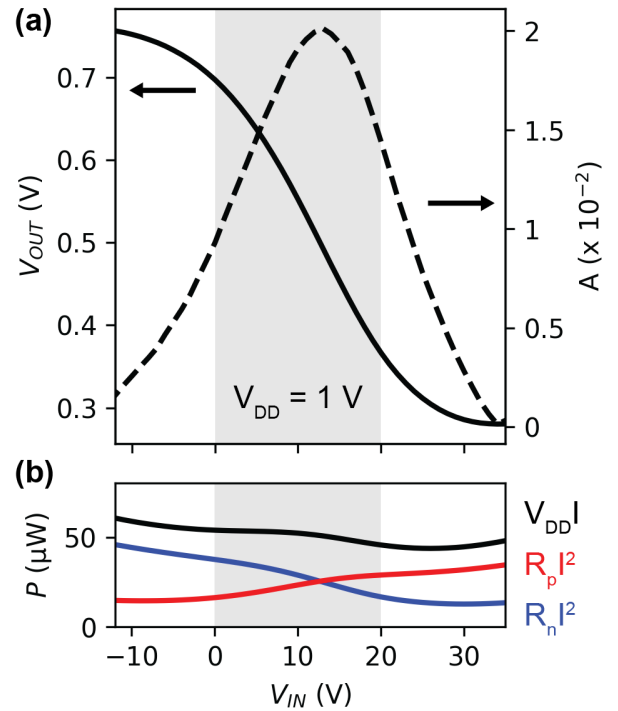


Fig. 3. (a) Output voltage  $V_{OUT}$  (solid line) and voltage gain  $A$  (dashed line) vs. input voltage  $V_{IN}$  of a representative complementary inverter assembled with two GFETs with  $L = 20 \mu\text{m}$ . (b) The static power dissipation of the inverter (black) and the power dissipated by the transistors through  $R_p$  (red) and  $R_n$  (blue). The dynamic response of the inverter is obtained by applying digital signals with low and high logic levels of  $0 \text{ V}$  and  $20 \text{ V}$  (grey dashed area).

erties of graphene, is attractive for applications requiring high speed operation on flexible substrates.

Fig. 3a shows the output voltage  $V_{OUT}$  as a function

of the input voltage  $V_{IN}$  (solid line) of the inverter with  $L = 20 \mu\text{m}$  for both GFETs channels, for a fixed  $V_{DD} = 1 \text{ V}$ . The voltage gain  $A = |dV_{OUT}/dV_{IN}|$  is indicated by the dashed line. The device shows the characteristics of an inverter with a measured output voltage swing of about  $0.28 - 0.75 \text{ V}$  and a maximum voltage gain of  $2 \times 10^{-2}$ . It is worth noticing that an inverter with a voltage gain lower than unity is not functional for applications because it attenuates the input signal instead of amplifying it, resulting in a weaker output. Furthermore, it cannot be cascaded with other inverters since each stage would further reduce the voltage magnitude, leading to cumulative signal attenuation and rendering the cascaded system unusable. A voltage gain greater than unity could be achieved by optimizing the GFETs gate dielectrics and increasing the supply voltage  $V_{DD}$  [9], resulting however in an increase of the power dissipation. Fig. 3b shows the static power dissipation ( $P = V_{DD}I$ ) of the inverter in black, the power dissipated by  $R_p$  in red and the power dissipated by  $R_n$  in blue. The static power dissipation of the inverter, which is the sum of the power dissipated by  $R_n$  and  $R_p$  ( $P = R_n I^2 + R_p I^2$ ), is about  $50 \mu\text{W}$  and roughly independent from  $V_{IN}$ , and thus, the static power dissipation is substantial compared to conventional CMOS inverters. Therefore, the graphene inverters can only be employed for applications requiring high speed operation and where the power dissipation is not a concern.

Figs. 4a-d show the dynamic response of the inverter to digital signals with frequencies of 10 Hz, 100 Hz, 1 kHz and 10 kHz. The inverters characteristic shows well defined and stable output logic levels up to 10 kHz, where the signal distortion is attributed to low-pass filter of the high-voltage amplifier that was used to generate  $V_{IN}$  with a high logic level of 20 V. We note that the input voltage can be decreased by reducing the thickness of the  $\text{SiO}_2$  dielectric and the voltage supply adjusted, enabling a matching of the input and output voltage levels to achieve a functional inverter.

Fig. 5a shows the  $V_{OUT}$  vs  $V_{IN}$  characteristic of the inverters assembled with pairs of GFETs with  $L = 5, 10, 20, 50$  and  $100 \mu\text{m}$ . The corresponding voltage gains  $A$  are indicated by the dashed lines. The transfer characteristics of the different inverters display similar output voltage  $V_{OUT}$ , ranging from about  $0.3 \text{ V}$  to  $0.8 \text{ V}$ , and maximum voltage gain  $A$  of about  $2 \times 10^{-2}$ . Thus, the voltage swing  $V_{swing}$  and gain  $A$  are not affected by the scaling of the transistors channel length  $L$ . In contrast, the static power dissipation  $P$  ranges from about  $12 \mu\text{W}$ , for the device with the longest channels ( $L = 100 \mu\text{m}$ ), to about  $240 \mu\text{W}$  for the shortest device ( $L = 5 \mu\text{m}$ ), as shown in Fig. 5b. It is important to note that the relatively high power dissipation could limit the range of applications of the graphene-based inverters. To design devices that can meet the specific needs of applications in flexible electronics, it is crucial to find the right trade-off between power consumption and frequency response and thus, to understand how these parameters scale with the dimensions of the transistors.

Fig. 6 reports the static power dissipation and voltage gain of the inverters as a function of the channel length

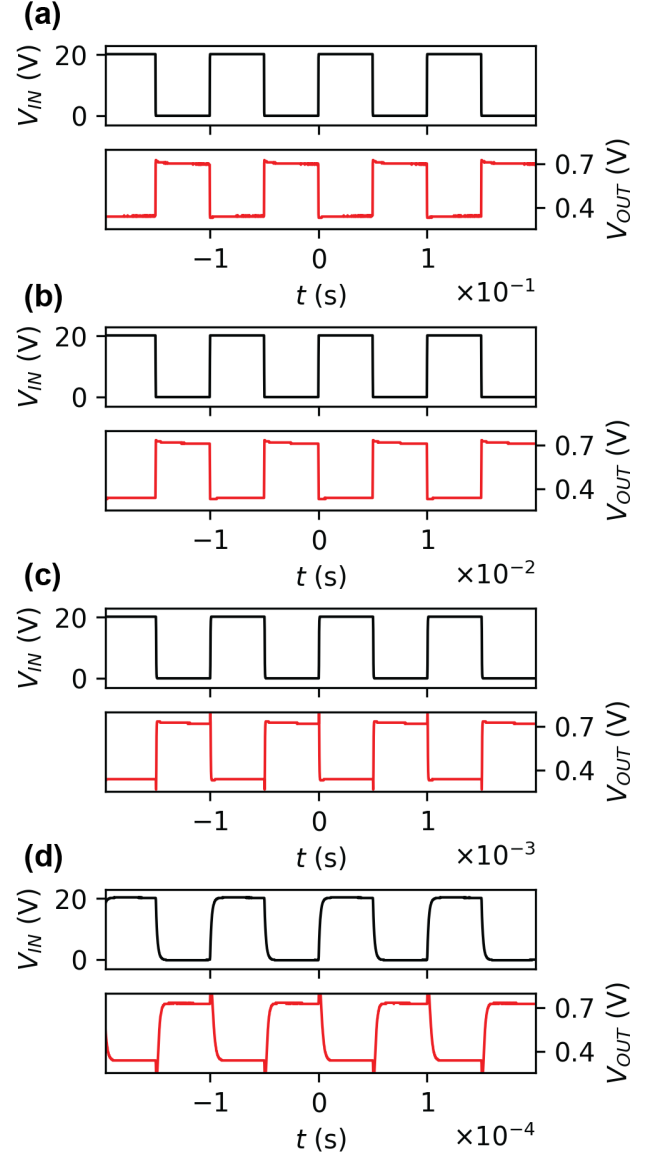


Fig. 4. Dynamic response of the the complementary inverter assembled with two representative GFETs with  $L = 20 \mu\text{m}$  and for  $V_{DD} = 1 \text{ V}$ . The frequency of the input signal  $V_{IN}$  (black) was set to: (a)  $f = 10 \text{ Hz}$ , (b)  $f = 100 \text{ Hz}$ , (c)  $f = 1 \text{ kHz}$ , and (e)  $f = 10 \text{ kHz}$ . The output voltage  $V_{OUT}$  is shown in red.

$L$ . We observe that static power dissipation scales as  $1/L$ , inversely proportional to the channel resistance ( $R_{n,p} \approx L/W$ ), while the voltage gain  $A$  is constant and about  $2 \times 10^{-2}$ . Therefore, the static power dissipation of the inverter can be tuned by varying the channel resistance, without affecting the output voltage swing and voltage gain. On the other hand, an increase of the channel resistance  $R_{n,p}$  correspond to a decrease of the inverter cut-off frequency. Considering the gate-oxide capacitance, i.e.  $C_{ox} = \epsilon_0 \epsilon_r L W / t$ , where  $\epsilon_0$  is the vacuum permittivity, while  $\epsilon_r = 3.9$  and  $t = 300 \text{ nm}$  are the dielectric constant and thickness of  $\text{SiO}_2$ , the cut-off frequency of the inverter is  $f_c \approx 1/(2R_{n,p} C_{ox}) \approx 1/L^2$ . Accordingly, the cut-off frequency of the graphene inverter shown in Fig. 2, with  $R_{n,p} \approx 4 \text{ k}\Omega$  and  $C_{ox} \approx 12 \text{ fF}$ , is approximately

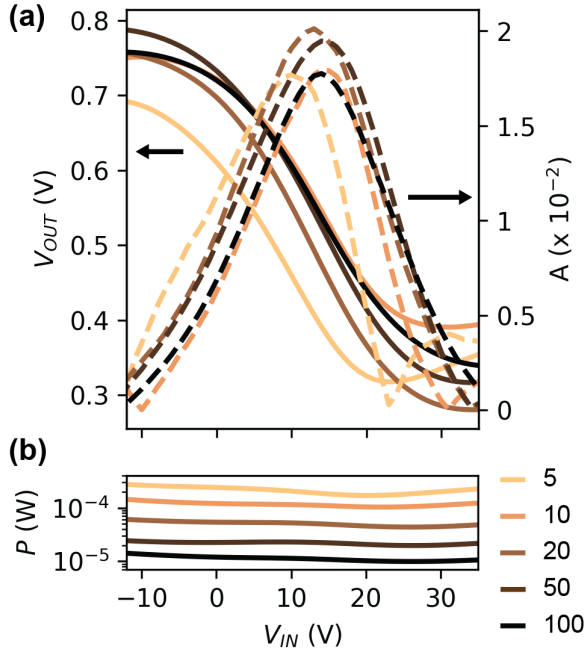


Fig. 5. Transfer characteristics of the complementary inverters. (a)  $V_{OUT}$  (solid lines) and voltage gain  $A$  (dashed lines) vs.  $V_{IN}$  and (b) Static power dissipation  $P$  vs.  $V_{IN}$  of the inverters with channel length  $L = 5, 10, 20, 50$  and  $100 \mu\text{m}$  and width  $W = 5 \mu\text{m}$ .

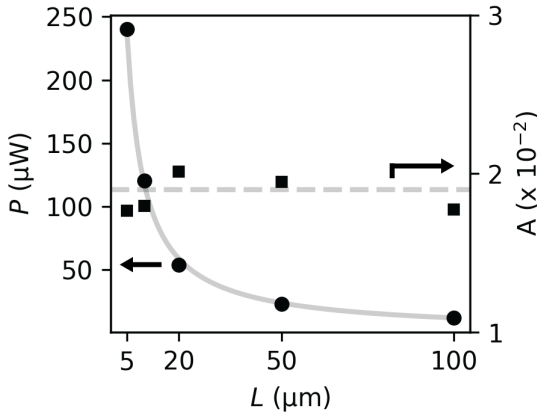


Fig. 6. Static power dissipation  $P$  (circles) and voltage gain  $A$  (squares) of the graphene complementary inverter vs. channel length  $L$ . The solid grey line shows the  $1/L$  trend of the static power dissipation. The dashed grey guideline indicates the constant voltage gain.

1.8 GHz. Nevertheless, the the actual cut-off frequency of the inverters is limited by the graphene channel resistance and the system load capacitance, as shown in the following circuit analysis.

Fig. 7a shows the equivalent electrical circuit of the arbitrary signal generator connected to the high-voltage amplifier, which has a cut-off frequency of 100 kHz and an output resistance  $R_{HV} = 10 \Omega$  ( $C_{HV} = 160 \text{ nF}$ ), and of the oscilloscope channel 1, which is modeled by the parallel input resistance  $R_{CH1} = 1 \text{ M}\Omega$  and capacitance  $C_{CH1} = 20 \text{ pF}$ . Fig. 7b shows the equivalent electrical circuit of the graphene complementary inverter, where the gate-to-source capacitance of the single GFET is calculated

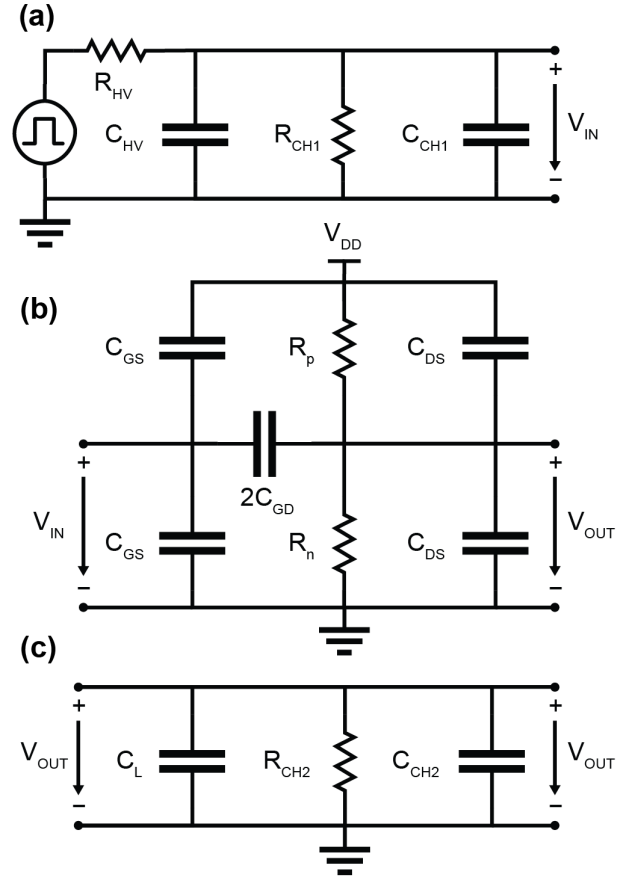


Fig. 7. (a) Equivalent circuit of the digital signal generator including the 1 V square waveform generator, the 10x high-voltage amplifier with a 100 kHz low-pass filter and an output resistance  $R_{HV} = 10 \Omega$ , and the oscilloscope channel 1 with  $R_{CH1} = 1 \text{ M}\Omega$  and  $C_{CH1} = 20 \text{ pF}$ . (b) Equivalent circuit of the complementary inverter with  $C_{GS} = 5 \text{ pF}$  and  $C_{DS} = 40 \text{ pF}$ . (c) Measured load capacitance  $C_L = 250 \text{ pF}$  and the oscilloscope channel 2, with  $R_{CH2} = 1 \text{ M}\Omega$  and  $C_{CH2} = 20 \text{ pF}$ .

as  $C_{GS} = C_{PAD} + C_{ox} \approx C_{PAD} = 5 \text{ pF}$ . Since the geometrical capacitance of the Au metal pads  $C_{PAD}$  is large (the surface is  $A = 150 \mu\text{m} \times 150 \mu\text{m}$ ), the gate-oxide capacitance can be neglected. The drain-to-source capacitance  $C_{DS} = 40 \text{ pF}$  was measured with the LCR meter. The resistances  $R_p$  and  $R_n$  were modeled by a polynomial of the form  $R(V_{IN}) = aV_{IN}^3 + bV_{IN}^2 + cV_{IN} + d$ , which coefficients were obtained by fitting the polynomial to the data shown in Fig. 9 of the Appendix. Fig. 7c shows the equivalent electrical circuit of the output measurement setup including the load capacitance  $C_L$ , which takes into account the cables and instrumentation, and the oscilloscope channel 2, which is modeled by the parallel input resistance  $R_{CH2} = 1 \text{ M}\Omega$  and capacitance  $C_{CH2} = 20 \text{ pF}$ .

Fig. 8a shows the measured (solid black line) and simulated (dashed red line) input voltage. The time constant of the system is given  $\tau \approx RC$ , where  $R \approx R_p // R_n$  and  $C \approx C_L > C_{ox}$ . Accordingly, increasing the length of the graphene channels leads to higher resistance  $R$ , and therefore, a slower time response, as shown in Fig. 8b. On one hand, the capacitive loading of the output, which is mostly due to the measurements instruments, can

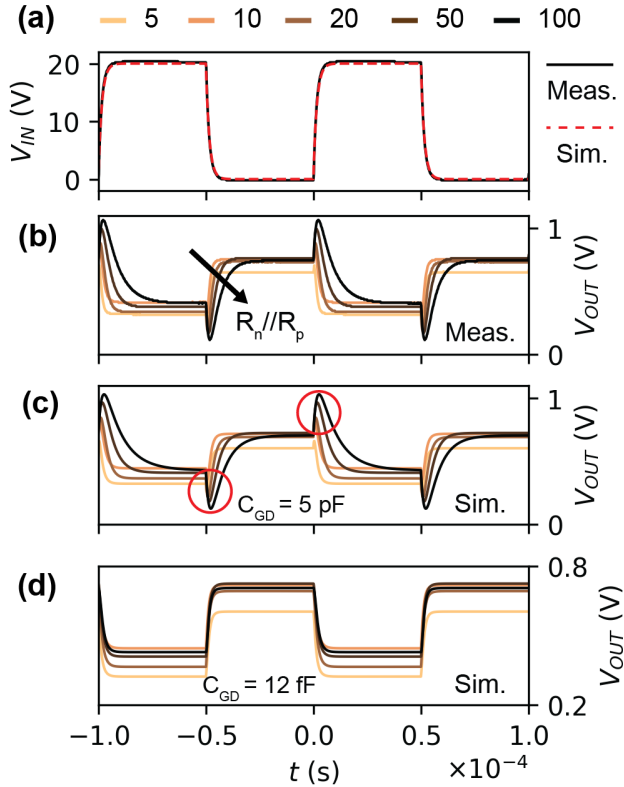


Fig. 8. Dynamic response of the inverters to digital input signal with frequency  $f = 10$  kHz. (a) Measured (solid black line) and simulated (dashed red line) input voltage  $V_{IN}$ . (b) Measured output voltage  $V_{OUT}$  of the inverters with channel length  $L = 5, 10, 20, 50$  and  $100 \mu\text{m}$  and width  $W = 5 \mu\text{m}$ . (c) Simulated output voltage  $V_{OUT}$ . (d) Simulated output voltage  $V_{OUT}$  for an optimized circuit, where  $C_{GS} = C_{GD} = C_{DS} = C_{ox} = 12$  fF.

be reduced to  $C \approx C_{ox}$  by integrating the devices on a single chip, and therefore, enabling an higher operational frequency. On the other hand, the capacitance of the metal interconnects  $C_{PAD}$  can be minimized by implementing a local gate. This would result in a reduction of the gate-to-drain capacitance to  $C_{GD} = C_{PAD} + C_{ox} \approx C_{ox}$  and would avoid the loading curves circled in red in Fig. 8c. In fact, the circuit simulation with optimized interconnects, i.e.  $C_{PAD} \approx 0$  F, no longer produces these loading curves, as shown in Fig. 8d. We note that the reduction of the dielectric thickness will not only enable the matching of the input and output voltage levels but will also increase the gate oxide capacitance, leading to a slower time response of the inverter.

### III. CONCLUSIONS

In summary, the devices presented in this work, which were assembled using C60 and Pentacene doped GFETs, demonstrated the characteristics of complementary inverters. The results set a promising base to the subsequent fabrication of an integrated inverter. From our results, we anticipate that the fabrication of functional inverters operating in the GHz frequency regime should be possible by integrating the GFETs on a single chip, reducing the dielectric thickness, and optimizing the metal interconnects, all steps being feasible with current state-of-the-art

fabrication processes.

## IV. EXPERIMENTAL METHODS

### A. Device Fabrication

The fabrication process of Graphene Field Effect Transistors (GFETs) and the deposition of C60 and Pentacene thin films are described. A more detailed description of the GFETs fabrication process, including information on the Chemical Vapor Deposition (CVD) of graphene, can be found elsewhere [5], [10], [11], [12]. Briefly, the CVD graphene foils were wet transferred on Si/SiO<sub>2</sub> (525 μm / 300 nm) substrates with pre-patterned Ti/Au (5 nm / 50 nm) electrodes. The graphene was then patterned using e-beam lithography and Reactive ion etching (RIE) to create geometrically defined channels with lengths  $L = 5, 10, 20, 50, 100 \mu\text{m}$  and width  $W = 5 \mu\text{m}$ . Thin films of C60 (about 10 nm) and Pentacene (about 5 nm) were thermally evaporated onto two separate GFET chips, which were subsequently connected with electrical measurement probes to realize a complementary inverter.

### B. Electrical Characterization

All the devices were measured under vacuum ( $1 \times 10^{-6}$  mbar) and at room temperature (293 K). A Semiconductor Parameter Analyzer Keithley 4200 was used for the I-V characterization. The square wave signals (0 – 2 V) were generated using a Tektronix AFG 3102 that was connected to a high-voltage amplifier (Basel SP908) to provide the digital input voltage  $V_{IN}$  (0 – 20 V). The positive voltage  $V_{DD} = 1$  V was supplied by a Yokogawa 7651 DC source. The input and output voltages were measured using a Tektronix TDS 2024C oscilloscope. The device and load capacitances were measured with a BK Precision 895 LCR meter.

### C. Data Analysis and Circuit Simulation

Python scripts were used for the data analysis and visualization of the acquired data. Numpy and Scipy libraries were mainly used for the processing and fitting of the measured data. Only the continuous backward sweep of the transfer characteristics were considered for the analysis. The measurement setup and the complementary inverter circuits were simulated using LTspice 17.1.18.

## APPENDIX

Fig. 9 shows (a) output characteristic ( $I$  vs  $V_{DD}$ ) and (b) transfer resistances ( $R$  vs  $V_{IN}$ ) of the graphene complementary inverters. For the circuit simulations, the resistances  $R_{n,p}(V_{IN})$  were extrapolated by fitting a polynomial in the range 0 - 20 V.

Table I provides the main parameters of the graphene inverters that were fabricated and measured in this study. The parameters were extrapolated at fixed  $V_{DD} = 1$  V and for a digital input signal within 0 V to 20 V. The voltage swing is given by  $V_{swing} = V_{OH} - V_{OL}$ , while the static power dissipation is calculated at  $V_{in} = 0$  V and the cut-off frequency of the inverters is calculated as  $f_c = 1/4\pi R_{n,p} C_{ox}$ . Assuming that the channel dimensions uncertainty ( $\Delta L$  and  $\Delta W$ ) is approximately  $0.2 \mu\text{m}$  and

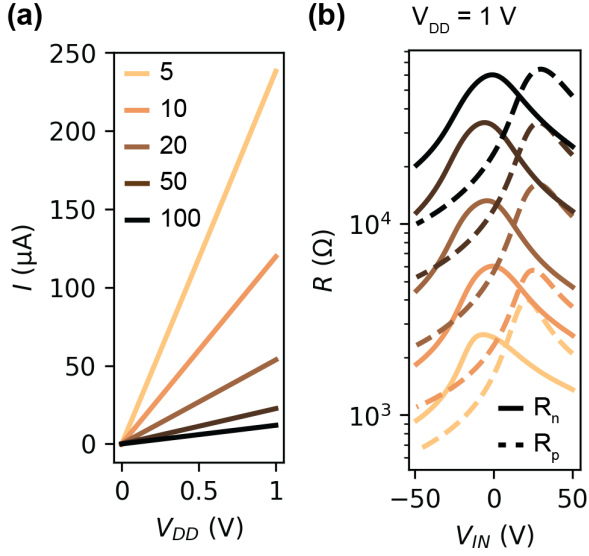


Fig. 9. (a)  $I$  vs.  $V_{DD}$  for channel length  $L = 5, 10, 20$  and  $50 \mu\text{m}$ . (b)  $R_n$  (solid line) and  $R_p$  (dashed line) vs  $V_{IN}$  of the inverter for channel length  $L = 5, 10, 20$  and  $50 \mu\text{m}$ , at  $V_{DD} = 1\text{V}$ .

TABLE I  
PARAMETERS OF THE GRAPHENE COMPLEMENTARY INVERTERS.

$L$ ( $\mu\text{m}$ )	$V_{swing}$ (V)	$A$ ( $10^{-2}$ )	$P$ ( $\mu\text{W}$ )	$f_c$ (GHz)
$5 \pm 0.2$	$0.29 \pm 0.04$	$1.77 \pm 0.10$	$240 \pm 9.8$	$27.9 \pm 1.47$
$10 \pm 0.2$	$0.28 \pm 0.03$	$1.79 \pm 0.08$	$120 \pm 3.9$	$8.29 \pm 0.18$
$20 \pm 0.2$	$0.33 \pm 0.03$	$2.01 \pm 0.08$	$54 \pm 1.4$	$1.77 \pm 0.02$
$50 \pm 0.2$	$0.32 \pm 0.03$	$1.95 \pm 0.08$	$25 \pm 0.6$	$0.32 \pm 0.00$
$100 \pm 0.2$	$0.28 \pm 0.03$	$1.78 \pm 0.07$	$12 \pm 0.3$	$0.08 \pm 0.00$

that the graphene sheet resistance is about  $R_{S,n} \approx 3\text{k}\Omega$ , the uncertainty of  $V_{swing}$  is calculated as follows:

$$\Delta V_{swing} \approx R_{S,n} I_{DD} \sqrt{\left(\frac{\Delta L}{W}\right)^2 + \left(\frac{L\Delta W}{W^2}\right)^2} \quad (1)$$

while the power uncertainty is approximately  $\Delta P = \Delta V_{swing} I_{DD}$ , and the frequency  $f_c$  uncertainty is given by:

$$\Delta f_c \approx \frac{t}{\pi R_{S,n} \epsilon_0 \epsilon_r} \sqrt{\left(\frac{\Delta L}{L^3}\right)^2} \quad (2)$$

Similarly, the error on the voltage gain  $A$  is extrapolated from the expression:

$$\Delta A \approx A \sqrt{\left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \quad (3)$$

However, the variability between graphene-based inverters possibly depends on other factors, including the sheet and contact resistance of graphene. For detailed statistics on the variability between GFETs, refer to [5].

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