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# Boosting room temperature tunnel magnetoresistance in hybrid magnetic tunnel junctions under electric bias

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## Abstract

Spin-resolved electron symmetry filtering is a key mechanism behind giant tunneling magnetoresistance (TMR) in Fe/MgO/Fe and similar magnetic tunnel junctions (MTJs), providing room temperature functionality in modern spin electronics. However, the core process of the electron symmetry filtering breaks down under applied bias, dramatically reducing the TMR above 0.5 V. This strongly hampers the application range of MTJs. To circumvent the problem, resonant tunneling between ferromagnetic electrodes through quantum well states in thin layers has been used so far. This mechanism, however, is mainly effective at low temperatures. Here, a fundamentally different approach is demonstrated, providing a strong TMR boost under applied bias in V/MgO/Fe/MgO/Fe/Co hybrids. This pathway uses spin orbit coupling (SOC) controlled interfacial states in vanadium, which contrary to the V(001) bulk states are allowed to tunnel to Fe(001) at low biases. The experimentally observed strong increase of TMR with bias is modelled using two nonlinear resistances in series, with the low bias conductance of the first (V/MgO/Fe) element being boosted by the SOC-controlled interfacial states, while the conductance of the second (Fe/MgO/Fe) junctions controlled by the relative alignment of the two ferromagnetic layers. These results pave a way to unexplored and fundamentally different spintronic device schemes, with tunneling magnetoresistance uplifted under applied electric bias.

## I. INTRODUCTION

Nearly two decades after atomistic calculations predicted the giant TMR due to symmetry resolved coherent tunneling<sup>1,2</sup>, this effect is currently one of the basic electron transport mechanisms in most of spintronics sub-branches, ranging from magnetoresistive random access memories and programmable logic elements<sup>3</sup> to magnetic sensors<sup>4</sup>. The theoretically predicted several-thousand-percent zero bias TMR is, in practice, reduced an order of magnitude due to interface inter-diffusion, roughness or surface states.

However, even more humbling basic characteristic of single barrier MTJs is a *strong monotonic reduction of the TMR with voltage*, on the scale of about 0.5 V<sup>5-9</sup>. For the case of incoherent tunneling in non-epitaxial junctions, the reduction is mainly caused by itinerant tunnel electrons with excess energy above the Fermi level ( $E_F$ ) (the so-called “hot electrons”)<sup>10</sup>. These electrons, which are generated with increasing bias and temperature, are able to excite magnons at the FM/I interface, which in turn favour spin-flip events in the tunneling process<sup>11</sup>. While this is not relevant for a spin valve in the parallel (P) configuration (since no change in spin is necessary for the transport), it is significant in the anti-parallel (AP) configuration, increasing the transmission and thus reducing the resistance difference with the P state. For the coherent tunneling case, as in our epitaxial junctions, the scenario involves the band-to-band transmission of electrons preserving the orbital symmetry<sup>8</sup>. The applied bias increases the coupling between the two FM electrodes, creating new channels that enhance the transmission in the AP state faster than in the P state<sup>7</sup>.

So far, a few different approaches have been used to compensate the main shortcoming of MTJs for the applications: (i) optimising the ferromagnetic electrodes (F1,F2) or barrier (I) in F1/I/F2 MTJs, (ii) enhancing the conductance for specific biases through resonant tunneling via quantum well states (QWS) inside the barrier in F1/QWS/I/F2 MTJs, or (iii) sequential tunneling in F1/I/F2/I/F3 double barrier MTJs (DMTJs).

Within the first approach (i), asymmetric single barrier junctions have been proposed in order to partially mitigate the electric-field-induced TMR degradation, suppressing the conductance through surface states for some bias polarity<sup>12</sup>. On the other hand, the incorporation of EuS spin-filter barriers<sup>13</sup> is only operative below the EuS Curie temperature ( $T_C = 17$  K).

Spin-dependent resonant tunneling through quantum-well<sup>14,15</sup> and interface<sup>12</sup> states investigated within line (ii) showed that devices are either operative at low temperatures only or involve technically challenging symmetry confinement in a few mono-layers of ferromagnetic material<sup>16</sup>. Other similar<sup>17</sup> approaches providing TMR modulation are also not robust enough to build energy efficient<sup>18</sup> room temperature spintronic devices. Finally, within the approach (iii) only a TMR suppression slower than the expected for two independent MTJs in series has been achieved in standard DMTJs<sup>19</sup>, while showing a steady TMR decay with bias<sup>20,21</sup>.

In this study we demonstrate a radically different and breakthrough approach to solve the long standing problem. We report an electric-bias-induced 2-3 fold increase of the TMR in hybrid MTJs (H-MTJs) of V/MgO/Fe/MgO/Fe/Co (NS/I/F1/I/F2 with NS being a normal metal with surface states) in a wide temper-

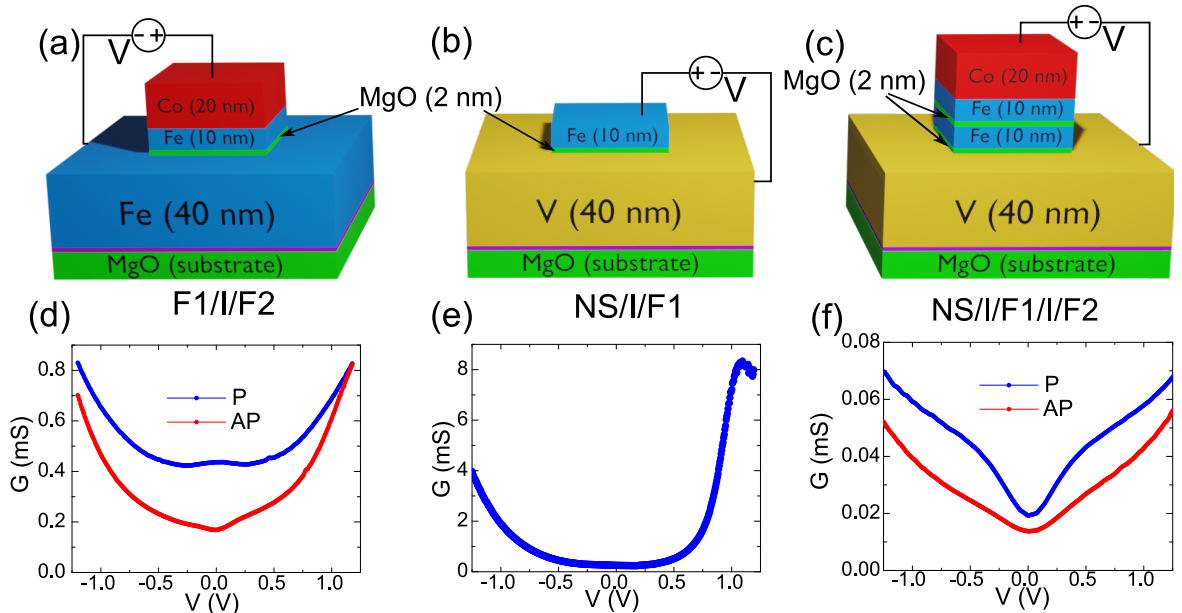


FIG. 1: (a), (b) and (c) show sketches of the F1/I/F2 (control samples), NS/I/F1 and NS/I/F1/I/F2 junctions under study, respectively. Vanadium (001) is the NS electrode, while F1 and F2 are the respectively magnetically soft Fe(001) and hard (sensing) Fe(10 nm)Co(20 nm) ferromagnetic layers. (d) Shows conductance curves in the P and AP configurations of a control sample at room temperature. Part (e) shows the high bias conductance in a V/MgO/Fe junction at room temperature, evidencing the conductance variation with voltage of the NS/I/F1 junctions, of nearly two orders of magnitude below 1 V. Part (f) shows the high bias conductance in a V/MgO/Fe/MgO/Fe/Co junction in the P (blue) and AP (red) alignments of the ferromagnetic electrodes, also at room temperature.

ature range, from liquid helium to room temperatures. The *output voltage* parameter, which is crucial for possible applications<sup>21–24</sup>, strongly exceeds the values observed for single barrier F1/I/F2 MTJs at biases above 0.5 V. Moreover, to our best knowledge, the room temperature value exceeding 0.8 V are a record high for all known spintronic devices. We explain this unprecedented behavior with a simplified model, considering magnetic-state-dependent sequential tunneling through two nonlinear devices in series. The conductance of the first element (V/MgO/Fe) is essentially controlled by SOC and symmetry protected surface states, while the conductance of the second (Fe/MgO/Fe/Co) is given by its magnetic state.

## II. EXPERIMENTAL RESULTS

Details on the samples fabrication and measurement procedures are explained in the Methods section. Figure 1 introduces the experimental configurations for the F1/I/F2 control samples, the NS/I/F1 single barrier and the NS/I/F1/I/F2 double barrier hybrid structures. Panels a, b and c sketch the structure of each junction respectively, while panels d, e and f compare the bias dependencies of the conductance for the type of sample shown above. The lateral size of all the studied junctions is  $20 \times 20 \mu\text{m}^2$  unless otherwise stated. The conductance of

V/MgO/Fe shows a very strong bias dependence reaching about a  $\times 3$  increase up to 0.5 V and a  $\times 100$  up to 1.3 V. Figure 1f demonstrates that for the broad low bias range below about 0.5 V, the conductance of the NS/I/F1/I/F2 junction varies much more with bias in the P state compared to the AP state. This is clearly an opposite behavior with respect to the one observed in F1/I/F2 junctions (Figure 1d).

### A. Bias enhanced TMR and dependence on temperature and junction size

Figure 2 compares the bias dependence of TMR for the single and double barrier spin valve structures.

The TMR is calculated as the relative conductance difference between the parallel (P) and antiparallel (AP) states of the two ferromagnetic layers:

$$\text{TMR} = \frac{G_P - G_{AP}}{G_{AP}} \times 100 \quad (1)$$

For the Fe/MgO/Fe/Co single barrier structures (F1/I/F2), TMR is maximum near  $V = 0$  V, and decreases with increasing bias. On the contrary, for NS/I/F1/I/F2 H-MTJs the TMR first increases with voltage, until a maximum is reached near  $V = 0.5$  V,

and then starts to decrease. This behavior is further enhanced at low temperatures, as can be seen in Figure 2.

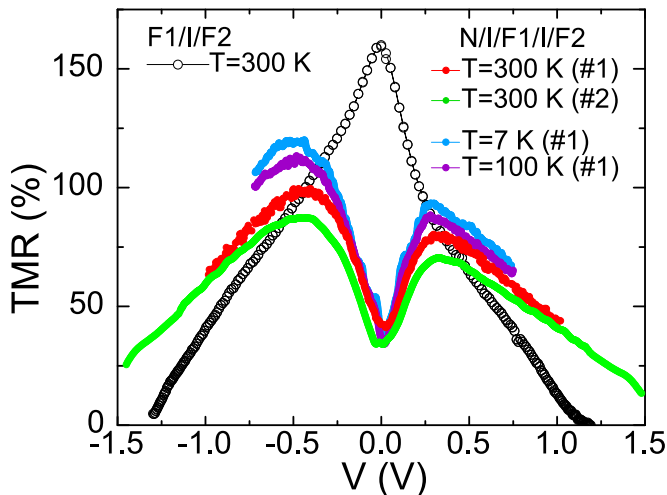


FIG. 2: Comparative of TMR vs applied bias for several different H-MTJs at different temperatures. Light blue ( $T = 7$  K), purple ( $T = 100$  K), red and green ( $T = 300$  K) curves correspond to two different N/I/F1/I/F2 junctions, labeled as #1 and #2 in the legend. The curve with black open dots corresponds to a Fe/MgO/Fe/Co control sample at  $T = 300$  K.

### B. Bias dependence of output voltage

Besides the TMR vs bias determined from the differential conductance, we have also analyzed a related parameter which is important for applications, namely the output voltage of the device<sup>21–24</sup>, defined as

$$\Delta V = |V| \times \frac{R_{AP} - R_P}{R_P} \quad (2)$$

where the magnetoresistance is now defined from the resistance instead of the conductance. We observed that the output voltage  $\Delta V$  in MTJs is higher than the one of H-MTJs only at low biases (see Figure 3). For H-MTJ devices, the output voltage monotonously increases with voltage at room temperature practically in the whole measured range, exceeding 0.8 V at an applied bias of 1.5 V, while for the single barrier MTJs it peaks at  $V \sim 0.7$  V. The maximum  $\Delta V$  reached exceeds previous record values in Fe/C/MgO/Fe tunnel junctions, which were also obtained with an applied bias of 1.5 V<sup>25</sup>.

## III. DISCUSSION

Below we discuss two most important properties of the V/MgO interface explaining the unexpected TMR vs bias

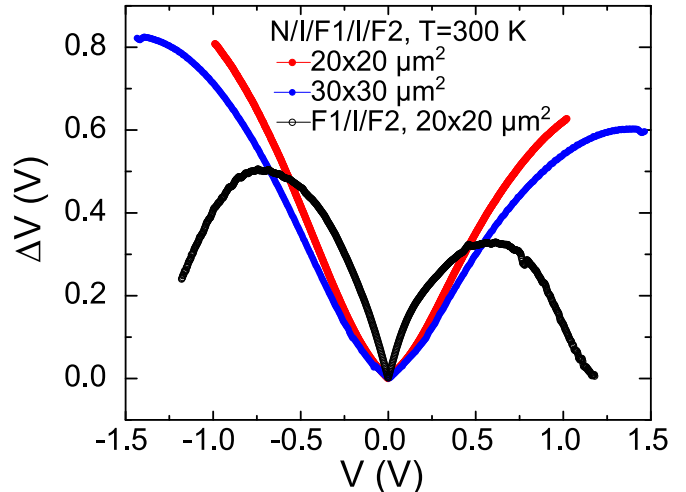


FIG. 3:  $\Delta V$  vs applied bias at room temperature for a control sample (black) and two H-MTJs of different lateral sizes (red is a  $20 \times 20 \mu\text{m}^2$  blue a  $30 \times 30 \mu\text{m}^2$  one).

behavior. Its strongly nonlinear conductance response to the applied bias is due to (i) extremely low zero bias conductance (as indicated by the experiments, see Figure 1) and the presence of surface states with an electron symmetry fundamentally different from the bulk one.

Our *ab-initio* calculations (Figure 4a-c), in line with previous studies<sup>26</sup>, explain the very low zero bias conductance in V/MgO/Fe as only a single bulk band with  $\Delta_2$  symmetry crosses the Fermi energy in the [100] direction (normal to the interface). The  $\Delta_2$  symmetry states, however, are absent at the Fe(001) Fermi level. Even if they were present, the corresponding electron transmission would be completely filtered out by the MgO(001)<sup>1</sup>. On the other hand, the  $\Delta_5$  band in V is situated 0.5 eV above  $E_F$  and it is also strongly attenuated by the MgO<sup>1</sup>. Therefore, the low bias electron (spin) transport through V/MgO/Fe from the  $\Delta_2$  states in Vanadium could be possible if  $\Delta_2$  to  $\Delta_1$  symmetry transformation takes place close to the V/MgO interface. This peculiar property of the V band structure was previously explored by the insertion of thin Vanadium layers into hybrid Fe/V/Fe/MgO/Fe MTJs, which provided an increase of TMR up to 800000% through the creation of QWSs for  $\Delta_1$  electrons confined inside the soft Fe layer between the MgO and Vanadium<sup>26</sup>.

Interestingly, our *ab-initio* simulations disclose that the surface atomic layers at the V/MgO interface have  $\Delta_1$  symmetry. Moreover, the numerical results also reveal that the vanadium surface states at the V/MgO interface provide a low bias (below 100 mV) peak in the density of states (DOS), in qualitative agreement with scanning tunneling spectroscopy measurements on V(001)<sup>27</sup>. Most importantly, though, the simulations show a strong increase of the vanadium surface DOS peak with the inclusion of interfacial SOC and a relatively weak trans-

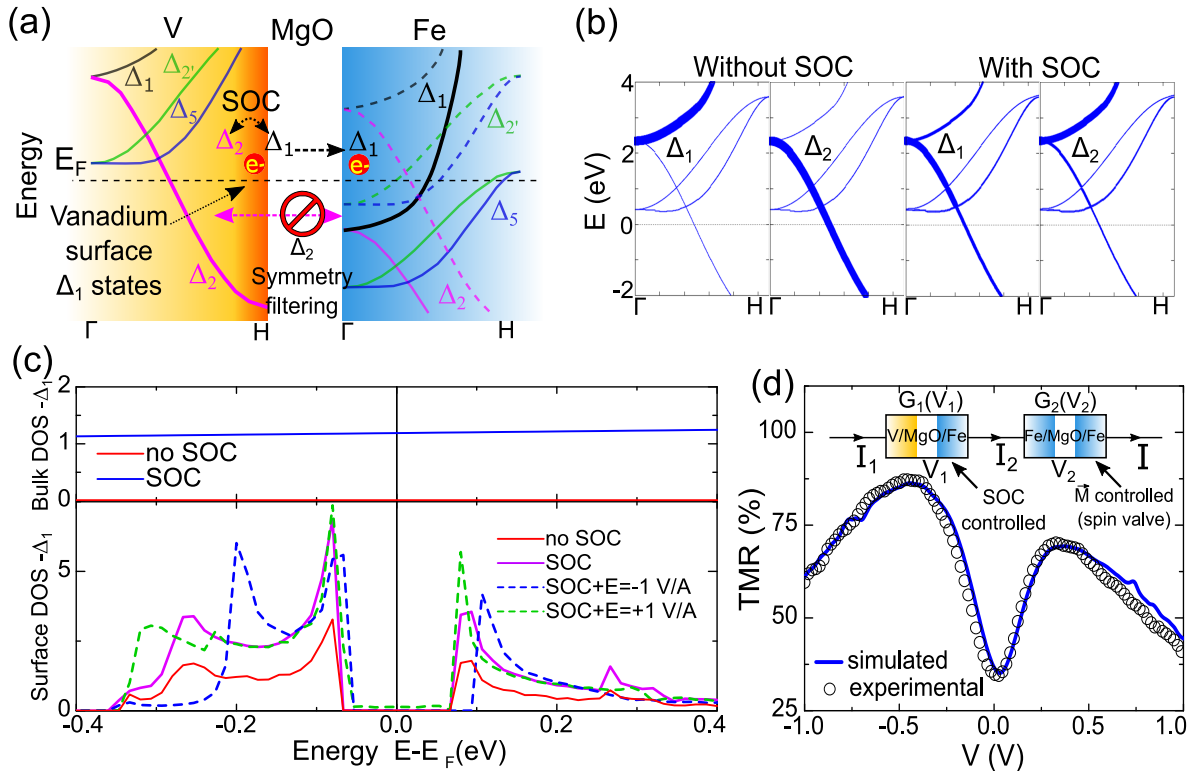


FIG. 4: (a) Sketch of the band structure of the V/MgO/Fe system, including the vanadium  $\Delta_1$  surface states, representing the main transport mechanism involving interfacial SOC and symmetry filtering in the MgO. Similar results have been obtained in Ref.<sup>26</sup>. In the Fe part, solid lines indicate the bands for the main spin population, while dashed lines are used for the minority spin population bands. (b) Band structure of the V layer, in the absence of SOC (first 2 panels) and with SOC (third and fourth), where the thickness of the band line is proportional to the indicated electron symmetry. This is used to calculate the DOS in (c), which shows the  $\Delta_1$  density of states (DOS) in the Vanadium electrode, both in the bulk (upper part) and the surface (below), where new states appear around  $\pm 0.1$  eV from the Fermi energy in the presence of SOC and electric field. (d) The TMR( $V$ ) characteristic of the hybrid double barrier V/MgO/Fe/MgO/Fe/Co structure can be modelled as two in series nonlinear devices (sketch shown in inset). The system is solved considering the experimental  $G_2(V_2)$  in P and AP configurations for the F1/F2 barrier and a parametrized  $G_1(V_1)$  of the N/F1 barrier, adjusted to obtain the best fit of the final TMR( $V$ ) curve for the N/F1/F2 junction.

formation under electric fields up to 1 V/Angstrom (see lower part in Figure 4c). The effect of the SOC on the DOS is pronounced because the Fermi level without SOC lies within a gap for the  $\Delta_1$  electrons (DOS from Figure 4c is a histogram of the band along the  $\Gamma$ -H ( $\Delta$ ) line,  $\pm 0.4$  eV around  $E_F$ ), which is quenched when the SOC is turned on because of the symmetry mixing ( $\Delta_1$  gets scattered into  $\Delta_2$  and vice versa, as shown in Figure 4b), so the DOS gap gets filled with these states. There is also no  $\Delta_5$  at  $E_F$  without SOC, while with SOC  $\Delta_5$  (not shown in the Figure) and  $\Delta_1$  symmetries appear. Therefore, the enhancement of DOS when SOC is turned on mainly reflects the creation of  $\Delta_1$  from  $\Delta_2$ .

These results allow for a simple qualitative explanation of the main finding. As long as the switching of the device between the P and AP states redistributes the total voltage between the two parts (V/MgO/Fe and Fe/MgO/Fe/Co), the low bias conductance should increase faster with the total bias in the P state rather

than in the AP state, due to the presence of the interfacial DOS peak providing the increase of TMR in the low bias regime.

Quantitatively, the TMR( $V$ ) characteristic of the hybrid double barrier V/MgO/Fe/MgO/Fe/Co structure can be explained based on individual current-voltage characteristics of the bottom V/MgO/Fe and top Fe/MgO/Fe/Co MTJ subsystems considered as in series nonlinear devices (Figure 4d inset). This decomposition in serial devices can be done because the 10 nm thickness of the middle Fe layer, larger than the coherence length for both the majority and minority spins, prevents coherent tunnelling across the two barriers. Therefore, the transport mechanisms in the double barrier N/F1/F2 junction is a sequential tunnelling in N/F1 and F1/F2 in series MTJs. However, the simulation of the serial device characteristics is not a simple voltage divider problem, because the voltage distribution on each component depends on the individual voltage-

dependent nonlinear resistance. Therefore, the in-series circuit problem requires the resolution of a nonlinear circuit equations. This can be done in few steps, by considering the Kirchhoff voltage and current laws (KVL, KCL): (i) The KCL charge continuity condition, written as  $I_1 = I_2 = I$  (where  $I_1$  and  $I_2$  are the currents passing through the N/F1 and F1/F2 barriers respectively), allows to determine the corresponding individual voltage drops  $V_1$  and  $V_{2(P/AP)}$  at each barrier from the individual  $i(V)$  characteristics of the N/F1 and F1/F2 nonlinear resistors. (ii) Then, the KVL will provide the total voltage drop on the serial device  $V = V_1 + V_{2(P/AP)}$  for the current  $I$  for which we determined the individual voltage drops. (iii) Finally, the serial circuit conductance would be  $G_{P/AP}(V) = I/V$  and the corresponding  $TMR(V) = [G_P(V) - G_{AP}(V)]/G_{AP}(V)$ . This algorithm has been applied in our case considering as initial individual characteristics the experimental  $G_2(V)$  in P and AP configurations (denoted as  $G_{2(P/AP)}(V)$ ) for a F1/F2 MTJ, and a parametrized characteristic for the N/F1 junction issued from the fit of the experimental  $G_1(V)$  of a N/F1 junction, adjusted to obtain the best fit of the final  $TMR(V)$  curve for the N/F1/F2 junction. The result of this simulation (Figure 4(d)) explains the TMR variation with voltage in the hybrid double barrier MTJ in terms of competition between two main effects: (i) the standard decrease with voltage of the TMR in the top Fe/MgO/Fe/Co (F1/F2) MTJ (see Figure 2) and (ii) the voltage induced increase in conductivity in the bottom V/MgO/Fe (N/F1) MTJ.

The relatively low TMR at small biases is mainly a consequence of the low conductance of the Fe/MgO/V tunnel barrier (see Figure 1), which provides an additional fixed resistance to the junction, therefore reducing the relative resistance difference between the P and AP states (i.e. the TMR). On the other hand, the same Fe/MgO/V interface is directly responsible for the enhancement of the TMR with applied bias. Its characteristic  $G(V)$  behavior allows the P and AP conductances to diverge, increasing the TMR up to  $\sim 0.5$  V where it becomes higher than for similar single barrier MTJs (Figure 2), compensating the drawback at low bias with an advantage at intermediate and high voltages. At the same time, the fixed resistance of the Fe/MgO/V interface will increase the resistance-area product (RA) of the structure, which is another important parameter for applications. To the best of our knowledge, there isn't any MTJ structure that allows for both an increasing of the TMR with bias and a low RA, although thinner tunnel barriers may allow for qualitatively similar behavior with a lower RA (calculations are, in fact, done with thinner barriers since the 2-3 nm of MgO are computationally prohibitive to simulate). While the reduction of the RA factor is important for applications in memory elements, it's not so crucial for magnetic sensors where the increasing of TMR with voltage could be a bigger advantage.

## IV. CONCLUSION

In summary, we introduce conceptually new hybrid magnetic tunnel junctions, consisting of standard MTJs sequentially coupled to a strongly nonlinear part, where the conductance is mainly provided by SOC-controlled interfacial states with symmetries different from the bulk states. This configuration provides a robust increase of the TMR with bias up to 0.5 V in a wide temperature range and unprecedented for room temperature spintronics high output voltage values. Our approach demonstrates the importance of the electron-symmetry-protected surface states in metallic interfaces, and is expected to push the applicability range of spintronic devices towards higher biases.

## V. METHODS

### A. Samples growth and characterization

The MTJ multilayer stacks have been grown by molecular beam epitaxy (MBE) in a chamber with a base pressure of  $5 \times 10^{-11}$  mbar following the procedure described in Ref.<sup>28</sup>. The samples were grown on (001) MgO substrates. Then, a 10 nm thick seed of anti-diffusion MgO underlayer is grown on the substrate to trap the C from it before the deposition of the Fe (or V). Then, the MgO insulating layer is epitaxially grown by e-beam evaporation, the thickness being approximately  $\sim 2$  nm, and so on with the rest of the layers. Each layer is annealed at 450 °C for 20 mins for flattening. After the MBE growth, all the MTJ multilayer stacks are patterned in micrometres-sized square junctions by UV lithography and Ar ion etching, controlled step-by-step *in situ* by Auger spectroscopy.

### B. Experimental measurement methods

The measurements are performed using room temperature<sup>9</sup> and low temperature<sup>29,30</sup> setups. The first consists of a sample holder inside a small low vacuum chamber, which is connected to a Keithley 2700 current source and a DMM-322 PCI voltmeter card, both controlled by a computer. The magnetic field used to switch the magnetic states is applied using a solenoid connected to a KEPCO 10-100 current/voltage source., which is also controlled with the computer. Low temperature measurements are based on a JANIS He<sup>3</sup> cryostat (the minimum attainable temperature is 0.3 K). The magnetic field is varied using a 3D vector magnet consisting of one solenoid (Z axis) with  $H_{max} = 3.5$  T and two Helmholtz coils (X and Y axis) with  $H_{max} = 1$  T. The temperature is measured and controlled using a LakeShore 340 controller. The current is applied with a Keithley K220 current source, and the voltage is measured with a DMM-552 PCI voltmeter card.

In both experimental configurations, the different magnetic states are obtained as follows: first, the field is set to  $H = 1000$  Oe (in the in-plane direction of the sample) saturating the magnetization of the two ferromagnetic layers, and then going back to zero field obtaining the P state. The AP state is obtained by applying a small magnetic field in the opposite direction, not exceeding the hard ferromagnetic layer coercive field of about 500 Oe.

### C. Ab-initio calculations methods

The electronic structure calculations have been performed within a Full-Potential-Linear-Augmented-Plane-Wave method provided by the Wien2k code<sup>31</sup>. A supercell model has been used to describe the surface features. The symmetry dependent densities of states are calculated as histograms from the dispersion bands  $E(k)$  along the corresponding high symmetry directions (e.g.

$\Gamma-H = \Delta$ ). The results are in full agreement with LKKR calculations from Ref.<sup>26</sup>.

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