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Current sensing for SiC Power Devices

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Abstract: High voltage, high current capabilities of SiC based devices has been already proved, and high current SiC devices working at high temperature are susceptible to be on the market soon. SiC power integration will have to be considered as a further development step to discrete power devices. Packaging and device integrated protections remain the main constrains for high temperature operation and system integration. In case of short-circuit or over-current, SiC devices can reach high temperature values, and die might be subjected to high stresses. In order to address such critical requirements, current sensing and real time temperature monitoring are mandatory. The structure proposed in this paper, derived from Si technology, provides a protection feature to SiC power devices to get reliable high temperature electronics. Concretely, an integrated current sensor has been implemented in a vertical power SiC JFET and its fabrication is reported for the first time. The current sensor layout and process technology are presented. An experimental current sensing validation is also reported.

Introduction

High voltage and high current capabilities of SiC based devices has been already proved [1, 2]. High current VJFET are susceptible to be commercially available in a near future [3], and various power devices able to work at high temperature have been reported as well. In further development steps, SiC power integration should be considered as it is currently done in the Si Smart Power and modules technologies. Packaging remains the main constrain for high temperature operation, and up to date no specific industrial package has been reported. Another important aspect concerns the power switches protection. In case of short-circuit or over-load, power devices can reach high internal temperature values, subjecting packaged systems to high stress. It is thus desirable to have integrated protection features, as currently developed for Si, to avoid any related failure [4, 5], improving consequently the efficiency of the integrated power system.

In order to address such critical requirements in SiC, both current sensing and real time temperature monitoring are required. The current sensing structure reported in this paper offers a simple way of incorporating a protection feature to SiC power devices. In addition to previously reported temperature monitoring solutions, this approach offers current monitoring capabilities and facilitates its incorporation into a main control system, key points to get highly reliable SiC power devices and systems. In this sense, an integrated current sensor has been integrated in SiC (4H SiC-JFET power switches) and reported for the first time in this paper.

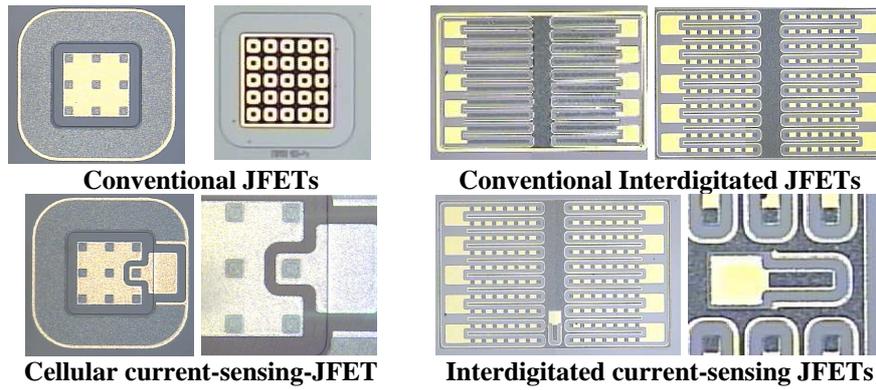


Fig. 1: Photography of fabricated conventional JFET (Top) and current-sensing JFET (bottom)

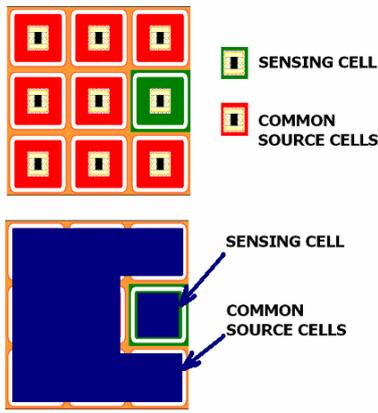


Fig. 2 : Mask view (left) and microscope view (right) of cellular SiC current- sensing- JFET

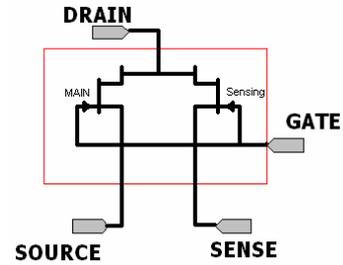


Fig. 3 : Equivalent Electrical Circuit

Device structure

In order to fabricate fully integrated high power devices and to get high reliability level, the current sensor has been monolithically integrated with the VJFET. The devices are fabricated with a buried gate layer VJFETs fabrication process [6] without any modification. This technological process allows single and multi-cellular layouts. Thus, both cellular and interdigitated VJFETs have been designed and fabricated; incorporating the integrated current sensing cell (Fig. 1 and 2).

An equivalent electrical circuit is shown in Fig. 3. The sensing ratio between the main and the sensed current, $n = (I_{main} + I_{sense})/I_{sense}$, is simply the geometrical ratio between the parallelized cells and the single sense cell. Current sensing principle has been suitably applied to current limiting device. 4H-SiC sense-JFETs have been packaged in DIL40 and characterized at both room temperature (RT) and high temperature (190°C).

Room temperature characterization of the current sensing

The experimental validation of the current sensing function is presented in Fig. 4 and Fig. 5 for two layouts. We can see that the current in the sensing cell (full lines) follows the device output current (dots). The cellular JFET shows an experimental sensing ratio $n = 8.8$ ($n=9$ expected), whereas the interdigitated JFETs sensing ratio is $n = 65$ ($n=62$ expected). The measurements performed on a packaged device using 4 probes techniques provide sensing ratio values closed to the expected ones. Furthermore, the $I(V_{DS})V_{GS}$ curves show that the sense-cell reacts instantaneously to both drain and gate bias changes, $n = (I_{main} + I_{sense})/I_{sense}$ being independent on the applied $[V_{DS}, V_{GS}]$ bias.

CELLULAR-JFET current sensor

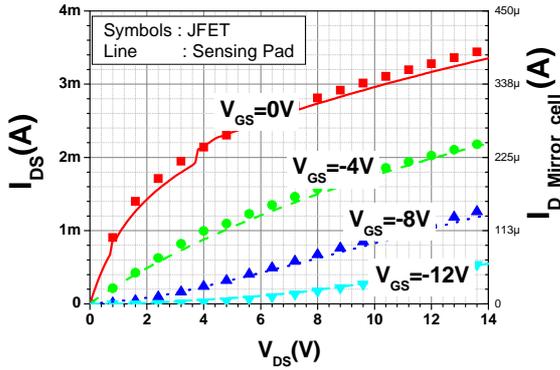


Fig. 4 : Experimental $I(V)$ I_{Main} (left), I_{sense} (right) ; $n = 8.8$ (expected 9)

INTERDIGITATED-JFET current sensor

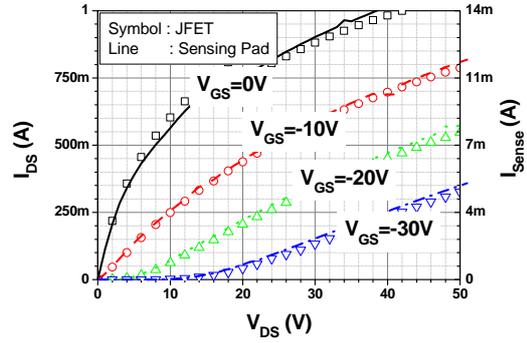


Fig. 5 : Experimental $I(V)$ I_{Main} (left), I_{sense} (right) ; $n = 65$ (expected 62)

At RT, the sensing current is independent on the switch working conditions. It has been experimentally demonstrated that the sensing ratio can be easily adjusted, depending on the application requirements, just designing an appropriate layout (cellular or interdigitated).

Thermal impact on current sensing

Infra-red thermal imaging was performed (Fig. 6) in order to check the temperature distribution of a packaged sense-JFET operating in a limiting state. Fig. 7 shows the monitored device, source, gate and sensing terminals and the thermal cross-section IR-line.

As inferred from Fig. 8 the current sensor temperature ($T_S=73^\circ\text{C}$) is similar to the finger temperature (T_F). The temperature distribution within the device can be assumed to be homogeneous. Thus, a mobility reduction caused by the self-heating effect is the same for the whole device and does not affect the current sensing value. As shown in Fig. 9, the sensing ratio is independent of the junction temperature (either RT or 190°C). ($n = 45$ for this device layout).

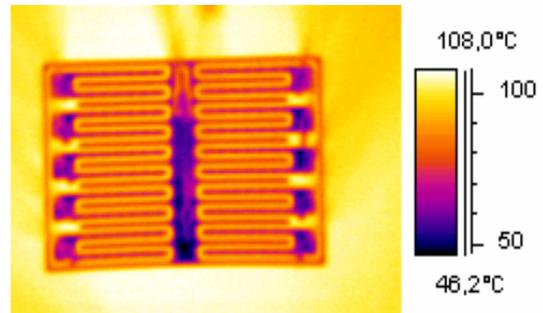


Fig. 6 : IR-imaging of the monitored sense-JFET

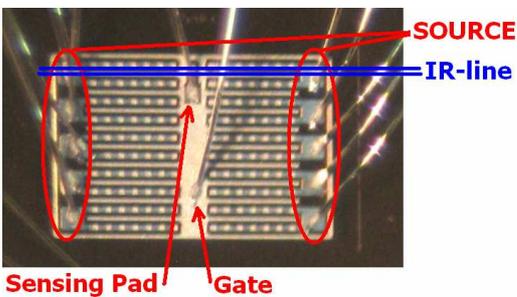


Fig. 7 : Top view photography of the monitored sense-JFET

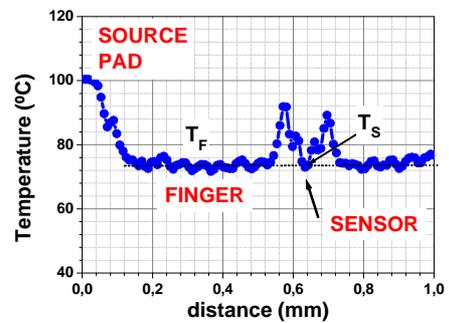


Fig. 8. Temperature distribution along the IR-line (see Fig. 7)

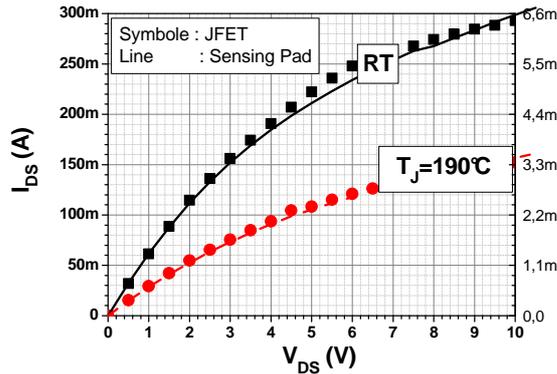


Fig. 9 : Temperature effect on 4H-SiC sense-JFET

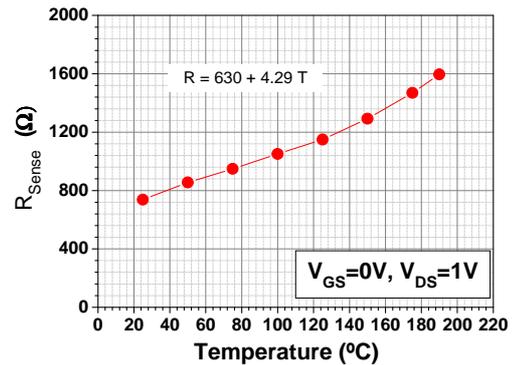


Fig. 10 : Sensing resistor dependence on temperature. (Linear regression is given using T in Celsius).

Furthermore, the current sensing pad can provide the device internal temperature (Fig. 10). Measuring the current and the sensing cell resistance value with an appropriate electronic driving board, both current and temperature real time monitoring are easily extracted.

Conclusion

We report and characterize for the first time a fully integrated current sensor implemented in 4H-SiC JFETs devices. Various layouts have been implemented to analyze both geometrical and driving (bias control) effects on current sensing ratio, n . Experiments validate the current sensing and temperature monitoring feature for SiC power devices. No change due to temperature on current sensing function has been evidenced up to 190°C, independently of the device layout. The perspectives in terms of integration and the benefits in terms of reliability are promising. Critical requirements such as real time current monitoring, over-current and/or short-circuit protection of high voltage SiC power devices, can be easily addressed. This principle can be advantageously applied to any cellular power switch, providing protection features and more reliable high temperature SiC power electronics.

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